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Investigation of Inverse Piezoelectric Effect and Trap Effect in AlGaN/GaN HEMTs Under Reverse-Bias Step Stress at Cryogenic Temperature

QING ZHU[1,2], XIAOHUA MA[2], (Member, IEEE), BIN HOU[2], MEI WU[2], JIEJIE ZHU[1,2], (Member, IEEE), LING YANG[1,2], MENG ZHANG[1,2], AND YUE HAO[2], (Senior Member, IEEE)

[1]School of Advanced Materials and Nanotechnology, Xidian University, Xi'an 710071, China
[2]State Key Discipline Laboratory of Wide Bandgap Semiconductor Technology, Xidian University, Xi'an 710071, China

Corresponding author: Xiaohua Ma (xhma_xidian@163.com)

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ABSTRACT The inverse piezoelectric effect and trap effect in GaN HEMTs under the high electric field by reverse-bias step stress at cryogenic temperature (CT, 77K) have been investigated. It is found that the inverse piezoelectric effect is suppressed while the trap effect is enhanced at CT. Due to the lower tensile stress in the as-grown AlGaN barrier at CT, the amplitude of the critical voltage related to inverse piezoelectric effect increases from 75V at 300K to 100V at CT, mitigating the irreversible degradation of the devices. The inverse piezoelectric effect dominates the degradation of reverse gate leakage, which is weakened at CT. However, the devices suffer from more degradation of I_d (decreases by 94.38%) and $G_{m,max}$ (decreases by 95.15%) at CT in the dark, induced by the serious trap effect due to the longer emission time. UV-light-assisted stress measurements have been utilized to identify the contribution of the two mechanisms to the degradation of device characteristics at CT. The degradation of $I_d(G_{m,max})$ is only 0.82% (3.31%) for the piezoelectric effect and 93.56% (91.84%) for trap effect at CT, respectively.

INDEX TERMS AlGaN/GaN, cryogenic temperature, reverse-bias stress, high electric field, inverse piezoelectric effect, trap, degradation.

I. INTRODUCTION

GaN exhibits high radiation hardness because of its high bond strength and high threshold displacement energy induced by the large bandgap [1]. As a result, GaN-based RF devices and power devices are perfect candidates for space exploration and satellite communications [2]. In addition to the radiation, the harsh space environment also includes extreme temperature. During the past few decades, the characteristics of devices at high temperature [3] and the reliability [4]–[7] on inverse piezoelectric effect, hot carriers, and electrochemical reaction have been widely investigated. However, the research on GaN-based devices at low temperature, especially cryogenic temperature, was relatively few.

Up to now, the studies of GaN based devices working at low temperature focus on the following aspects: (1) Enhanced transport properties at low temperature due to the weaker phonon scattering [8], [9]; (2) More excellent DC and RF properties at low temperature [10], [11]; (3) The kink effect associated with impact ionization [12]. Most researches have focused on the characterization of the GaN material and devices at low temperature. However, the low temperature reliability of GaN based HEMTs is lack of investigation [13].

Many reliability issues of GaN HEMTs are related to the high electric field in the AlGaN barrier layer and/or in the channel [14], [15]. Two models under the high electric field in the reverse-bias stress have been proposed. One is the

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electrons injected from the gate and then trapped in the barrier or at the AlGaN surface, resulting in the recoverable degradation. The trapped electrons would deplete the two-dimensional electron gas through modifying the electrostatics of the channel, which have influence on the characteristics of devices. The other is the inverse piezoelectric effect, resulting in the unrecoverable degradation. The inverse piezoelectric effect connects the high voltage with high mechanical stress in the pseudomorphic AlGaN barrier. The application of high voltage induces the high electric field, which results in the extra tensile stress in the AlGaN barrier. When the stored elastic energy density exceeds the tolerance of the barrier layer, the excessive tensile stress relaxes through the formation of crystallographic defects. This mechanism can be characterized by a critical voltage, beyond which the unrecoverable degradation takes place. Nevertheless, the two mechanisms under reverse-bias stress at low temperature are rarely investigated. And the contribution of different mechanisms to the degradation in devices is ambiguous.

In this paper, the inverse piezoelectric effect and trap effect have been investigated at cryogenic temperature (77K, marked as CT) by reverse-bias step stress. The amplitude of the critical voltage at CT is 25V higher than that at room temperature (RT), which suggests that it is more difficult for the inverse piezoelectric effect and irreversible degradation to take place at CT. However, the degradation of characteristics such as the drain current and the maximum transconductance, is more serious at CT, which is dominated by the trapping effect of electrons injected from the gate. The mechanisms under reverse-bias stress at CT have been investigated by theoretical calculation and experiments. The UV light has been introduced in the study of inverse piezoelectric effect. The quantitative analysis of the degradation due to inverse piezoelectric effect and trap effect has been made. The introduction of UV light, on the one hand, establishes the multiphysically-coupled environment including electricity, temperature and light, and on the other hand, provides a method to distinguish the above two effects.

II. DEVICE FABRICATION AND EXPERIMENTS

The AlGaN/GaN hetero-junction structure was grown by MOCVD on (0001) sapphire substrates. The epitaxial structure was composed of, from the substrate up, a nuclear layer, a 1.3 μm unintentionally doped (UID) GaN layer, a 1nm thick AlN interlayer and a 22 nm thick unintentionally doped $Al_{0.3}Ga_{0.7}N$ barrier layer. Mesa isolation was performed by Cl_2-based reactive ion etching (RIE). Ohmic contact was realized by consecutively annealing the e-beam evaporated Ti/Al/Ni/Au stacks at 830 °C for 30 s in nitrogen ambient. It was followed by a 60-nm plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 passivation layer. The Si_3N_4 in the gate area was removed by RIE, and then the metal stacks of Ni/Au/Ni were deposited to form the Schottky contact. The length of the gate was 0.8 μm. The gate-to-source spacing and gate to drain spacing were both 1.6 μm.

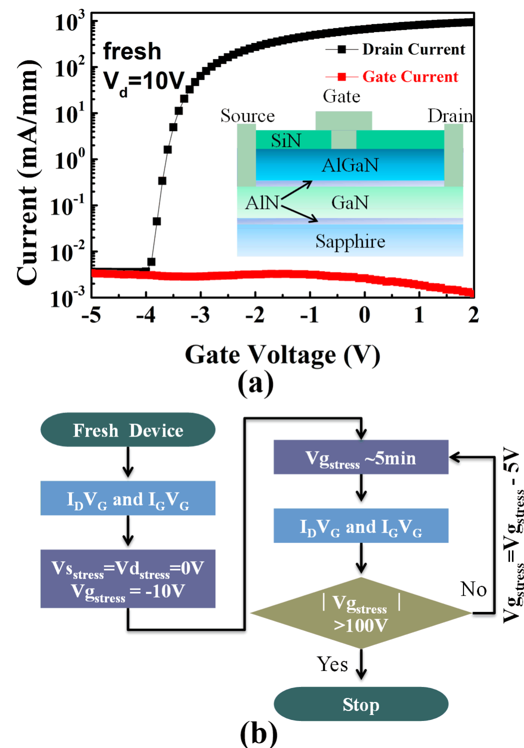


FIGURE 1. (a) The transfer characteristics of the fresh device at room temperature (RT). Inset: Cross-section view of the device structure utilized in the step-stress experiments. (b) Reverse-bias step stress procedure at room temperature (RT) and cryogenic temperature (CT).

The structure of devices utilized in this paper is shown in Fig. 1a. The fresh device shows $I_{d,max}$ of 836 mA/mm, V_{th} of -3.64V and $G_{m,max}$ of 217 mS/mm. The off-state drain leakage current is approximately equal to the gate leakage current. The stress experiments were carried out as the procedure in Fig.1b. The gate voltage was stepped from -10V to -100V in the step of 5V while keeping $V_s = 0V$ and $V_d = 0V$. The device was stressed for 5min at each step and the stress currents were monitored simultaneously. At the end of each step, the gate stress voltage was removed. And then transfer characteristics at $V_d = 10V$ and $I_g - V_g$ curves ($V_s = 0$ and drain floating) were measured in a short time and the next voltage step was applied immediately. This cycle at a certain frequency was repeated until the end of the step-stress experiments. The step-stress experiments in the dark and under the UV light (380nm) were both carried out at CT and RT, respectively.

III. RESULTS AND DISCUSSION

This section focuses on the results and discussion on the degradation of devices under reverse-bias step stress. Two mechanisms including inverse piezoelectric effect and trap effect will be discussed at cryogenic temperature, whose contribution to the degradation of device characteristics will be investigated in detail.

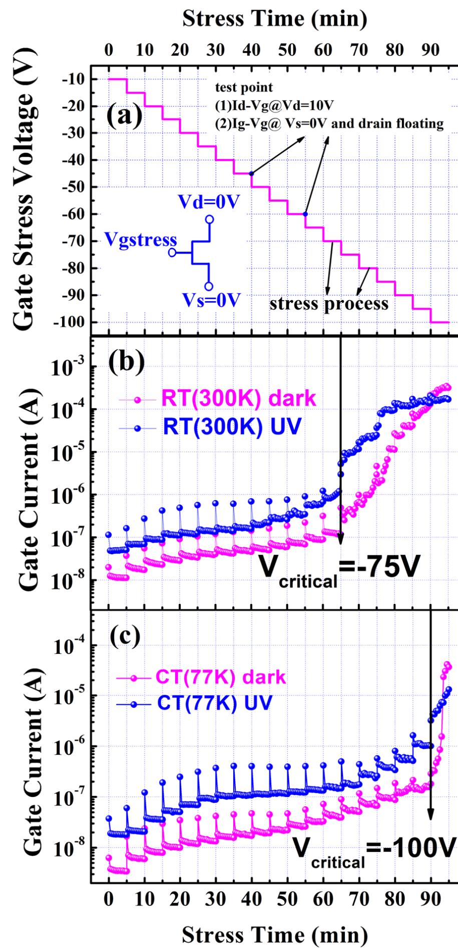


FIGURE 2. (a) Stress scheme used in this study. The gate stress current in the step-stress experiments at RT (b) and at CT (c) in the dark and under the UV light, respectively.

A. INVERSE PIEZOELECTRIC EFFECT

Fig. 2 shows the gate stress current in the reverse-bias step stress experiments performed at RT and CT in the dark and under 380nm UV light, respectively. The gate stress current at RT is higher than that at CT. This is because that the reverse gate leakage current is found to be dominated by Frenkel-Poole emission (a trap-assisted process), and Fowler-Nordheim tunneling (an electric-field-dominated process) [16], [17]. In this paper, for the devices with $Lg = 0.8\mu m$ under large reverse-bias voltage, the electric field increases faster at the edge of the gate than that under the center of the gate. At the lower reverse gate voltage bias, the gate leakage mechanism both at the edge and under the center of the gate electrode are dominated by F-P emission. And then, when reverse gate voltage bias increases, at the gate edge the gate leakage mechanism is dominated by F-N tunneling due to the higher reverse electric field; while under the center of the gate electrode, the gate current is still dominated by F-P emission [18]. As the voltage continues increasing, both the two regions of the gate electrode are dominated by the F-N tunneling mechanism. Frenkel-Poole emission would be enhanced by high temperature and electric field. Since trap emission is also enhanced by UV light, the gate stress current under UV light is higher than that in the dark.

The high electric field at the edge of the gate is one of the main factors of devices failure [19], where the inverse piezoelectric effect tends to occur. The critical voltages, beyond which irreversible degradation takes place due to inverse piezoelectric effect, are −75V at RT and −100V at CT in the dark, as shown in Fig. 2. That is to say, it is more difficult for the inverse piezoelectric effect to take place at the lower temperature. As shown in Fig.2, when −100V is applied, the gate stress current under UV light becomes higher than that in the dark. Before the inverse piezoelectric effect takes place, the electrons are injected from gate into the AlGaN barrier by the high electric field. And the injected electrons could be trapped in the barrier in the dark. After the critical voltage, the electrons detrapped from the traps in the barrier contribute to the gate stress current along the newly formed leak path, which results in that the gate stress current in the dark increases more quickly and slightly larger than that under the UV light at $V_{gstress} = -100V$. The gate stress current increases more quickly after critical voltage at CT than that at RT. This is because that at CT the inverse piezoelectric effect occurs at a larger bias and more electrons are trapped in the barrier before critical voltage, and then more trapped electrons contribute to the gate stress current at CT after critical voltage.

In the following, the reason for the higher amplitude of the critical voltage at CT will be discussed. As mentioned in section I, electrons could be injected from the gate to the AlGaN surface by high electric field. The trap states at the AlGaN surface are identified as donor-like traps. If electrons are trapped at the surface, the 2DEG concentration is reduced due to the electrostatic balance. It has been reported that the surface trapping effect could relieve the electric field peak at the gate edge to some extent [20]. To eliminate the surface trapping effect and focus on the main influence of the temperature on the piezoelectric effect, the UV light was utilized. As shown in Fig. 2, the critical voltages under the UV light are the same as those in the dark, which indicates that the surface charging has little influence on the inverse piezoelectric effect.

As mentioned in section I, the inverse piezoelectric effect connects the high voltage with the mechanical stress (usually tensile stress) in the AlGaN barrier. For GaN-based HEMTs, due to the existence of lattice mismatch, the AlGaN barrier suffers from the tensile stress, which would be enhanced under the reverse-bias voltage. To further investigate the difference of inverse piezoelectric effect between CT and RT, the tensile stress in the AlGaN barrier need to be calculated.

Firstly, the lattice mismatch at different temperature is calculated. S_0 denotes the as-grown lattice mismatch between AlGaN and GaN, which remains unchanged even with

additional electric field, and can be given as follows [21]:

$$S_0 = \frac{a_{GaN}(T) - a_{AlGaN}(T)}{a_{AlGaN}(T)} \tag{1}$$

where a_{GaN} and a_{AlGaN} represent the lattice constants of GaN and AlGaN, respectively. The temperature dependence of a can be described as

$$\mathrm{a}(T) = a_0 \times [1 + \alpha \times (T - T_0)] \tag{2}$$

where a_0 is the lattice constant at RT [21] and T_0 is 300K. The calculation results of S_0 are shown in Fig. 3a.

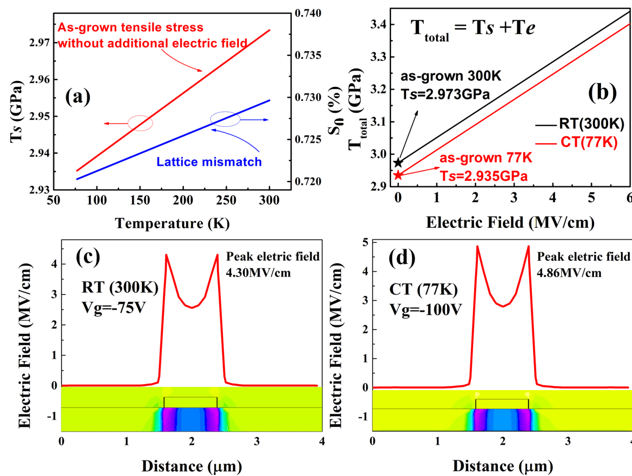


FIGURE 3. (a) The temperature dependence of lattice mismatch and as-grown tensile stress (Ts) without additional electric field. (b) Total tensile stress (T_{total}) with additional electric field. (c) ATLAS simulation of electric field at Vg = −75V at RT (300K). (d) ATLAS simulation of electric field at Vg = −100V at CT (77K).

TABLE 1. The parameters used in the calculation of the mechanical stress in the barrier layer [21]–[23].

Parameters	GaN	AlN	$Al_{0.3}Ga_{0.7}N$
$\alpha(K^{-1})^a$	5.59e-6	4.2e-6	5.17e-6
$C_{11}(Gpa)^b$	350	356	351.8
$C_{12}(Gpa)^b$	110	121	113.3
$C_{13}(Gpa)^b$	104	113	106.7
$C_{33}(Gpa)^b$	405	373	395.4
$e_{31}(C/m^2)^c$	-0.49	-0.6	-0.523
$e_{33}(C/m^2)^c$	0.73	1.46	0.949

[a] Thermal expansion coefficients.
[b] Elastic constants.
[c] Piezoelectric tensors.

Then the total tensile stress (T_{total}) in the AlGaN barrier is given by Joh [20].

$$\begin{aligned} T_{total} &= (C_{11}+C_{12} - 2\times\frac{C_{13}^2}{C_{33}})\times S_0 + (\frac{C_{13}\times e_{33}}{C_{33}} - e_{31})\times E \\ &\equiv Ts + Te \end{aligned} \tag{3}$$

where the elastic constant C and the piezoelectric tensor e are listed in Table 1, and E denotes the additional electric field. The effect of temperature on the parameters (C and e) is so small that it will be ignored. [22], [24] Ts represents the as-grown tensile stress without additional electric field, which decreases as temperature decreases, as shown in Fig. 3a. The Ts at CT is 0.038GPa lower than that at RT. The tensile stress induced by additional electric field is expressed as Te. At CT, Ts is lower, and then the higher electric field is required to achieve the tolerance of the barrier layer leading to the occurrence of the inverse piezoelectric effect, as shown in Fig. 3b. As a result, the amplitude of the critical voltage related to the inverse piezoelectric effect at CT is larger than that at RT (Fig. 2). To verify the accuracy of the calculation, the vertical electric fields at critical voltage have been simulated by Silvaco Atlas. For a fixed T_{total} corresponding to the onset of the inverse piezoelectricity, the difference in the electric field between RT and CT is 0.498MV/cm, as shown in Fig. 3b. The simulated peak electric field at critical voltage (V_g = −75V) at RT is 4.30MV/cm, and 4.86MV/cm for critical voltage (V_g = −100V) at CT. The difference in the simulated peak electric fields between RT and CT is 0.56MV/cm, which is close to the calculated result, indicating that the calculated results agree with the experimental results in Fig.2 (25V difference of critical voltage between RT and CT).

B. TRAP BEHAVIOR OF ELECTRONS INJECTED FROM THE GATE

The transfer characteristics of the devices before and after stress are shown in Fig.4. The off-state current increases after $V_{gstress}$ = −100V both in the dark and under the UV light, due to the inverse piezoelectric effect. The on-state current decreases in the dark, which is more serious at 77K.

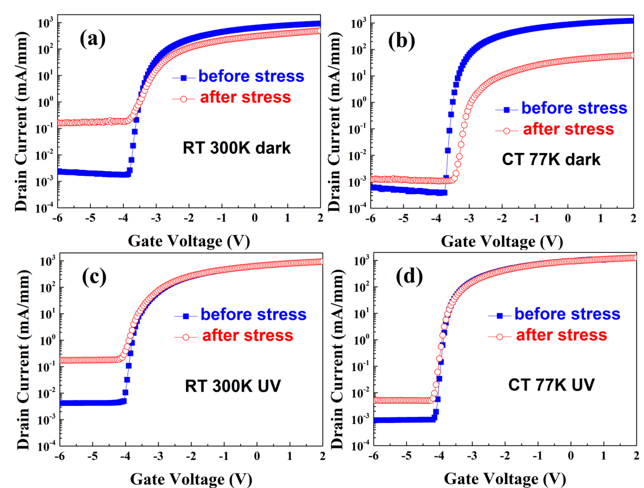


FIGURE 4. Transfer characteristics of the devices before and after stress. (a) RT dark, (b) CT dark, (c) RT UV, (d) CT UV.

To investigate the degradation of the devices, trap behavior has been considered. The electrons are injected into the traps both in the AlGaN barrier and at the interface of SiN/AlGaN

by the high electric field under the reverse-bias stress [25], as shown in Fig. 7b. The trapped electrons could be detrapped by thermal activation at the intervals of alternating stress. The emission time of traps (τ_T) is given by

$$\tau_T = (\sigma_T N_c \nu_T)^{-1} \exp(\frac{E_T}{kT}) \tag{4}$$

where σ_T is the capture cross section of the trap, N_c is the density of states in the conduction band, ν_T is the average thermal velocity of the carriers and E_T is the trap state activation energy. When the temperature drops to CT, the electrons can hardly release from the traps by thermal activation. In other words, the τ_T increases as the temperature decreases.

In order to further investigate the degradation of devices during the stress procedure, typical characteristic parameters, e.g. n_s, V_{th} and I_d, are analyzed.

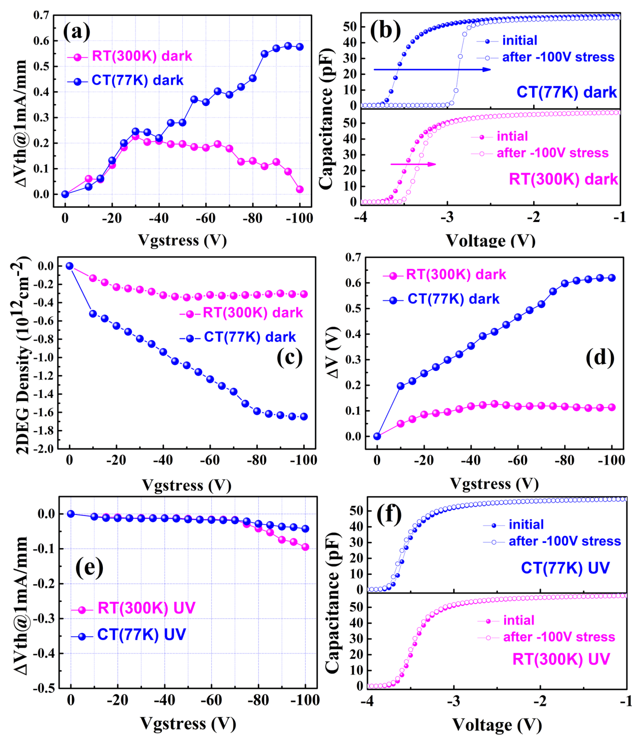


FIGURE 5. **(a) The variation of threshold voltage after each step stress at RT and CT in the dark. (b) C-V characteristics in AlGaN/GaN schottky diodes before and after stress in the dark. (c) 2DEG density derived from C-V characteristics in the dark. Inset: the top view of the AlGaN/GaN schottky diode. (d) The voltage drift induced by the decreasing 2DEG density in the dark. (e) The variation of threshold voltage after each step stress at RT and CT under the UV light. (f) C-V characteristics in AlGaN/GaN schottky diodes before and after stress under the UV light.**

The threshold voltage (V_{th}) is determined as the gate voltage corresponding to the drain current of 1mA/mm. As shown in Fig. 5a, as the stress voltage increases, the V_{th} shifts positively firstly and then tend to saturation at CT in the dark. For RT, the V_{th} shifts positively first, then reaches saturation and finally shifts negatively. The positive drift of V_{th} would be induced by the electrons trapped in the AlGaN under the gate. However, After -75V reverse-biased gate stress at RT, the off-state characteristics (including the gate leakage current, drain leakage current and subthreshold swing) are degraded due to the inverse piezoelectric effect, as shown in Fig.8. In this work, V_{th} is determined as the gate voltage corresponding to the drain current of 1mA/mm. Due to the poor off-state characteristics after critical voltage, more negative gate voltage is required to reduce the drain current below 1mA/mm. Therefore, the V_{th} shifts negatively at RT after -75V reverse-biased gate stress along with drastically increased off-state drain leakage current and subthreshold swing.

To investigate the trap effect under the gate, C-V characteristics were measured during the step stress in the dark. AlGaN/GaN schottky diodes were used to study the C-V characteristics, which consisted of a circular gate contact of a diameter of 130 μm and a surrounding ohmic contact with an Ohmic-Schottky separation of 30 μm. In the experiments, the procedure was the same with that described in section II (Fig. 1b), except that the monitoring parameters were C-V related characteristics. The C-V curves before and after the step stress are shown in Fig. 5b, which shift positively as the stress voltage increases. Then the 2DEG density (n_s) can be calculated by integrating the C-V curves as follows [26]:

$$n_s = \frac{1}{q} \int_{V_{pinch-off}}^{V_{on}} CdV \tag{5}$$

where q represents the magnitude of electronic charge, V is the voltage, and the pinch-off voltage ($V_{pinch-off}$) is defined as the maximum gate voltage for capacitance smaller than 10nF/cm^2, the on-state voltage V_{on} is defined as the gate voltage for the electron concentration reaching the peak value.

The n_s as a function of the reverse-bias step stress is shown in Fig. 5c. The n_s decreases firstly as the increase of stress voltage and tends to be saturated both at RT and CT. What's more, the reduction of n_s at CT is larger than that at RT. This phenomenon can be explained as follows: at the beginning of the stress experiment, as the stress voltage increases gradually, electrons are injected into the traps in the AlGaN barrier and the n_s is partly depleted by the trapped electrons, due to the electrostatic balance, at both RT and CT. As mentioned above, the electrons could be detrapped by thermal activation at the intervals of alternating stress. Namely, the electron-trapping and electron-detapping process can both take place during the experiments. Then in fact, the n_s is influenced by the net trapped electrons in the AlGaN barrier. When the number of electrons trapped and detrapped reaches dynamic balance, the net trapped electrons tend to be saturated and the n_s reaches its minimum value. It is noticed that the detapping process relies on the τ_T as mentioned in (4). Since τ_T at CT is larger than that at RT, the detrapping process at CT is difficult to occur, then the net number of trapped electrons is larger, as a result, the reduction of n_s is larger.

As shown in Fig. 5d, ΔV shifts positively as the increasing of stress voltage and then tends to saturation both at RT and CT, which can be easily explained from (6), considering the

variation of Δn_s.

$$\Delta V = q \times \Delta n_s / C \tag{6}$$

where q represents the magnitude of electronic charge, and C is the unit area capacitance. The variation of ΔV resulted from the variation of n_s is consistent with the drift of V_{th} in the dark before critical voltage.

The variation of V_{th} under the UV light is shown in the Fig.5e. The V_{th} shifts negatively slightly before critical voltage because the electrons are detrapped in the barrier by the UV light. The V_{th} shifts more negatively after critical voltage due to the poor off-state characteristics, for the same reason in the dark as mentioned above. The C-V characteristics in AlGaN/GaN schottky diodes before and after stress under the UV light are shown in the Fig. 5f. The C-V curves shifts negatively slightly, which means that the n_s under the gate during the stress under the UV light changes little. Therefore, the V_{th} shifts slightly under the UV light due to nearly unchanged n_s.

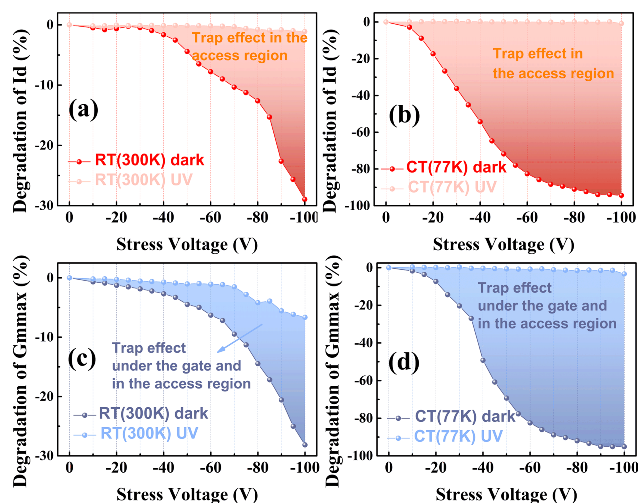


FIGURE 6. The drain current after each step stress at RT (a) and CT (b) derived from transfer characteristics (Vd = 10V) in the dark and under the UV light, respectively. The transconductance after each step stress at RT (c) and CT (d) in the dark and under the UV light, respectively.

As to the degradation of Id, the extraction methods from the transfer characteristics are generally two types. One is the Id corresponding to a fixed gate voltage. And the other is the Id corresponding to a varying gate voltage with Vth correction [27]. As mentioned above, the V_{th} shifts during the step stress. Hence, the degradation of Id at Vg $= V_{th} + 5V$ is shown in Fig. 6a, to exclude the influence of Vth drift. The Id decreases by 28.95% and the Gm, max decreases by 28.15% at the end of the step stress at RT in the dark, while the reduction of which is 94.38% and 95.15% at CT, respectively. For experiments under UV light, the Id decreases by 1.11% at RT and 0.82% at CT, respectively. The Gm, max reduces by 6.66% at RT and 3.31% at CT, respectively. The shaded areas of Fig. 6 are induced by trap effect, which will be discussed in section C.

The whole trap behavior during the step stress experiments can be illuminated in Fig. 7. Generally, the possible

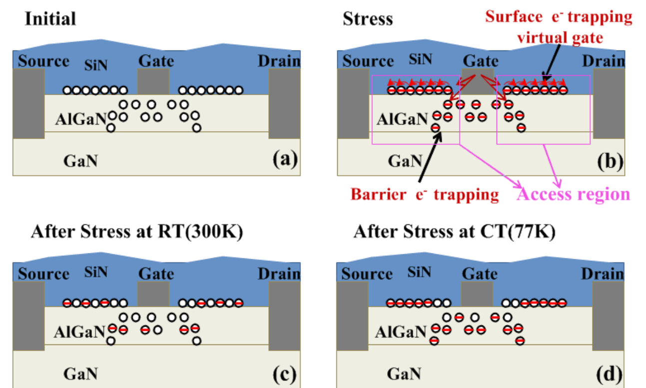


FIGURE 7. The schematic diagram of trap behavior before and after the step stress experiments.

distribution of the traps in the fresh devices can be simply presented in Fig. 7a. When the reverse-bias voltage is applied to the devices, the electrons are injected into the traps in the AlGaN barrier and at the SiN/AlGaN interface by the high electric field, as shown in Fig. 7b. The trapped electrons at the SiN/GaN interface form a "virtual gate", which would deplete the access region channel and result in the degradation of I_d and $G_{m,max}$. The length of "virtual gate" increases as the reverse-bias voltage increases, which results in more severe degradation.

The trap behavior also happens in the AlGaN barrier, which has similar influence on the I_d and $G_{m,max}$. The trapped electrons could be detrapped partly by thermally activation at RT. However, the longer τ_T at CT induces more serious degradation of I_d and $G_{m,max}$, and a similar phenomenon is described in the above C-V measurements in the dark. And the trapped electrons would be activated by the UV light. That is to say, the trapping process is almost eliminated by the UV light.

Finally, the gate reverse current (I_g) at $V_{gs} = -10V$ extracted from the Ig-Vg curves during the stress experiments is shown in Fig. 8a. The off-state drain current (I_{doff}) @$V_{gs} = -6V$ extracted from transfer characteristics during the stress experiment is shown in Fig. 8b. The same trend of the I_g and I_{doff} during the stress suggests that their degradation is dominated by the same mechanism. The I_g and I_{doff} decrease firstly as the increase of stress voltage, then remain constant and finally increase rapidly after critical voltage in the dark. However, the I_g and I_{doff} under the UV light stay at a stable value until the critical voltage. This is because of the trap effect in the AlGaN barrier under the gate. The trapped electrons in the barrier lift the conduction band and suppress the following electrons-injection-process from the gate [28], resulting in the decrease of I_g and I_{doff} both from Poole-Frenkel emission and Fowler-Nordheim tunneling [29]. For experiments under the UV light, the constant I_g and I_{doff} before critical voltage are due to the elimination of trapping process by light activation. When the stress voltage increases to the critical voltage, new path leakage in the barrier occurs,

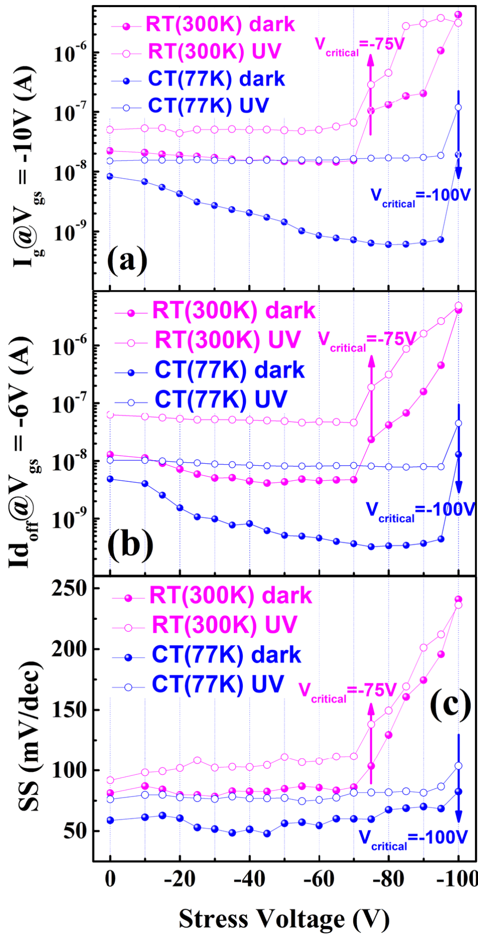


FIGURE 8. The gate reverse current I_g @$V_{gs} = -10V$ (a), off-state drain current @ $V_{gs} = -6V$(b), and the subthreshold swing (SS) (c) after each step stress in the dark and under the UV light at both CT and RT, respectively.

and the I_g and I_{doff} increases rapidly [30]. The SS extracted from the Id-Vg curves during the stress experiments is also presented in Fig. 8c, which increases after critical voltage and is closely related to the off-state current (dominated by gate reverse current).

C. CONTRIBUTION OF DIFFERENT MECHANISMS

To further analyze the contribution of different mechanisms to the degradation of device characteristics, the characteristics after stress in the dark and under UV light are compared in detail. The related mechanisms in the experiments are trap behavior under the gate and in the access region, and permanent structure damage caused by inverse piezoelectric effect.

When the UV light is applied, the characteristics of devices remain unchanged before critical voltage. After critical voltage, the I_g and SS increases rapidly, while the I_d and $G_{m,max}$ decrease slightly.

The UV light is applied to eliminate the trap effect during the stress. And the degradation of characteristics after critical voltage under the UV light is induced only by the permanent structure damage, namely inverse piezoelectric effect. From Fig. 6 and Fig. 8, the inverse piezoelectric effect induces serious degradation of I_g, I_{doff} and SS, but has little impact on I_d and $G_{m,max}$.

The contribution of these two mechanisms can be described by

$$\Delta Parameter_{pe} = \Delta Parameter_{UV}$$
$$\Delta Parameter_{te} = \Delta Parameter_{dark} - \Delta Parameter_{UV} \quad (7)$$

where Δ Parameter represents the degradation of device characteristics including I_d and $G_{m,max}$. The subscripts pe and te refer to the inverse piezoelectric effect and the trap effect, respectively.

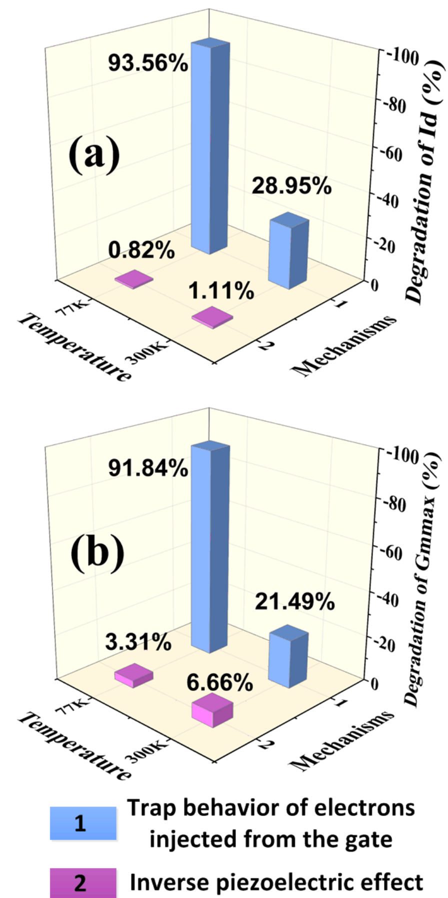


FIGURE 9. The degradation of drain current (a) and the maximum trans-conductance (b) induced by different mechanisms at CT and RT after −100V stress, respectively.

The drift of V_{th} is related to the trap behavior under the gate. The degradation of I_d derived at $V_g = V_{th}+5V$ excludes the impact of V_{th}. That is to say, the degradation of I_d induced only by the trap effect in the access region, as shown in the shaded areas of Fig. 6. The G_m is connected with the intrinsic transconductance ($G_{m,i}$) and the resistance between source and gate (R_{gs}). Since $G_{m,i}$ and R_{gs} are mostly affected by the traps under the gate and in the access region, respectively, the

trap behavior in the both regions has impact on the degradation of $G_{m,max}$. The detailed degradation of I_d and $G_{m,max}$ is shown in Fig. 9a and b, respectively.

IV. CONCLUSION

The degradation of AlGaN/GaN HEMTs under reverse-bias step stress at CT and RT is investigated. The amplitude of critical voltage related to the inverse piezoelectric effect at CT is higher than that at RT, for the smaller tensile stress in the AlGaN barrier at CT without additional voltage. The UV light has little impact on the inverse piezoelectric effect. It is the temperature instead of the traps that dominates on the critical voltage, which has been verified by the theoretical calculations and simulation results. The contribution of the two mechanisms to the degradation of device characteristics is distinguished by UV light experiments. The inverse piezoelectric effect induces the increase of I_g at $V_{gs} = -10V$, and has little impact on I_d and $G_{m,max}$. Trapping behavior dominates the positive V_{th} drift and the decrease of I_d and $G_{m,max}$. Devices at CT suffer more serious degradation of I_d and $G_{m,max}$ due to the longer τ_T at lower temperature. The quantitative analysis of the degradation of characteristics due to different mechanisms provides more explicit guidance for the process optimization of the devices and is more meaningful for the practical application of devices. The results presented in this paper are meaningful for reliability analysis of GaN-based power devices in the cryogenic-temperature environment, and provides reference for their application in deep space exploration.

REFERENCES

[1] S. J. Pearton, F. Ren, E. Patrick, M. E. Law, and A. Y. Polyakov, "Review-ionizing radiation damage effects on GaN devices," *ECS J. Solid State Sci. Technol.*, vol. 5, no. 2, p. Q35, 2016.

[2] Q. Dong, Y. X. Liang, D. Ferry, A. Cavanna, U. Gennser, L. Couraud, and Y. Jin, "Ultra-low noise high electron mobility transistors for high-impedance and low-frequency deep cryogenic readout electronics," *Appl. Phys. Lett.*, vol. 105, no. 1, Jul. 2014, Art. no. 013504.

[3] N. Maeda, M. Hiroki, S. Sasaki, and Y. Harada, "High-temperature characteristics in normally off AlGaN/GaN heterostructure field-effect transistors with recessed-gate enhanced-barrier structures," *Appl. Phys. Express*, vol. 5, no. 8, Jul. 2012, Art. no. 084201.

[4] F. Sang, M. Wang, M. Tao, S. Liu, M. Yu, B. Xie, C. P. Wen, J. Wang, W. Wu, Y. Hao, and B. Shen, "Time-dependent threshold voltage drift induced by interface traps in normally-off GaN MOSFET with different gate recess technique," *Appl. Phys. Express*, vol. 9, no. 9, Jul. 2016, Art. no. 091001.

[5] T. Brazzini, M. A. Casbon, M. J. Uren, P. J. Tasker, H. Jung, H. Blanck, and M. Kuball, "Hot-electron electroluminescence under RF operation in GaN-HEMTs: A comparison among operational classes," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2155–2160, May 2017.

[6] F. Gao, S. C. Tan, J. A. del Alamo, C. V. Thompson, and T. Palacios, "Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 437–444, Feb. 2014.

[7] F. Gao, D. Chen, H. L. Tuller, C. V. Thompson, and T. Palacios, "On the redox origin of surface trapping in AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 115, no. 12, Mar. 2014, Art. no. 124506.

[8] J. Zhang, X. Yang, J. Cheng, Y. Feng, P. Ji, A. Hu, F. Xu, N. Tang, X. Wang, and B. Shen, "Enhanced transport properties in InAlGaN/AlN/GaN heterostructures on Si (111) substrates: The role of interface quality," *Appl. Phys. Lett.*, vol. 110, no. 17, Apr. 2017, Art. no. 172101.

[9] F. Meng, J. Zhang, H. Zhou, J. Ma, J. Xue, L. Dang, L. Zhang, M. Lu, S. Ai, X. Li, and Y. Hao, "Transport characteristics of AlGaN/GaN/AlGaN double heterostructures with high electron mobility," *J. Appl. Phys.*, vol. 112, no. 2, Jul. 2012, Art. no. 023707.

[10] M. A. Alim, A. A. Rezazadeh, and C. Gaquiere, "Temperature effect on DC and equivalent circuit parameters of 0.15-*mu*m gate length GaN/SiC HEMT for microwave applications," *IEEE Trans. Microw. Theory*, vol. 64, no. 11, p. 3483, Nov. 2016.

[11] A. Endoh, "Effect of temperature on cryogenic characteristics of AlGaN/GaN MIS-HEMTs," *Phys. Status Solidi C*, vol. 6, S2, p. S964, Jun. 2009.

[12] J. K. Kaushik, V. R. Balakrishnan, B. S. Panwar, and R. Muralidharan, "On the origin of kink effect in Current-Voltage characteristics of AlGaN/GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3351–3357, Oct. 2013.

[13] E. Iervolino, "Investigation of AlGaN/GaN HEMTs degradation with gate pulse stressing at cryogenic temperature," *AIP Adv.*, vol. 7, no. 9, Sep. 2017, Art. no. 095317.

[14] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in GaN HEMTs-Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013.

[15] M. Meneghini, I. Rossetto, C. De Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, and G. Meneghesso, "Reliability and failure analysis in power GaN-HEMTs: An overview," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, p. 2.

[16] L. Xia, A. Hanson, T. Boles, and D. Jin, "On reverse gate leakage current of GaN high electron mobility transistors on silicon substrate," *Appl. Phys. Lett.*, vol. 102, no. 11, Mar. 2013, Art. no. 113510.

[17] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, no. 2, Jan. 2006, Art. no. 023703.

[18] Y. Chen, X. Ma, W. Chen, B. Hou, J. Zhang, and Y. Hao, "Influence of the gate edge on the reverse leakage current of AlGaN/GaN HEMTs," *AIP Adv.*, vol. 5, no. 9, Sep. 2015, Art. no. 097154.

[19] D. Marcon, G. Meneghesso, T.-L. Wu, S. Stoffels, M. Meneghini, E. Zanoni, and S. Decoutere, "Reliability analysis of permanent degradations on AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3132–3141, Oct. 2013.

[20] W.-W. Chen, X.-H. Ma, B. Hou, J.-J. Zhu, Y.-H. Chen, X.-F. Zheng, J.-C. Zhang, and Y. Hao, "Impacts of SiN passivation on the degradation modes of AlGaN/GaN high electron mobility transistors under reverse-bias stress," *Appl. Phys. Lett.*, vol. 105, no. 17, Oct. 2014, Art. no. 173507.

[21] J. Joh, F. Gao, T. Palacios, and J. A. del Alamo, "A model for the critical voltage for electrical degradation of GaN high electron mobility transistors," *Microelectron. Rel.*, vol. 50, no. 6, pp. 767–773, Jun. 2010.

[22] Y. Xiang, X. Chen, C. Ji, X. Yang, F. Xu, Z. Yang, X. Kang, B. Shen, G. Zhang, and T. Yu, "Temperature-dependent polarization characteristics in $Al_{0.25}Ga_{0.75}N$/AlN/GaN heterostructure," *Appl. Phys. Lett.*, vol. 108, no. 6, Feb. 2016, Art. no. 063503.

[23] S. Choi, E. Heller, D. Dorsey, R. Vetury, and S. Graham, "Analysis of the residual stress distribution in AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 113, no. 9, Mar. 2013, Art. no. 093510.

[24] K. Adachi, H. Ogi, A. Nagakubo, N. Nakamura, M. Hirao, M. Imade, M. Yoshimura, and Y. Mori, "Elastic constants of GaN between 10 and 305 k," *J. Appl. Phys.*, vol. 119, no. 24, Jun. 2016, Art. no. 245111.

[25] M. Meneghini, A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni, "Electroluminescence analysis of time-dependent reverse-bias degradation of HEMTs: A complete model," in *Proc. Int. Electron Devices Meeting*, Dec. 2011, pp. 19–25.

[26] J. Zhu, Q. Zhu, L. Chen, B. Hou, L. Yang, X. Zhou, X. Ma, and Y. Hao, "Impact of recess etching on the temperature-dependent characteristics of GaN-based MIS-HEMTs with Al_2O_3/AlN gate-stack," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 840–847, Mar. 2017.

[27] C.-H. Dai, T.-C. Chang, A.-K. Chu, Y.-J. Kuo, S.-C. Chen, C.-C. Tsai, S.-H. Ho, W.-H. Lo, G. Xia, O. Cheng, and C. Tung Huang, "On the origin of hole valence band injection on GIFBE in PD SOI n-MOSFETs," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 540–542, Jun. 2010.

[28] W.-W. Chen, X.-H. Ma, B. Hou, S.-L. Zhao, J.-J. Zhu, J.-C. Zhang, and Y. Hao, "Reliability investigation of AlGaN/GaN high electron mobility transistors under reverse-bias stress," *Microelectron. Rel.*, vol. 54, nos. 6–7, pp. 1293–1298, Jun. 2014.

[29] E. Arslan, S. Butun, and E. Ozbay, "Leakage current by Frenkel-Poole emission in Ni/Au Schottky contacts on $Al_{0.83}In_{0.17}N$/AlN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 94, no. 14, Apr. 2009, Art. no. 142106.

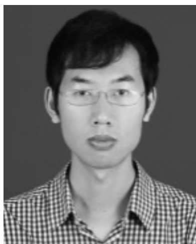
[30] J. Joh and J. A. del Alamo, "Impact of gate placement on RF power degradation in GaN high electron mobility transistors," *Microelectron. Rel.*, vol. 52, no. 1, pp. 33–38, Jan. 2012.

QING ZHU received the B.S. degree in electronic science and technology from Xidian University, Xi'an, China, in 2014, where she is currently pursuing the Ph.D. degree with the School of Advanced Materials and Nanotechnology.

Her current research interest includes the reliability analysis of GaN-based devices.

XIAOHUA MA (Member, IEEE) received the Ph.D. degree in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2007.

He is currently a Professor and the Vice Dean with the School of Microelectronics, Xidian University.



BIN HOU received the B.S. degree in electronic science and technology and the Ph.D. degree in materials physics and chemistry from Xidian University, Xi'an, China, in 2011 and 2018, respectively.

He holds a postdoctoral position at the School of Microelectronics, Xidian University. His current research interests include the fabrication and characterization of GaN-based normally-off field effect transistors.

MEI WU received the B.S. degree in microelectronics, in 2012, and the M.S. degree in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2015, where she is currently pursuing the Ph.D. degree with the School of Microelectronics.

Her current research interest includes the thermal characterization of GaN-based HEMTs

JIEJIE ZHU (Member, IEEE) received the B.S. degree in electronic science and technology and the Ph.D. degree in materials physics and chemistry from Xidian University, Xi'an, China, in 2011 and 2016, respectively.

He is currently a Lecturer with the School of Advanced Materials and Nanotechnology, Xidian University.

LING YANG received the B.S. degree in electronic science and technology and the M.S. and Ph.D. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2005, 2008, and 2011, respectively.

He is currently an Associate Professor with the School of Advanced Materials and Nanotechnology, Xidian University. His current research interests include the fabrication and characterization of GaN-based high frequency field effect transistors.

MENG ZHANG received the B.S. degree in electronic science and technology from Xidian University, Xi'an, China, in 2013, where he is currently pursuing the Ph.D. degree with the School of Advanced Materials and Nanotechnology.

His current research interests include the fabrication and characterization of GaN-based high frequency field effect transistors and GaN-based device with fin-shaped structure.

YUE HAO (Senior Member, IEEE) received the B.S. degree in semiconductor physics and devices from Xidian University, Xi'an, China, in 1982, and the Ph.D. degree in computing mathematics from Xi'an Jiaotong University, Xi'an, in 1990.

He is currently a Professor with the School of Microelectronics, Xidian University, and serves as the Vice President of Xidian University.