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High-Precision Adaptive Slope Compensation Circuit for DC-DC Converter in Wearable Devices

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ABSTRACT This paper presents a high precision adaptive slope compensation circuit for for DC-DC converter in wearable devices. Compared with the traditional adaptive slope compensation circuit, the comparator is used to sample the output voltage and input voltage, which greatly improves the accuracy.In this paper, the circuit is designed in UMC 0.18-μm CMOS Technology and verified by Virtuoso Spectre Circuit Simulator. The simulation results show that the accuracy of the adaptive slope compensation circuit in this paper can reach more than 96%.

INDEX TERMS Adaptive slope compensation, DC-DC, wearable devices, accuracy.

I. INTRODUCTION

With the rapid development of power electronic technology and computer-based information technology, power management chips are widely used in industrial, medical, military, consumer and other electronic products [1]. Since the appearance of power management chips, there have been many kinds of power management chips on the market, but after more than 50 years of development, switching power has experienced multiple innovations from technology to circuit structure. Now, switching mode power supply (SMPS) gradually replaces other types of power management chips, and it is the most widely used power management chip with superior performance on the market [2], [3].

In FIG. 1, there are several wearable devices that are commonly found on the market. In real life, people attach great value to the standby time of the battery for wearable devices [4]. Therefore, the battery is one of the key technologies of the wearable device [5]. In order to increase the endurance of electronic equipment, it is necessary to have good power management chips. Excellent and efficient power management chips can not only maintain the stability of electronic products, it is also the key to improve battery life. In this paper, a solution of inductance current fluctuation of switching power supply is proposed for low-power wearable devices powered by lithium-ion batteries to achieve the power stability of wearable devices. Switching power supply has the advantages of small size, light weight, large voltage range and high efficiency. It is widely used in terminal equipment, communication equipment and other electronic equipment dominated by electronic computers. It is an indispensable force for the rapid development of the electronic information industry. The switching mode power supply is a kind of power supply which uses modern power electronics technology to

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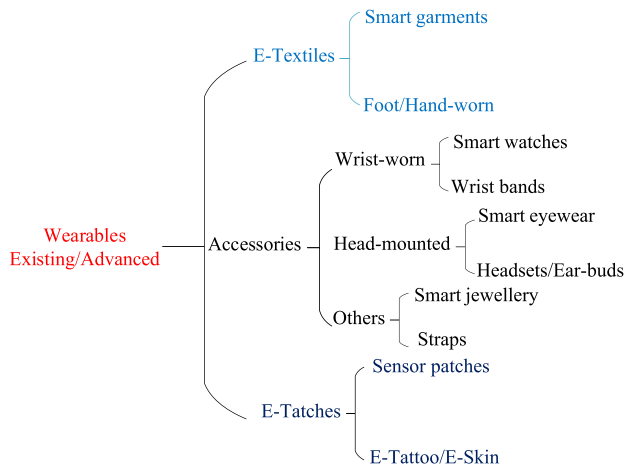

FIGURE 1. **Classification of wearable devices [8].**

control the ratio of turn-on and turn-off of semiconductor switching devices and stabilize the output voltage [6], [7]. In these switching mode power supplies, the control mode of the system mainly includes current mode and voltage mode. The voltage control mode has only one control loop, which adjusts the loop by monitoring the change of the output voltage, but its response speed is slow and complex compensation is needed. The current control mode contains two control loops, and the changes of voltage and current change at the same time to be adjusted in the loop, so the response speed is relative [9] faster. Because of the existence of the current feedback loop, the compensation structure of the circuit system is greatly simplified. Current control mode is widely used in DC-DC converters nowadays because of its fast response and simple compensation structure [10], [11]. In practical application, the appropriate slope compensation should be given according to the specific switching power circuit, otherwise, when the compensation amount of the slope compensation is too large, which means overcompensation, it will deteriorate the transient response and the load capacity of the whole system. On the contrary, if the compensation is insufficient, there may be under-compensation, which can not completely eliminate the defects of peak current control mode, and can not reliably guarantee the work of the whole circuit. Since the slope compensation of the DC-DC converters need to consider the input and output signals, it is therefore necessary to adjust adaptively changed according to the slope of the input-output voltage [12]. The adaptive slope compensation circuit designed in this paper is used in Buck type DC-DC converter, which adopts peak current control mode. Although the circuit system has a fast response to the transient response, when the duty cycle is more than 50%, it is prone to sub harmonic oscillation, and the chip stability is seriously affected. Therefore, in order to ensure the stability of the system, the slope compensation circuit must be added [13]. Slope compensation refers to adding slope compensation current to the current control loop of DC-DC converter to reduce the sub-harmonic oscillation caused by inductance current fluctuation [14], [15].

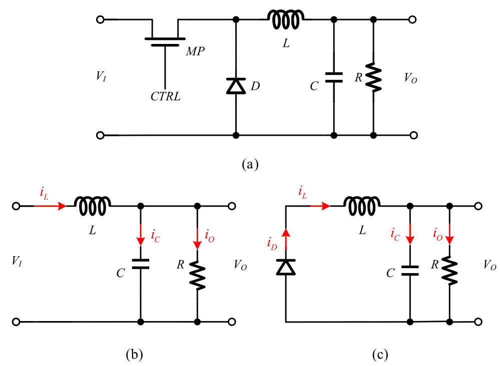

FIGURE 2. **(a) Buck switching mode power supply circuit structure; (b) Equivalent circuit of switching transistor in the conducting stage; (c) Equivalent circuit of switching transistor in the non-conducting stage.**

II. BASIC PRINCIPLE OF SLOPE COMPENSATION

A. BUCK SWITCHING MODE POWER SUPPLY

The average output voltage of Buck switching mode power supply V_O is always less than the input voltage V_I [16]. Fig. 2 (a) is the circuit structure of the Buck SMPS. When the power switching transistor MP is on, the current of the inductance increases and the electric energy is stored in the inductance in the form of magnetic energy; the freewheeling diode D is in the cut-off state; the capacitor C provides the energy for the load R. When the power switching transistor MP cutoff, the current of the inductance decreases, but it cannot be altered. The voltage reverse of the both ends of the inductance makes the freewheeling diode D on, the inductance releases the magnetic energy through the freewheeling diode D and recharges the load capacitor [17].

The following analysis ignores the equivalent resistance of the inductor, the conduction voltage of the switching transistor and the conduction voltage of the freewheeling diode.

When $0< t\leq T_{ON}$, the power switching transistor MP is in the conducting status, here T_{ON} is the conduction time of the switching transistor, and the equivalent circuit of the main circuit in the conducting status is shown in Fig. 2 (b). At this point, the inductive current increases linearly, and the amount of increase is:

$$\Delta I_L(+) = \frac{V_I - V_O}{L} T_{ON} \tag{1}$$

When $T_{ON}< t\leq T$, the power switching transistor MP cuts off, here T_{OFF} is the conduction time of the switching transistor, and the equivalent circuit of the main circuit in the non-conducting status is shown in Fig. 2 (c). At this time, the inductance current decreases linearly. The amount of decrease is:

$$\Delta I_L(-) = \frac{V_O}{L} T_{OFF} \tag{2}$$

In steady state, I_L keeps constant at the end and beginning of each cycle, so:

$$\Delta I_L(+) = \Delta I_L(-) = \frac{V_I - V_O}{L} T_{ON} = \frac{V_O}{L} T_{OFF} \tag{3}$$

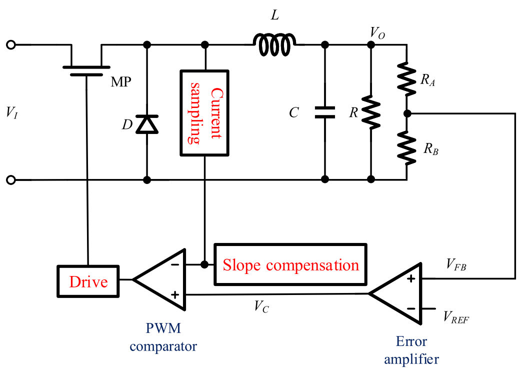

FIGURE 3. Schematic diagram of peak current control mode.

The relationship between output voltage and input voltage and duty ratio can be obtained as follows:

$$D = \frac{V_O}{V_I} \tag{4}$$

B. PEAK CURRENT CONTROL MODE

In general,current control mode includes uniform inductive current control mode and peak inductive current control mode. Due to the complexity of sampling and control circuit of the uniform inductive current control mode, it is seldom used. The peak inductive current control mode is selected in this design [18]. Its principle is shown in Fig. 3. As shown in Fig. 3, the peak current mode is to add a current control loop above the voltage control mode, thus realizing the sampling and control of the output voltage and inductive current. The sample of output voltage V_{FB} is achieved by the resistor divider, then feedback voltage V_{FB} and the reference voltage V_{REF} are compared in the error amplifier, whose output is the error signal V_C. When the current signal obtained by sampling and the compensation signal produced by the slope compensation circuit is summed and compared with V_C in the comparator, the PWM control signal is obtained. The PWM control signal determines the duty ratio of the system and realizes the regulation and stability of the output voltage [18], [19].

C. TRADITIONAL SLOPE COMPENSATION PRINCIPLE

Conventionally, the compensation signal is one-time slope compensation, that means, a slope compensation current with constant slope is added into the current control loop to eliminate the influence of inductance current disturbance. During the CCM peak current control mode, when duty ratio D>50% and without slope compensation, the inner current loop will be unstable, and a disturbance with small inductance current will produce greater disturbance after several cycles. As shown in Fig. 4, the red line represents the inductance current I_L, ΔI_0 represents the disturbance on the inductance current, and the blue line represents the inductance current with the interference I'_L. During the CCM current mode, when a small disturbance ΔI_0 appears in the inductance current, If duty ratio D is less than 50% (D<50%), the inductance

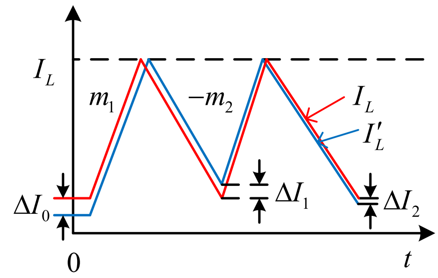

FIGURE 4. Duty ratio D is less than 50%.

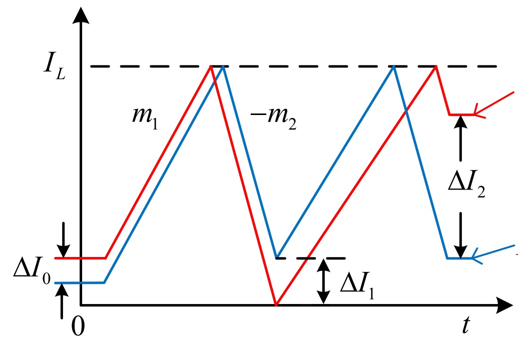

FIGURE 5. Duty ratio D is greater than 50%.

current disturbance ΔI_0 will be attenuated to ΔI_1 in the next cycle and the current will recover to the original value after a number of periods. and the inductance current ΔI_0 disturbance is automatically eliminated [12], [13], [15].

In another case, if the duty ratio D>50%, then the inductance disturbance current ΔI_0 will be increased to ΔI_1 in the next period, and gradually increase in the following cycles exponentially, thereby the system will oscillate. It is assumed that the slope of the increase in inductance current is m_1, the slope of reduction is m_2, and the slope compensation signal slope is K.

$$\frac{\Delta I_1}{\Delta I_0} = \frac{m_2}{m_1} \tag{5}$$

By analogy, through N cycles:

$$\Delta I_N = \Delta I_0 (\frac{m_2}{m_1})^N \tag{6}$$

Because $\frac{m_2}{m_1} = \frac{D}{1-D}$, so:

$$\Delta I_N = \Delta I_0 (\frac{m_2}{m_1})^N = \Delta I_0 (\frac{D}{1-D})^N \tag{7}$$

Equation (7) shows that: when the duty ratio is D< 50%, the fluctuation of the inductance current is weakened in turn, and the system is recovered after N periods. While when considering the case of duty ratio D> 50%, the inductance current disturbance ΔI_0 will be increased continuously, and the system will eventually oscillate [20]. Finally, slope compensation is to add a current with a slope of −K in the inner loop, as shown in Fig. 6. Even if the duty ratio D is larger

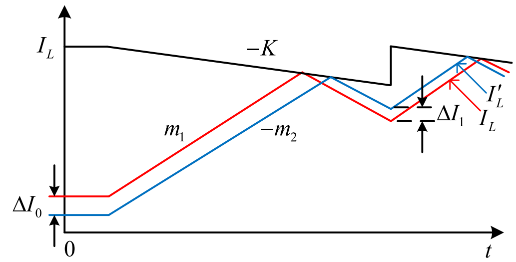

FIGURE 6. Duty ratio D> 50%, adding slope compensation.

than 50%, the inductance current disturbance ΔI_0 will be weakened gradually and recovered to the stability value [21].

$$\Delta I_N = \Delta I_0 (\frac{m_2 - K}{m_1 + K})^N \tag{8}$$

At this point, the system will be stable in the case of $0 < \frac{m_2 - K}{m_1 + K} < 1$. For the Buck DC-DC converter, the inductance current with a slop of $m_1 = (V_{in} - V_{out})/L$ decreases with a slop of $m_2 = V_{out}/L$, resulting the duty ratio of the system $D = V_{out}/V_{in}$. Finally, the slope compensation slope must satisfy:

$$K > \frac{2V_{out} - V_{in}}{2L} \tag{9}$$

As long as the slope compensation slope K satisfies the equation (9), the DC-DC converter system will maintain stability.

Although the traditional slope compensation technique can keep the DC-DC converter stable, overcompensation usually occurs because the compensation slope needs to be smaller than the maximum duty ratio D to keep stability. Overcompensation slows down the chip's transient response and degrades the performance to drive load, so a piecewise linear slope compensation circuit is proposed [20], [21].

In order to avoid excessive compensation, adaptive slope compensation is proposed where the slope of the slope current will change with the duty ratio D, which means different duty ratio corresponds to different compensation slope K, avoiding the generation of overcompensation effectively.

III. ARCHITECTURE DESIGN

According to the principle of switching mode power supply and slope compensation, an adaptive slope compensation circuit is designed for peak current control mode Buck DC-DC converter in Fig. 3. The circuit uses voltage sampling module and current mirror to generate a current which is proportional to the difference between input and output voltage. Once the current charges a capacitor and obtains the slope compensation voltage, the relationship between duty ratio and compensation slope is established, and the slope adaptive regulation is realized. In this section, each important basic sub-block of the circuit is analyzed and designed, including voltage sampling module, pulse generation circuit, etc.

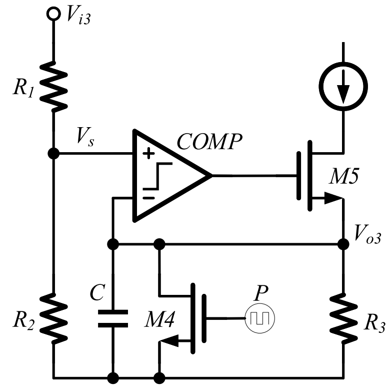

FIGURE 7. Voltage sampling based on comparator.

A. VOLTAGE SAMPLING

According to the theoretical analysis of adaptive slope compensation, it is necessary to sample the input voltage and output voltage as feedback control signal to achieve closed-loop stability so as to stabilize the output voltage. Therefore, the voltage sampling sub-block is an important part of the adaptive slope compensation circuit.

In general, comparators are operational amplifiers operating in open-loop or positive feedback. Fig. 7 shows the voltage sampling technique proposed in this work. The short pulse signal P controls the turn-off of transistor M4. When M4 is turned on, the voltage V_{o3} is set to 0 to ensure that V_{o3} is lower than V_s. The comparator output controls M5. When V_{o3} is lower than V_s, M5 is turned on, and charges the capacitor C. Owing to the delay of the comparator, an overshoot ($V_{o3} > V_s$) occurs. At this time, M5 is turned off and the capacitor is discharged through R_3. Eventually the whole system tends to be stable, that is, $V_{o3} = V_s$. The accuracy of this scheme is very high, and when the input voltage V_{i3} changes, the output voltage V_{o3} changes with the input voltage and can always satisfy $V_{o3} = V_s$ [7].

B. PULSE GENERATION CIRCUIT

Slope compensation waveform is characterized by rising slowly but falling rapidly, that is, most of the time, it has been in a rising status, so a narrow pulse signal is needed to control on and off status of switch, and then control the rising and falling of the slope compensation signal. When the power transistor is just turned on, the voltage at the both plates of the charging capacitor is set to 0. Considering the superposition of the peak detection voltage, the narrow pulse should be generated at the falling edge of the system clock [18], [19].

As shown in Fig. 8, the pulse generation circuit is realized by inverting the system clock after delay, and then doing NOR computing with the original clock to obtain the required narrow pulse. At the same time, the pulse width can be adjusted by adjusting the value of capacitor. The pulse signals with different pulse widths as shown in Fig. 9 can be obtained.

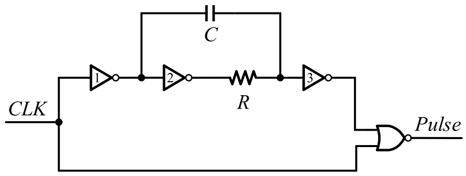

FIGURE 8. Pulse generation circuit.

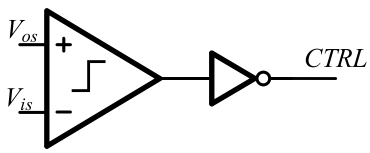

FIGURE 9. CTRL signal generation circuit.

C. DESIGN OF SLOPE CURRENT GENERATION CIRCUIT

In order to maximize the transient response speed and drive load capacity of the system, an adaptive slope compensation circuit slope compensation circuit is designed. As the duty cycle changes, the compensation slope also changes accordingly.

In order to meet the stability and have fast dynamic response time, it is necessary to adjust the slope compensation current dynamically. That is, when the input voltage and output voltage change, an appropriate compensation slope must be generated.

Obviously, the system can remain in stable status as long as equation (9) is satisfied.Thus, the input may be employed in accordance with the change of the output voltage of the different compensation slope, i.e., the duty ratio is small at a small slope compensation may be employed to reduce or eliminate excessive impact compensation.

A slope compensation circuit with self-calibration compensation slope is designed based on standard CMOS technology. The circuit can produce proper slope compensation along with the variation of input and output signals. As shown in Fig. 10, the voltage sampling sub-block 1 is used so that the current of transistor MP2 is determined by the voltage V_1 and the resistor R_3.

$$I_{MP2} = \frac{V_1}{R_3} \tag{10}$$

$$V_1 = V_{os} = \frac{V_{out}R_2}{R_1 + R_2} \tag{11}$$

The cascode current mirror composed of the transistors MP1 and MP2, MP3 and MP4 respectively, width to length ratio of MP3 and MP4 are set to be to A times that of MP1 and MP2 respectively, then the current I_{MP4} is equal to:

$$I_{MP4} = AI_{MP2} = \frac{AV_1}{R_3} \tag{12}$$

Similarly, setting the width to length ratio of MP9 and MP10 to E times that of MP11 and MP12 respectively, the network formed by the voltage sampling sub-block 2, R_4, MP9, MP10, MP11, and MP12 lead the current of I_{MP10} can be expressed as:

$$V_2 = V_{is} = \frac{V_{in}R_6}{R_5 + R_6} \tag{13}$$

MN3 and MN5, MN4 and MN6 constitute current mirror respectively, width to length ratio of MN5 and MN6 are set to be B times that of MN3 and MN4 respectively, then I_{MN5} is:

$$I_{MN5} = BI_{MP4} = \frac{ABV_1}{R_3} \tag{14}$$

Width to length ratio of MP7 and MP8 are set to be D times that of MP5 and MP6 respectively, the current which charge capacitor C_2 is:

$$I_{slope} = DI_{MP6} = D(I_{MN5} - I_{MP10}) = D(\frac{ABV_1}{R_3} - \frac{ABV_1}{R_3}) \tag{15}$$

The voltage across the capacitor is the slope compensation voltage V_{slope}, and the slope of the voltage K is:

$$K = \frac{dV_{slope}}{dt} = \frac{I_{slope}}{C_2} = \frac{D}{C_2}(\frac{ABV_{out}R_2}{R_3(R_1+R_2)} - \frac{EV_{in}R_6}{R_4(R_5+R_6)}) \tag{16}$$

In this design, MN7, MN8 and C_2 constitute a slope compensation circuit. When MN7 or MN8 is turned on, capacitor C_2 voltage is pulled low to zero potential. When MN7 and MN8 are turned off, I_{slope} charges capacitor C2 to generate a slope compensation signal [12], [13], [15], [20], [21].

The slope of slope compensation which satisfies equation (9) can be obtained by setting the width to length ratio of each transistor reasonably. In this design, the parameters of the equation (16) are A = B = D = E = 1. On the other hand, the relationship between short pulse P1 and P2 satisfies: P2 has a slightly wider pulse width than P1, voltage V_1 and V_2 has a period for stability, once V_1 and V_2 have been built completely, then transistor MN8 is turned on to charge the capacitor C_2.

Fig. 4 shows that when duty cycle is less than 50%, the fluctuation of inductance current will gradually decrease to zero. Therefore, when duty cycle is less than 50%, slope compensation current is in sleep mode. Therefore, Ctrl signal is generated as shown in Fig. 9 to control whether the slope current is generated or not. When $V_{os} < V_{is}$, CTRL is high, the control transistor MN7 is turned on, and the V_{slope} is pulled low to zero potential, which ensures no slope compensation is inserted when the duty ratio is small.

IV. SIMULATION RESULTS

A. SUB-BLOCK SIMULATION

According to the theoretical analysis of adaptive slope compensation, it is necessary to sample the input voltage and output voltage as feedback control signal to achieve closed-loop stability. Therefore, the voltage sampling is an important sub-block of the adaptive slope compensation circuit, as shown in Fig. 7. The simulation results of voltage sampling based on comparator are shown in Fig. 11. In Fig. 11, when the input voltage v_s changes from 1.5V to 2.5V, the output voltage v_{o3} will be equal to the input voltage v_s after a short setup time, therefore, voltage sampling has been realized.

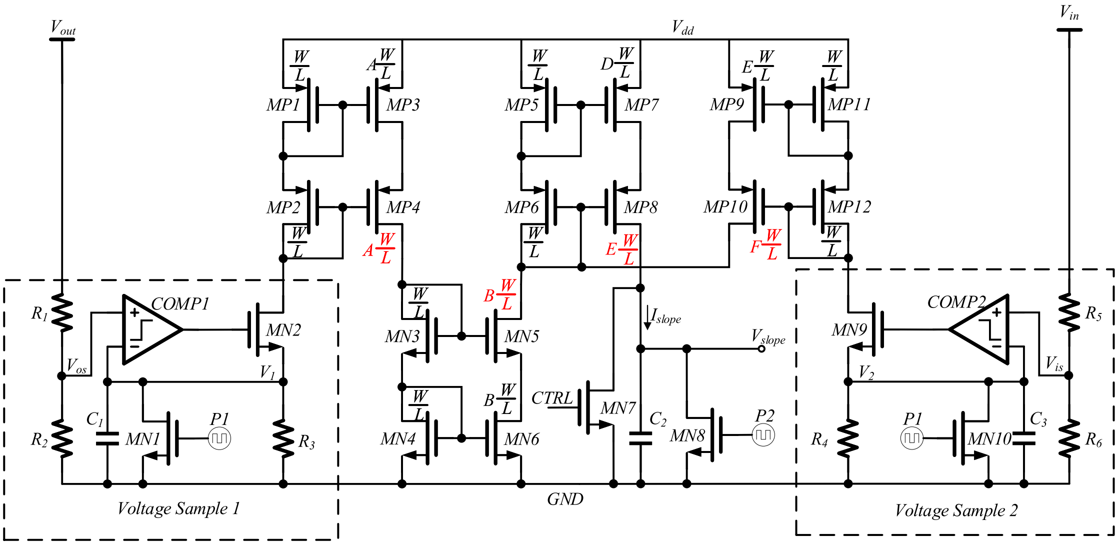

FIGURE 10. The high-precision adaptive slope compensation circuit proposed in this work.

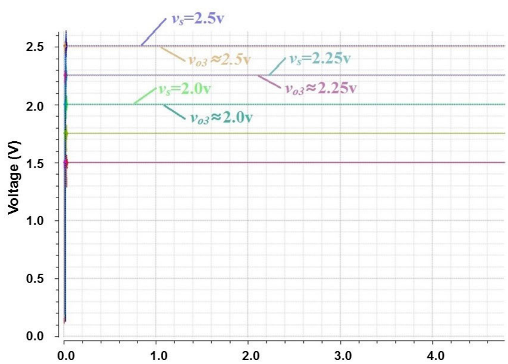

FIGURE 11. Simulation of voltage sampling sub-block.

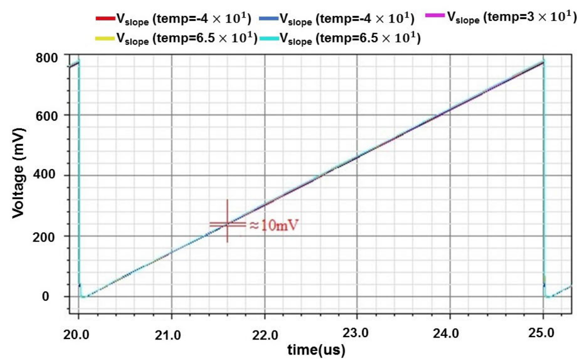

FIGURE 13. Analysis and simulation results at different temperatures.

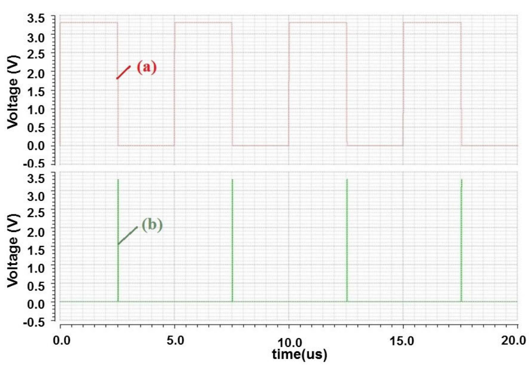

FIGURE 12. Transient response simulation results of pulse generation: (a) CLK (b) Pulse.

In this design, it is necessary to generate a narrow pulse signal to control the switch on and off. Fig. 12 shows the simulation results of the pulse generating circuit in Fig. 8. Fig. 12 shows that the narrow pulse is generated at the falling edge of the system clock, and the duty ratio is small, which can meet the specification of the system design.

Through the above simulation analysis, each sub-blocks of the adaptive slope compensation circuit has achieved the expected performance, and can meet the requirements of the whole system.

B. WHOLE CIRCUIT SIMULATION

When the input voltage is 5V and the output voltage is 4V, the simulation results at tt corner with different temperatures are shown in Fig. 13. When the temperature changes from −40 °C to +100 °C, the peak value of slope compensation fluctuates only about 10mV, the fluctuation of the slope compensation is only about 1% and the accuracy is up to 97%.

Simulation results of 5 corners (ff, fnsp, snfp, ss, tt) are shown in Fig. 14, which show that the fluctuation of the slope compensation is only about 3% and the accuracy is up to 95%.

When the output voltage is fixed and the input voltage changes, the simulation results of slope compensation circuit are shown in Fig. 15. Table 1 and Table 2 conclude the accuracy of the compensation slope. Here, k and Δk(set) represent the compensation slope and the expected change

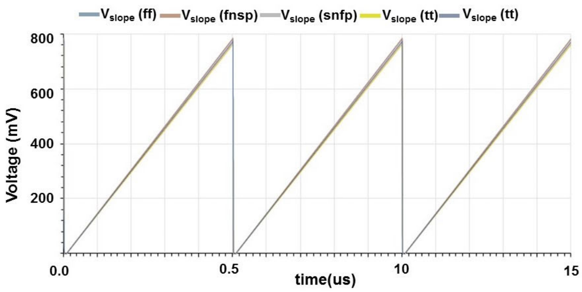

FIGURE 14. Simulation results with different corners.

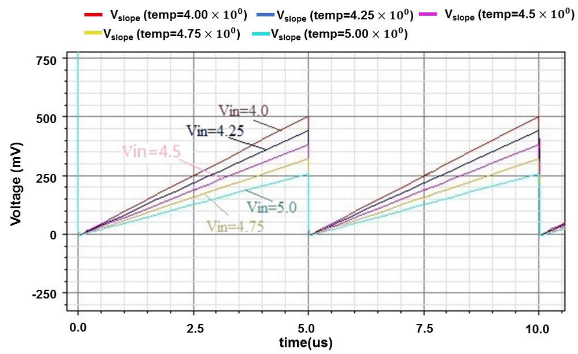

FIGURE 15. Relationship between slope change and input voltage.

TABLE 1. The accuracy of the slope with different V_{in}.

V_{in} (V)	k	Δk	$\Delta(\Delta k)$	$\Delta(\Delta k)/\Delta k(set)$
4	100280	12100	400	3.20%
4.25	88180	12140	360	2.88%
4.5	76040	12160	340	2.72%
4.75	63880	12200	300	2.40%
5	51680	12260	240	1.92%

TABLE 2. The accuracy of the slope with different V_{out}.

V_{out} (V)	k	Δk	$\Delta(\Delta k)$	$\Delta(\Delta k)/\Delta k(set)$
3	51680	25720	720	2.88%
3.25	77400	25720	720	2.88%
3.5	103120	25720	720	2.72%
3.75	128840	25760	760	3.04%
4	154600	25400	400	1.60%

amount, respectively. Δk represents the actual change amount of the slope, and Δ(Δk) represents the difference between the actual change amount and the expected change amount. Finally, Δ(Δk)/Δk(set) is used to indicate the accuracy of the slope compensation. When the input voltage is fixed and the output voltage changes, the simulation results of the slope compensation circuit is shown in Fig. 16. Table 1 concludes and the accuracy of the slope. Table 1 shows that when V_{out} is fixed and the V_{in} is changing between 4∼5 V, the slope compensation accuracy can reach more than 96%. Similarly,

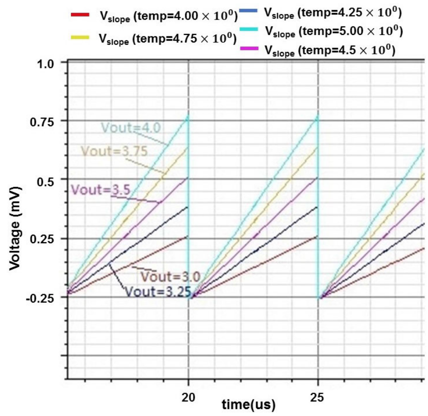

FIGURE 16. Relationship between slope change and output voltage.

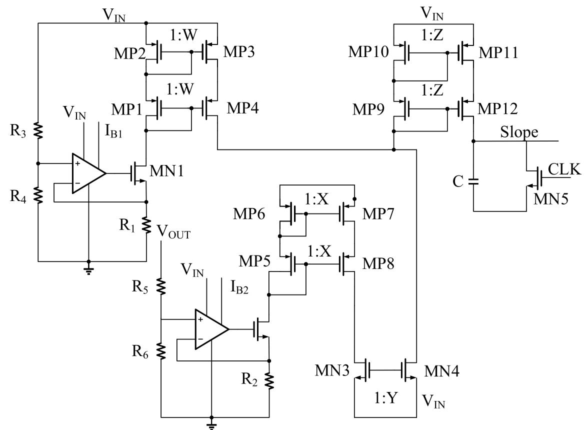

FIGURE 17. Circuit diagram for testing sampling accuracy.

TABLE 3. The accuracy of the slope with different V_{in}.

V_{in} (V)	k	Δk	$\Delta(\Delta k)$	$\Delta(\Delta k)/\Delta k(set)$
2.0	251 300	2 800	100	3.70%
2.5	248 500	2 700	0	0.00%
3.0	245 800	2 700	0	0.00%
3.5	243 100	2 800	100	3.70%
4.0	240 300	2 700	0	0.00%
4.5	237 600	2 600	100	3.70%
5.0	235 000	2 400	300	11.11%

Table 2 shows that when the V_{in} is fixed and the V_{out} is changing between 3∼4V, the accuracy of slope compensation can reach more than 96%.

V. COMPARISON WITH STATE-OF-THE-ART

Fig. 17 shows a self-adaptable slop compensation technique proposed in [22], but the accuracy of the slope compensation signal can only reach about 88%. Table 3 and Table 4 conclude the simulation results of self-adaptable slop compensation technique proposed in [22]. Compared with Table 1 and Table 3, compared with Table 2 and Table 4, it is obvious that

TABLE 4. The accuracy of the slope with different V_{out}.

V_{out} (V)	k	Δk	$\Delta(\Delta k)$	$\Delta(\Delta k)/\Delta k(set)$
4.50	26 700	21 870	4430	16.84%
6.75	48570	23570	2730	10.38%
9.00	72140	24 850	1450	5.51%
11.25	96990	25 710	590	2.24%
13.50	122700	26 300	0	0.00%
15.75	149000	26 600	300	1.14%
18.00	175600	26 100	200	0.76%
20.25	201700	25 200	1100	4.18%
22.50	226900	23 200	3100	11.79%

the accuracy of the circuit design proposed in this paper is higher.

VI. CONCLUSION

Adaptive high-precision slope compensation is often used in DC-DC converter products. In this paper, the important modules of the circuit are analyzed and simulated in this design, the slope compensation signal can be generated adaptively and the accuracy of slope compensation can reach more than 96%, so it can meet the requirements of high precision and high stability of today's wearable devices.

REFERENCES

[1] H. Fan, D. Li, K. Zhang, Y. Cen, Q. Feng, F. Qiao, and H. Heidari, "A 4-channel 12-bit high-voltage radiation-hardened Digital-to-Analog converter for low orbit satellite applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 3698–3706, Nov. 2018.

[2] H. Nakao, Y. Yonezawa, T. Sugawara, Y. Nakashima, and F. Kurokawa, "Online evaluation method of electrolytic capacitor degradation for digitally controlled SMPS failure prediction," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2552–2558, Mar. 2018.

[3] Y. Li, C. Ying, and X. Qianhua, "A small power switching mode power supply based on TOP switch," in *Proc. Int. Joint Conf. Artif. Intell.*, Apr. 2009, pp. 298–300.

[4] J. Wijsman, B. Grundlehner, H. Liu, H. Hermens, and J. Penders, "Towards mental stress detection using wearable physiological sensors," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Aug. 2011, pp. 1798–1801.

[5] O. D. Lara and M. A. Labrador, "A survey on human activity recognition using wearable sensors," *IEEE Commun. Surveys Tuts.*, vol. 15, no. 3, pp. 1192–1209, 3rd Quart., 2013.

[6] Z.-K. Zhou, Y. Shi, C. Gou, X. Wang, G. Wu, J.-F. Feng, Z. Wang, and B. Zhang, "A resistorless low-power voltage reference," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 613–617, Jul. 2016.

[7] S. Ratanapanachote, H. Ju Cha, and P. N. Enjeti, "A digitally controlled switch mode power supply based on matrix converter," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 124–130, Jan. 2006.

[8] S. Seneviratne, Y. Hu, T. Nguyen, G. Lan, S. Khalifa, K. Thilakarathna, M. Hassan, and A. Seneviratne, "A survey of wearable devices and challenges," *IEEE Commun. Surveys Tuts.*, vol. 19, no. 4, pp. 2573–2620, 4th Quart., 2017.

[9] K. Zhang, C. Li, Y. Niu, Y. Yang, and S. Xiao, "A technique for high precision temperature sensor," in *Proc. Int. Symp. Intell. Signal Process. Commun. Syst. (ISPACS)*, Nov. 2017, pp. 680–683.

[10] Y. Shi and H. Li, "Isolated modular multilevel DC–DC converter with DC fault current control capability based on current-fed dual active bridge for MVDC application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2145–2161, Mar. 2018.

[11] S. Sundaramoorthi, K. Karunanithi, S. Saravanan, and S. Praveenkumar, "Investigation and control of chaos in DC-DC noel converter using slope compensation method," in *Proc. IEEE Int. Conf. Intell. Techn. Control, Optim. Signal Process. (INCOS)*, Mar. 2017, pp. 1–5.

[12] F. Tian, S. Kasemsan, and I. Batarseh, "An adaptive slope compensation for the single-stage inverter with peak current-mode control," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2857–2862, Oct. 2011.

[13] Y. Li, W. Hong, F. Cao, Y.-P. Wang, and Y.-R. Wu, "Estimation of terrain slope using a compensation-Lambertian method from single-pass POLSAR data," in *Proc. IEEE Int. Geosci. Remote Sens. Symp. (IGARSS)*, vol. 2, Jul. 2008, pp. II-1310–II-1313.

[14] T. Y. Goh and W. T. Ng, "Single discharge control for single-inductor multiple-output DC–DC buck converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2307–2316, Mar. 2018.

[15] Y. Hu, Y. Wei, J. Wang, and M. Sun, "Design of slope compensation for a high-efficiency high-current DC-DC converter," in *Proc. 13th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Oct. 2016, pp. 1306–1308.

[16] S.-Y. Chen and J.-J. Chen, "Study of the effect and design criteria of the input filter for buck converters with peak current-mode control using a novel system block diagram," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3159–3166, Aug. 2008.

[17] K. Kim, H.-W. Shim, A. C. Scogna, and D.-S. Kim, "SMPS noise modeling and analysis in mobiles at 3-level buck converter-based fast charging mode," in *Proc. Asia–Pacific Int. Symp. Electromagn. Compat. (APEMC)*, Jun. 2017, pp. 232–234.

[18] S. Abe and T. Ninomiya, "Effect of peak current mode control on transient response for VRM application," in *Proc. 5th Int. Power Electron. Motion Control Conf.*, vol. 18, Aug. 2006, pp. 1–5.

[19] Y. Furukawa, S. Nibu, F. Kurokawa, and I. Colak, "Improving stability of switching power supply with digital peak current mode control," in *Proc. IEEE Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Nov. 2016, pp. 952–955.

[20] T. Qian and B. Lehman, "An adaptive ramp compensation scheme to improve stability for DC-DC converters with ripple-based constant on-time control," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Sep. 2014, pp. 3424–3428.

[21] K.-Y.-B. Cheng, F. C. Lee, and P. Mattavelli, "Adaptive ripple-based constant on-time control with internal ramp compensations for buck converters," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2014, pp. 440–446.

[22] Z. Zhou, R. Wang, and B. Zhang, "A self-adaptation slope compensation circuit," *J. Univ. Electron. Sci. Technol. China*, vol. 36, no. 1, pp. 47–49, 2007.

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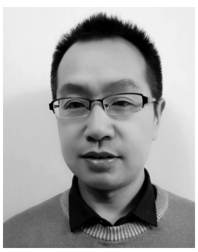

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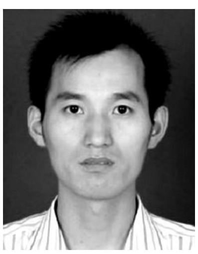

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