

Received January 7, 2020, accepted January 23, 2020, date of publication February 17, 2020, date of current version February 27, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2974514

Compact Switched-Capacitor Power Detector With Frequency Compensation in 65-nm CMOS

CHENYANG LI¹, (Student Member, IEEE), **CHIRN CHYE BOON¹**, (Senior Member, IEEE), **XIANG YI²**, (Senior Member, IEEE), **ZHIPENG LIANG³**, AND **KAITUO YANG¹**, (Student Member, IEEE)

¹VIRTUS Laboratory, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

²Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, USA

³Bantian Huawei Base, Shenzhen 518129, China

Corresponding author: Chirn Chye Boon (eccboon@ntu.edu.sg)

This work was conducted within the Delta-NTU Corporate Lab for Cyber-Physical Systems with funding support from Delta Electronics Inc. and the National Research Foundation (NRF) Singapore under the Corp Lab@University Scheme.

ABSTRACT This work presents a compact switched-capacitor power detector (PD) with frequency compensation technique in a 65-nm CMOS process. Utilizing self-biased MOSFET as switches, the PD works both at the positive and the negative cycle to increase the dynamic range (DR). The output of traditional power detectors usually change with the variations of input frequencies which make the measurement of PD more difficult. In this design, by adding a feed-forward frequency detection circuit, the load resistors of the power detector are changed according to the input frequencies. Thus, the effect of input frequency variation is minimized. The measured operation frequency of the power detector is from 3 GHz to 5 GHz with a dynamic range of 20 dB with an error of ± 2 dB. The variations of the output voltage are reduced from more than 4 dB to ± 0.5 dB, achieving a variation of less than ± 0.25 dB/GHz. To the authors' knowledge, it is the first power detector with input frequency compensation. The core of the power detector occupies an area of 0.014 mm^2 and consumes 2.04 mW static power.

INDEX TERMS CMOS power detector, dynamic range, frequency compensation, self-biased MOSFET.

I. INTRODUCTION

In a radio frequency (RF) integrated circuit (IC) system, power control is essential for the power amplifier to maintain reliable communications and extend battery life in mobile devices. In transmitter systems, the power detector is usually used to adjust transmission power, increasing the capacity and quality of the network. Supporting multi-band is a trend in modern communication systems. However, for different frequency bands, the outputs of PD varies with input frequencies. This variation can be up to several dB, which requires calibration on these frequencies, making the measurement of input powers difficult. To solve this problem, the frequency compensation technique is required. Besides, since modern systems have a large peak-to-average power ratio, this demand the investigation of power detector with wide dynamic range. Also, the power detector should have

a compact size and low power consumption to be integrated into the whole system.

Although the frequency compensation technique in PD is not discussed in the previous works before. Several techniques are introduced to increase the dynamic range (DR) and bandwidth of the PD [1]–[4]. A PD consists of HBTs in cascode configuration with diode connected PMOS transistor load in a SiGe BiCMOS technology is reported in [1]. The cascode configuration is used to provide wide-band input matching independent of input power level. The DR of the PD is improved by implementing diode connected PMOS transistor load to reduce the load impedance for high DC currents. However, the linearity of this PD is not good enough, so the high dynamic range is realized by increasing the error of the detected power. Cascading gain amplifiers and squaring circuits are utilized to achieve wide DR using the power level segmented detection method in [2]. The frequency response is enhanced by gain amplifiers with a cross-coupled NMOS structure. The power level is divided into several segments

The associate editor coordinating the review of this manuscript and approving it for publication was Xiaoguang Leo Liu¹.

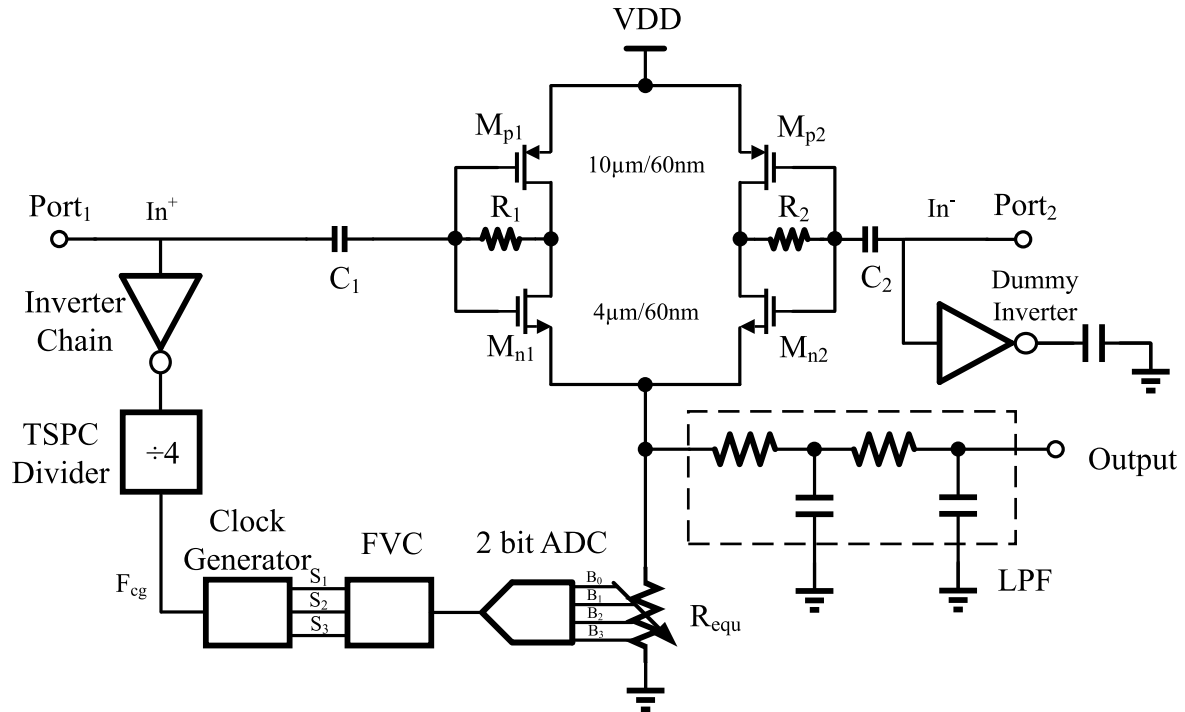


FIGURE 1. Block diagram of the proposed frequency compensated power detector.

and each segment is detected separately. In [3], a capacitor attenuation array and seven stage CMOS rectifiers with auxiliary capacitors are utilized for a wide dynamic range PD. The attenuation capacitors reduce the input signal for rectifiers so the PD can detect input power precisely. Auxiliary capacitors are introduced to improve the DR by making the rectifier maintain the transfer characteristic at the saturation region. However, these circuits are complicated and difficult to be realized. Switched-capacitor balanced diode structure is employed in [4]. It is designed with PN junction diodes working at both positive and negative cycle to increase the linearity. The switched-capacitor structure can reduce the voltage drop across the diodes over the entire period, improving the dynamic range of the PD. Although the DR is increased but the minimum detectable power is too large to be used in wireless communication applications. These reported PDs do not have frequency compensation considerations, so the variations of output voltages can be up to several dB/GHz, making the measurement of input power at different frequencies more difficult.

In this paper, we demonstrated a power detector with reasonable DR and frequency detection circuits to compensate the effect of input frequency variations by changing the load resistances. The PD employs self-biased P-type and N-type MOSFETs as switches and utilized a balanced structure to increase the DR of the PD. The measured DR is 20 dB with a small chip area and 2.04 mW static power. The output voltage variation is within ± 0.5 dB, achieving a variation less than ± 0.25 dB/GHz, which makes this PD more suitable for integrated multi-band RF transmitter systems.

II. DESIGN OF FREQUENCY COMPENSATED POWER DETECTOR

A. DESIGN OF POWER DETECTOR

The proposed power detecting circuit is shown in Fig. 1. It consists of two N-type and two P-type MOSFETs, two input capacitors as DC blockers, two feedback resistors for self-biasing of the MOSFETs, a variant load resistor controlled by digital signals, and a second order RC low-pass filter network to obtain the output DC voltage.

The structure of the proposed power detector is similar to the one published in [4], replacing the diodes used in [4] with self-biased MOSFETs. There are two reasons that the self-biased MOSFET is preferred to diode switch in this design. Firstly, since the PN-junction diode has a higher threshold voltage, the power supply could be much lower using MOSFET switches. This will reduce the power consumption. Secondly, the self-biased MOSFET is more sensitive to small signals compared to the diode. This may be due to the $I_{ds}-V_{gs}$ curve of the MOSFET has a sudden change of slope from the cut-off region to the saturation region when the V_{gs} increases gradually. However, for diode device, the slope of I-V curve changes gradually. Therefore, for the same voltage increase, the MOSFET will conduct more current than the diode.

In this structure, the four MOSFETs work as four switches. With proper supply voltage, the N-type and P-type MOSFETs are just biased below the saturation region. When a positive cycle RF input signal is applied to the $Port_1$, the N-type MOSFET M_{n1} is closed, while the P-type MOSFET M_{p1} is open. At the same time, a negative cycle input signal is applied to the $Port_2$, the P-type MOSFET M_{p2} is closed,

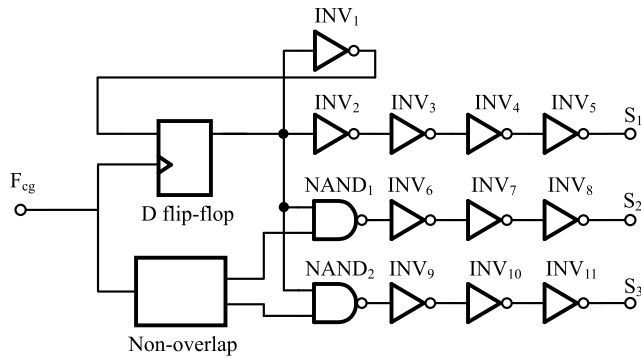


FIGURE 2. Schematic of the clock generator of the proposed power detector.

while the N-type MOSFET M_{n2} is open. The capacitor C_1 is discharged through the load resistance and C_2 is charged by the supply voltage. When a negative cycle input signal is applied to the $Port_1$ and a positive cycle signal is applied to the $Port_2$, switch M_{p1} and M_{n2} are closed, while the switch M_{p2} and M_{n1} are open. Then the capacitor C_1 is charged by the supply voltage and C_2 is discharged through the load resistance. The charging and discharging currents depend on the average voltages applied on terminals of the MOSFETs in one cycle.

B. DESIGN OF FREQUENCY DETECTION CIRCUIT

In the proposed PD, we innovatively compensate the variations of input frequencies by adding a frequency detection circuit. As shown in Fig. 1, the frequency detection circuit is composed of an inverter chain, two true single-phase clock (TSPC) dividers, a clock generator, a frequency-to-voltage converter (FVC) and a 2-bit ADC. The inverter chain is used to amplify the input signal and to convert the input sinusoidal signal to a square wave signal. If the input signal is large, the inverter chain works as a limiter to protect the following stage. Two series TSPC dividers are utilized to divide the input frequency by 4 to generate the clock for the next stage. Dividing the frequency of the input signal by 4 allows the FVC works at higher frequency.

The schematic of the clock generator and FVC are shown in Fig. 2 and Fig. 3. The working principles of these two circuits are similar to the work published in [5]. The clock generator provides three control signals S_1 , S_2 , and S_3 , controlling transistors of M_1 , M_2 , and M_3 as shown in Fig. 3. The input and output signals of the clock generator are presented in Fig. 4. It is composed of a D flip-flop, a non-overlapping circuit, two NANDs, and eleven inverters. The input frequency is divided by two to generate the signal S_1 . With the non-overlapping circuit and NANDs, we can obtain two non-overlapping signals S_2 and S_3 whose frequency is half of the input signal.

These three control signals are with the same frequency. The general operation of the FVC is to charge capacitors C_3 and C_4 by the current mirror when signal S_3 is high. The capacitor C_3 is discharged when signal S_2 is high. The

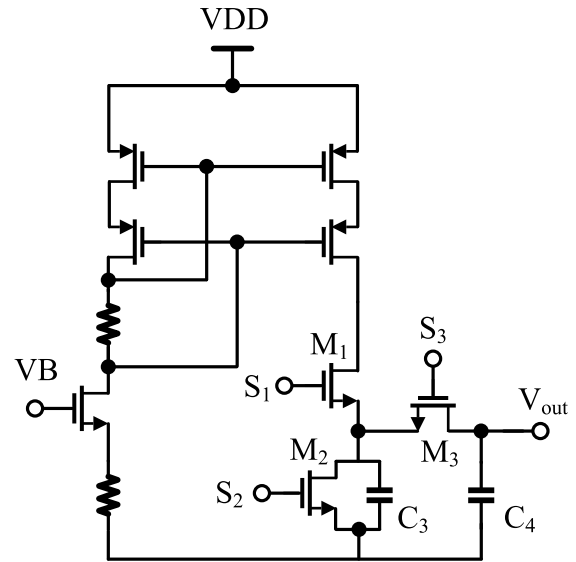


FIGURE 3. Schematic of the FVC of the proposed power detector.

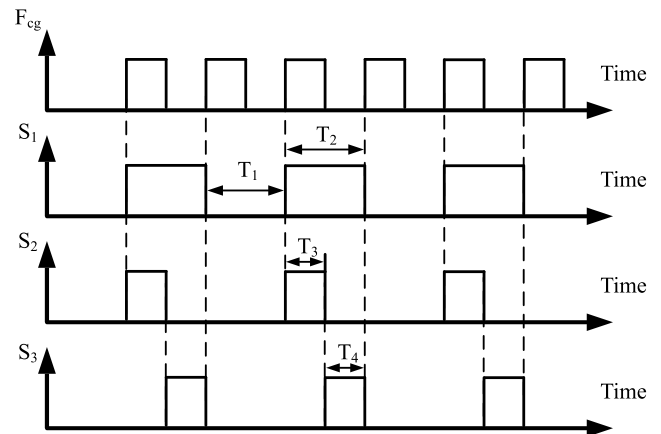


FIGURE 4. Control signals of the clock generator.

charge in C_4 is held constant to provide an output voltage corresponding to the frequency of the control signals. In the negative period T_1 of signal S_1 , all transistors M_1 , M_2 , and M_3 are turned OFF and the charge in C_4 is held constant. During the positive period T_2 of signal S_1 , transistor M_1 is turned ON. In this period, when signal S_2 is at a low voltage level and S_3 is high, capacitors C_3 and C_4 are charged by the current mirror. There is a charge redistribution in capacitors C_3 and C_4 at the beginning of this period when the charge of these two capacitors is not equal. Once the charge of these two capacitors equals, the redistribution procedure stops. When signal S_2 is at a high voltage level and S_3 is low, capacitor C_3 will be discharged and the voltage of C_4 is held constant. Since $C_3 = C_4 = C$. If the input frequency of the PD and the clock generator is f_{in} and f_{cg} , then the frequency of the signal S_3 is $f_{cg}/2 = f_{in}/8$. We have:

$$V_{out} = \frac{I_c}{2C} T_4 = \frac{I_c}{2C} \left(\frac{2}{f_{cg}} \right) = \frac{I_c}{2C} \left(\frac{8}{f_{in}} \right) \quad (1)$$

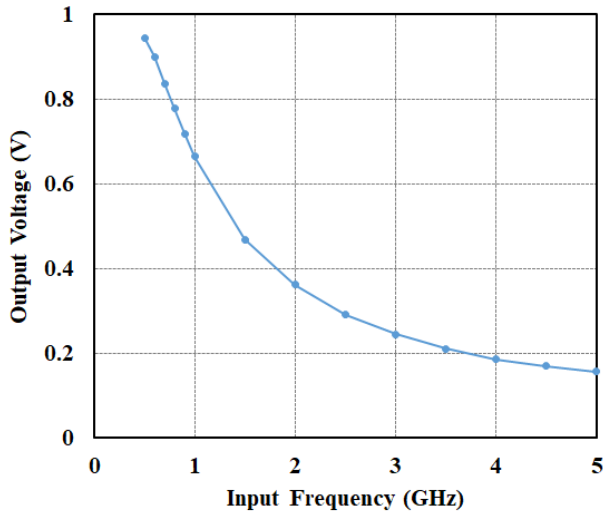


FIGURE 5. Output voltage versus input frequency of FVC.

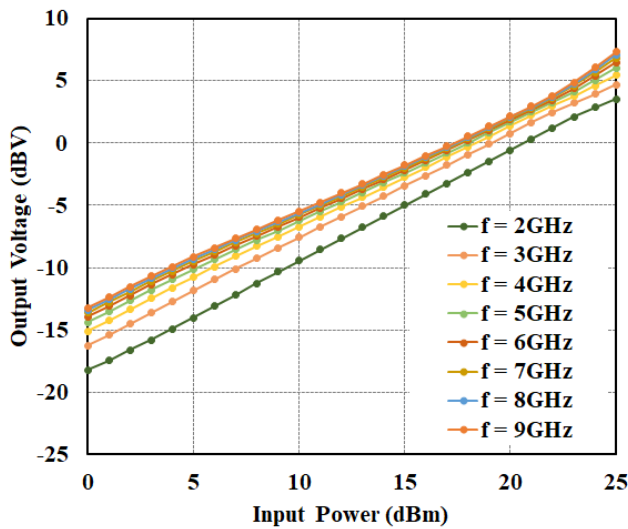


FIGURE 6. Simulation results of output voltages with different input frequencies for uncompensated PD.

So the output voltage of the FVC is reversely proportional to the input frequency. The charging and discharging procedure of this FVC is different from the one published in [5]. In [5], capacitor C_3 is charged firstly and then the charge of C_3 and C_4 are redistributed which makes the whole procedure slower. In the proposed FVC, the redistribution procedure is accelerated by injecting the current of the current mirror at the same time. So the working frequency of this FVC is higher and the time for the FVC to reach a steady state is faster. The output voltage versus input frequency of the FVC is shown in Fig. 5.

To compensate the variation of input frequencies, output voltage versus input power relationship with different input frequencies in an uncompensated PD are shown in Fig. 6. In this figure, simulation results of the PD working at 2 GHz-9 GHz are shown, so a clearer trend of output voltage variation while increasing input frequency can be observed.

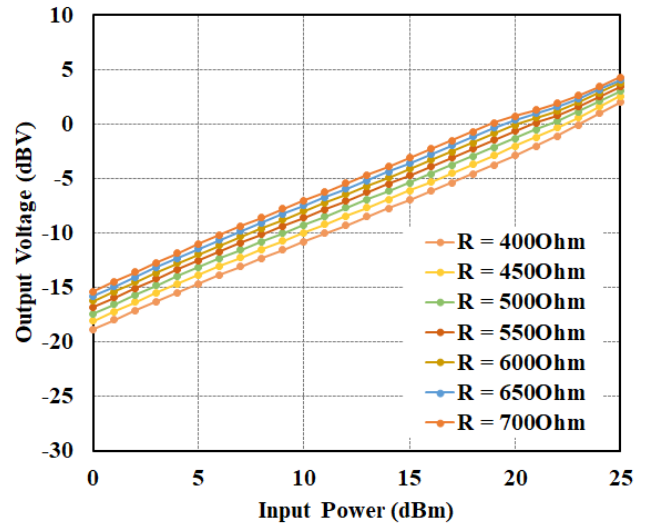


FIGURE 7. Simulation results of output voltages with different load resistances for uncompensated PD.

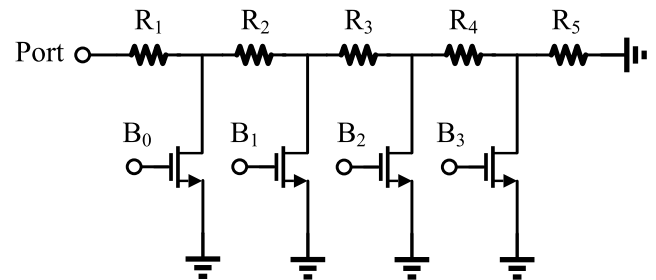


FIGURE 8. Schematic of the load resistor of the proposed power detector.

From the simulated results, we can see that with the increase of input frequency, the output voltages of PD also increase with the same input power. This is because with the frequency of the MOSFET switches turning ON and OFF increased, the charging and discharging frequency also increase, resulting in a higher output voltage. So to eliminate the effect of this charging current increase, we could reduce the load resistance instead. Simulation results for an uncompensated PD are shown in Fig. 7 that with a higher load resistance, the output voltage also increases. If we can reduce the load resistance while increasing the input frequency, the voltage-power curve may remain the same with different input frequencies.

To verify this idea, the output voltage of the FVC is digitized by a 2-bit ADC firstly in this design. For simplicity, the structure of the ADC is a basic flash ADC using a resistor-constructed voltage ladder and comparators. The resistors in the ADC are tuned to not to be linear for the best performance. The output digital signals control the switches to short resistors as shown in Fig. 8. With higher frequency, more resistors are shorted to ground, reducing the load resistance of the power detector. The resolution of the ADC can be increased if higher accuracy is needed. With proper load resistance, we can obtain the same performance of the PD for different input frequencies. In this PD, the load resistance is designed

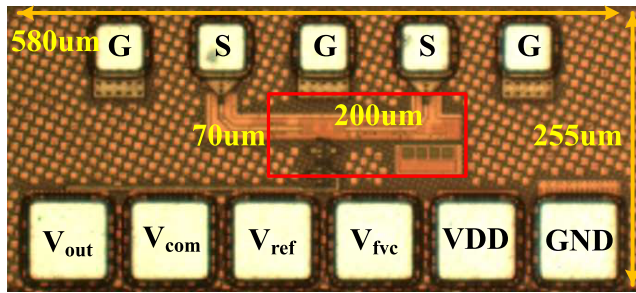


FIGURE 9. Micrograph of the proposed power detector.

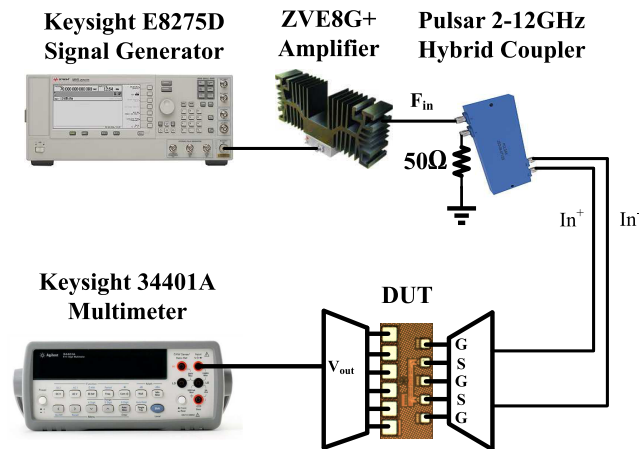


FIGURE 10. Measurement setup of the proposed power detector.

to be 800 Ω, 600 Ω, 550 Ω, 500 Ω, and 450 Ω for 2 GHz, 3 GHz, 4 GHz, 5 GHz, and 6 GHz respectively.

III. MEASUREMENT RESULTS

The proposed frequency compensated power detector has been designed and fabricated in GlobalFoundries 65-nm CMOS process. Fig. 9 shows the micrograph of the fabricated chip. The chip area is 580 µm × 255 µm including the pads for measurement. The area of the power detector is only 200 µm × 70 µm. With a 1.2 V supply voltage, the current consumption of the switched-capacitor power detector is 1.7 mA. Cascade Elite 300 probe station is used to measure the power detector as shown in Fig. 10. Keysight E8257D signal generator providing continuous-wave (CW) signal is first connected to an amplifier and a hybrid coupler to convert to the single-ended signal to the differential. Then differential signals are applied to the input of the power detector. To de-embed the effect of the amplifier and coupler, before the measurement of the PD, the gain of the amplifier and the loss of the hybrid coupler and coaxial cables are measured at target frequencies. So after measurement of the PD, the actual input power of the PD can be calculated to obtain accurate measurement results. The losses of the RF probes are also de-embedded using the S-parameters provided by Cascade. Keysight 34401A multimeter is used to measure the output voltage of the PD.

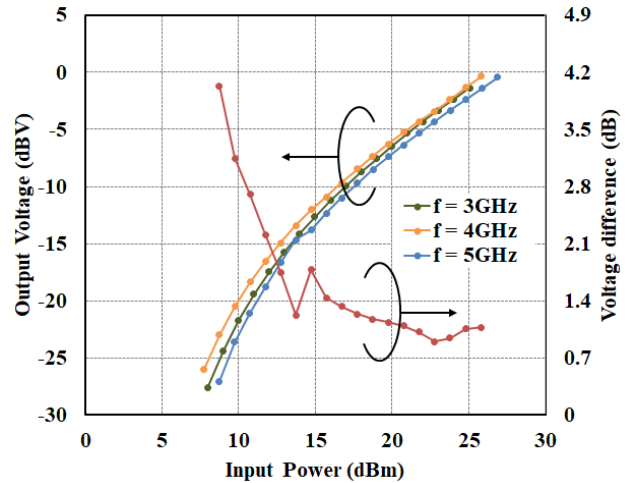


FIGURE 11. Measured performance of the PD without frequency compensation.

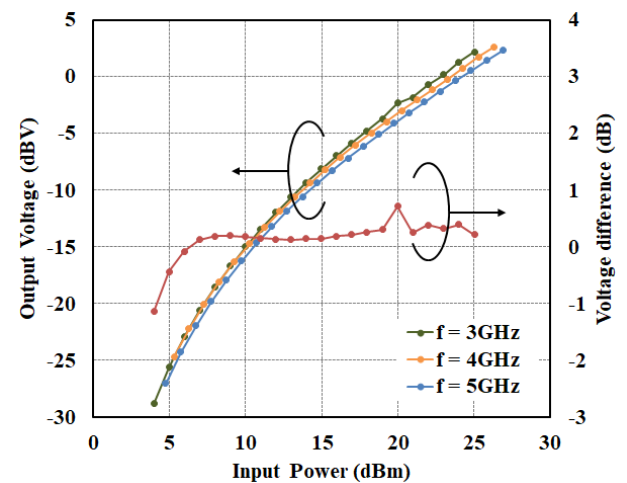


FIGURE 12. Measured performance of the PD with frequency compensation.

In this design, since the resolution of ADC is only 2-bit, five different load resistance values can be obtained by changing the output voltage of the FVC. In the measurement results, two of the five load resistances didn't compensate input frequency well. Therefore, only three frequency points which are well compensated are shown in these figures. Fig. 11 and Fig. 12 show the output voltages and maximum voltage difference versus input power at different frequencies with and without frequency compensation. The maximum voltage difference is calculated by the output voltage difference of PD in a frequency range from 3 GHz to 5 GHz at the same input power. It is shown that the with the frequency compensation circuit, the PD output voltage is more consistent at various input frequencies. However, with the frequency compensation circuit, the lowest detectable power is increased, and the dynamic range is also decreased. We think the possible reason maybe is the increased parasitic and the loading effect of the frequency compensation circuit. The proposed frequency compensated power detector has

TABLE 1. Comparisons with previous power detectors.

Reference	Frequency Compensation	Variation of Output Voltage (dB/GHz)	Dynamic Range (dB)	Operating Frequency (GHz)	Power Consumption (mW)	Active Area (mm ²)	Process
[1]	NO	-	52	7-20	7.2	0.42	250-nm BiCMOS
[2]	NO	-	>40	0.7-4	5.8	0.15	28-nm CMOS
[3]	NO	-	42	0.3-10	0.55	0.113	180-nm CMOS
[4]	NO	<1.5 ^a	>30	4-6	0.7	0.0036	65-nm CMOS
[6]	NO	-	43	2-14	35.2	1.75	130-nm CMOS
[7]	NO	-	40	0-20	-	0.385	180-nm BiCMOS
[8]	NO	-	29	1.8	16	0.48	180-nm CMOS
[9]	NO	-	40	0.9-8	70	0.98	180-nm CMOS
[10]	NO	-	21	0.5-20	0.12	0.085	130-nm CMOS
[11]	NO	-	20	0.125-8.5	0.18	0.0126	130-nm CMOS
[12]	NO	-	20	3.1-10.6	3.8	0.36	180-nm CMOS
This work	YES	<0.25	20	3-5	2.04	0.014	65-nm CMOS

^aEstimated from measurement results.

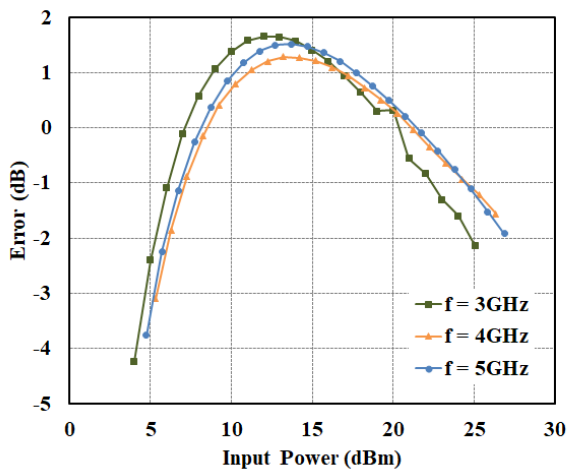


FIGURE 13. Measured error of the PD with frequency compensation.

an operating frequency range from 3 GHz to 5 GHz. The variations of the output voltage are reduced from more than 4 dB to ± 0.5 dB. The measurement results indicate that the power detector has more than 20 dB dynamic range. The error of the frequency compensated PD is within ± 2 dB as shown in Fig. 13. Compared with previous published PDs (Table 1), this PD features at frequency compensation technique with low power consumption, a compact area, and a reasonable DR.

IV. CONCLUSION

In this work, we have verified the idea of the input frequency can be compensated by changing the load resistance of the PD by designing an input frequency compensated, low power consumption, reasonable DR power detector with an area of 0.014 mm² in a 65-nm CMOS process. The measurement results show that with a static power consumption of 2.04 mW, the dynamic range is more than 20 dB in the frequency range of 3-5 GHz. Applying frequency detection circuits, the variations of the output

voltage are reduced from more than 4 dB to ± 0.5 dB, achieving a variation less than ± 0.25 dB/GHz. With low power consumption, small area, and input frequency compensation technique, the proposed power detector is suitable for multi-standard wireless communication on-chip applications.

REFERENCES

- [1] E. Ozeren, I. Kalyoncu, B. Ustundag, B. Cetindogan, H. Kayahan, M. Kaynak, and Y. Gurbuz, "A high dynamic range power detector at X-band," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 9, pp. 708–710, Sep. 2016.
- [2] J. Choi, J. Lee, Y. Xi, S.-S. Myoung, S. Baek, D. H. Kwon, Q.-D. Bui, J. Lee, D. Oh, and T. B. Cho, "Wide dynamic-range CMOS RMS power detector," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 868–880, Mar. 2016.
- [3] J. Wang, Y. Zheng, F. Yang, F. Tian, and H. Liao, "A wide band CMOS radio frequency RMS power detector with 42-dB dynamic range," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 1678–1681.
- [4] C. Li, X. Yi, C. C. Boon, and K. Yang, "A 34-dB dynamic range 0.7-mW compact switched-capacitor power detector in 65-nm CMOS," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9365–9368, Oct. 2019.
- [5] A. Djemouai, M. Sawan, and M. Slamani, "High performance integrated CMOS frequency-to-voltage converter," in *Proc. 10th Int. Conf. Microelectron.*, Nov. 2002, pp. 63–66.
- [6] K. Kim and Y. Kwon, "A broadband logarithmic power detector in 0.13- μ m CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 9, pp. 498–500, Sep. 2013.
- [7] T. Zhang, W. R. Eisenstadt, R. M. Fox, and Q. Yin, "Bipolar microwave RMS power detectors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2188–2192, Sep. 2006.
- [8] M.-L. Shieh, W.-J. Lai, J.-S. Li, Y.-L. Chiang, H.-H. Wu, C.-C. Xsieh, C.-H. Tu, S.-W. Chen, and J.-W. Wu, "Linear radio frequency power detector," in *Proc. Asia Pacific Microw. Conf.*, Dec. 2009, pp. 2316–2319.
- [9] J.-W. Wu, K.-C. Hsu, W.-J. Lai, C.-H. To, S.-W. Chen, C.-W. Tang, and Y.-Z. Juang, "A linear-in-dB radio-frequency power detector," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.
- [10] C. Li, F. Gong, and P. Wang, "A low-power ultrawideband CMOS power detector with an embedded amplifier," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 12, pp. 3270–3278, Dec. 2010.
- [11] Y. Zhou and M. Y.-W. Chia, "A low-power ultra-wideband CMOS true RMS power detector," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 5, pp. 1052–1058, May 2008.
- [12] K. A. Townsend and J. W. Haslett, "A wideband power detection system optimized for the UWB spectrum," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 371–381, Feb. 2009.



CHENYANG LI (Student Member, IEEE) received the B.Eng. and M.Eng. degrees in electronic science and technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with Nanyang Technological University, Singapore.

His research interest is high-linear power amplifier design for Wi-Fi systems.



XIANG YI (Senior Member, IEEE) received the B.E. degree from the Huazhong University of Science and Technology (HUST), in 2006, the M.S. degree from the South China University of Technology (SCUT), in 2009, and the Ph.D. degree from Nanyang Technological University (NTU), in 2014.

He was a Research Fellow with NTU, from 2014 to 2017. He is currently working as a Postdoctoral Fellow at the Massachusetts Institute of Technology (MIT). His research interests include radio frequency (RF), millimetre-wave (mm-wave), and terahertz (THz) frequency synthesizers and transceiver systems. He was a recipient of the IEEE ISSCC Silkroad Award and the SSCS Travel Grant Award, in 2013. He is the Technical Reviewer of several IEEE journals and conferences.



CHIRN CHYE BOON (Senior Member, IEEE) received the B.E. degree (Hons.) in electronics and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was with Advanced RFIC, where he worked as a Senior Engineer. Since 2005, he has been with NTU, where he is currently an Associate Professor. He specializes in the areas of radio frequency (RF) and MM-wave circuits design for communications applications. He has conceptualized, designed, and silicon-verified many circuits/chips resulting in over 150 refereed publications and 15 patents in the fields of RF and MM-wave. He is the coauthor of *Design of CMOS RF Integrated Circuits and Systems* and *CMOS Millimeter-Wave Integrated Circuits for Next Generation Wireless Communication Systems* (World Scientific Publishing). He serves as a Committee Member for various conferences. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is the Golden Reviewer of the IEEE ELECTRON DEVICE LETTERS. He has been the Program Director of RF and MM-wave research of S\$50 million in the VIRTUS Laboratory, Research Centre of Excellence, NTU, since March 2010. He is the Principal Investigator for research grants of over S\$13 million. He is also one of the key NTU-team members of MIT-NTU joint collaboration project Low Energy Electronic Systems, which has won the Singapore-MIT Alliance for Research and Technology (SMART) International Research Grant (IRG) proposal with a grant total of S\$25 million. He is the Winner of the Year-2 Teaching Excellence Award and Commendation Award for Excellent Teaching Performance, EEE, NTU.



ZHIPENG LIANG received the B.E. degree in electrical engineering from Sun Yat-sen University (SYSU), Guangzhou, China, in 2013, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2018. He is currently an Integrated Circuit Designer with Huawei, China. His research interest includes RF integrated circuit designs for wireless applications.



KAITUO YANG (Student Member, IEEE) received the B.S. and M.S. degrees (Hons.) from the School of Information Science and Technology, University of Science and Technology of China (USTC), in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree with Nanyang Technological University (NTU), Singapore.

He was a Researcher with the VIRTUS Laboratory, NTU, Singapore, from 2014 to 2019. His research interests include analog and RF integrated circuits and systems for wireless communications. He holds several patents in the field of RF-CMOS designs.

...