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A Combined DPWM Based on DSOGI-FLL for Switching-Loss Reduction and Dead-Time Compensation

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ABSTRACT High efficiency and high output power quality of converters are always two goals pursued in power electronic systems. In this paper, the conventional discontinuous pulse width modulation (DPWM) for switching-loss reduction and a modified time-based dead-time compensation for reducing output current harmonics are investigated. And a combined DPWM for switching-loss reduction and dead-time compensation is proposed, where the amplitude adjustment and the zero-sequence injection in modulation waves are carried out separately in different current intervals related to polarities of three-phase currents. Moreover, in order to detect accurate polarities of the three-phase currents with ripples and harmonics, the second-order generalized integrator frequency-locked loop (DSOGI-FLL) is adopted and inserted into the combined DPWM. Finally, a combined DPWM based on DSOGI-FLL is proposed for switching-loss reduction and dead-time compensation. The comparison of experimental results with several PWM schemes verifies that, the proposed PWM scheme can both effectively reduce the switching loss and compensate the dead-time, simultaneously enhancing the efficiency and the output power quality of the converter.

INDEX TERMS Dead-time, discontinuous pulse width modulation (DPWM), second-order generalized integrator frequency-locked loop (DSOGI-FLL), switching loss.

I. INTRODUCTION

Three-phase two-level voltage-source converters for the AC/DC power conversion have been widely adopted in systems of renewable power generation, electrical drive, active power filter, and uninterruptible power supply, etc. Improving the efficiency and the power quality of converters are two important goals which have always been pursued in the field of power electronics [1]–[3].

The loss of switching devices is a major factor affecting the converter efficiency, which is composed of the conduction loss and the switching loss [4]–[6]. The conduction loss can be influenced by factors such as voltage drops of devices, current amplitudes, and modulation schemes. The switching loss is related to the switching characteristics of devices, DC-link voltages, current amplitudes, modulation schemes, etc. The modification of modulation schemes has little influence on the conduction loss, but it can significantly

reduce the switching loss [6]. With the discontinuous pulse width modulation (DPWM) [7]–[9], the switching devices in each phase will not operate in 1/3 fundamental period, so the switching losses can be effectively reduced with improved converter efficiency. If devices do not switch exactly in the interval where the absolute value of current is maximum, a DPWM with minimum switching loss can be achieved. In [7], the conduction and switching losses with sinusoidal PWM (SPWM), space vector PWM (SVPWM), and DPWM are compared, presenting the advantages of DPWM on the loss reduction. [8] and [9] present the generalized analytical expression for modulation waves of the carrier-based DPWM. Several DPWM schemes are proposed in [10] for two-level voltage-source converters with balanced two-phase loads to reduce switching losses and current ripples.

Due to the superiority in switching-loss reduction, the DPWM has been extended for various applications. A carrier-based-DPWM for the Vienna rectifier is presented in [11], where a varying clamped area is adopted to reduce the clamped area around zero-crossing and reduce the distortion

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of output currents. A generalized DPWM for active power filters is proposed in [12] based on the detection of the current vector position, to decide the optimum clamped duration for the switching-loss reduction. In [13], the DPWM is adopted in paralleled interleaved three-phase two-level voltage-source converters, where the control of the common-mode circulating current is investigated. The DPWM is applied to a back-to-back converter in [14], and an improved offset selection method is presented to reduce the dc-link capacitor-current ripple. In [15], a DPWM with improved pulse sequence is proposed for the neutral point clamped three-level inverter, to reduce the switching loss and control the neutral point voltage simultaneously.

Through the optimization of modulation schemes, the switching loss can be reduced and the converter efficiency can therefore be improved. At the same time, the output power quality of the converter should not be ignored either. Among the factors affecting the power quality, the dead-time effect can generate quantities of low-frequency harmonics in the output current [16], [17], which should be also well addressed.

Since the voltage error generated by dead-time is related to the output-current polarity, most of the dead-time compensation schemes are implemented according to the current-polarity detection. The basic and original scheme for eliminating the dead-time effect is the time-based dead-time compensation [16], where the time error caused by the dead-time is compensated separately in each phase. Besides, numerous dead-time compensation schemes have also been investigated. In [17], a steady-state dead-time compensation is proposed, where the error between the real current and the reference one is used to determine the voltage error and the suitable time shift for the switching pattern within each sampling interval. A vector-based dead-time compensation is proposed in [18], and a dead-time error voltage vector is introduced to adjust the reference voltage vector depending on the load current polarity. In [19], the current ripple analysis in three-phase PWM converters is conducted to estimate the turn-off current, and a voltage error compensating method based on the turn-off transition is proposed. In [20], taking real-time current ripple into consideration, a dead-time compensation based on the current ripple prediction is proposed. [21] investigates the impact of undercompensation and overcompensation of dead-time effect on the small-signal stability of induction motor drives. In addition, the closed-loop control with the proportional resonant regulator [22], the repetitive controller [23], and the adaptive controller [24] can also be used for compensating the dead-time effect.

This paper aims to improve both the efficiency and the output power quality of the converter, therefore the conventional DPWM for switching-loss reduction [7] and the conventional time-based dead-time compensation [16], both related to current polarities, are selected. And the combination of the two schemes is investigated. Through the analysis, the zero-sequence component injection in the DPWM for switching-loss reduction is carried out in different current

intervals, which are judged from the polarities of three-phase currents. In order to simplify the calculation and facilitate the combination with the DPWM, the conventional time-based dead-time compensation is modified to be implemented also in different current intervals. Through the modification, a combined DPWM for switching-loss reduction and dead-time compensation is proposed.

Accurate current intervals are essential for implementing the combined DPWM. However, since quantities of ripples and harmonics exist in three-phase output currents, it is challenging to accurately detect current polarities around zero-crossings. Thanks to the characteristics of filtering and frequency adaptability of the second-order generalized integrator frequency-locked loop (DSOGI-FLL) [25]–[27], fundamental components without phase shift can be extracted from three-phase currents. Therefore, this paper proposes a combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation. Accurate current polarities are obtained from the extracted fundamental components by DSOGI-FLL, which are further used for judging current intervals. The amplitude adjustment and the zero-sequence injection are separately carried out to implement the combined DPWM for switching-loss reduction and dead-time compensation.

The contribution of this paper lies in the proposed combined DPWM based on DSOGI-FLL, which can achieve both switching-loss reduction and dead-time compensation. The conventional time-based dead-time compensation is modified to be implemented in different current intervals, to facilitate and simplify the combination with the conventional DPWM for switching-loss reduction. DSOGI-FLL is inserted into the combined DPWM to extract accurate current polarities for judging different current intervals, where the amplitude adjustment and the zero-sequence injection of the combined DPWM are separately carried out. With the combined DPWM based on DSOGI-FLL, the efficiency and the output power quality are simultaneously enhanced in converters.

The remaining part of this paper is structured as follows. In Section II, the modulation mechanism of the conventional DPWM for switching-loss reduction is investigated. In Section III, the conventional time-based dead-time compensation is analyzed and a modified time-based dead-time compensation is presented to facilitate the combination with the conventional DPWM. Section IV presents the combination of the conventional DPWM and the modified dead-time compensation. And in Section V, the combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation is proposed. Finally, experimental results with different PWM schemes are presented and compared in Section VI.

II. MODULATION MECHANISM OF THE DPWM FOR SWITCHING-LOSS REDUCTION

The power circuit of three-phase two-level voltage converters is shown in Fig. 1, where V_{dc} and C_{dc} are the DC-link voltage and capacitance; Q_x^+ and Q_x^- ($x = a, b, c$) are the upper and

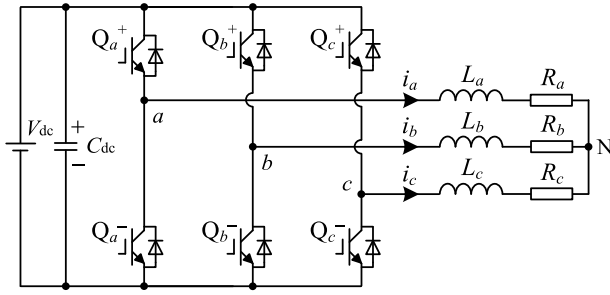


FIGURE 1. Power circuit of three-phase two-level converters.

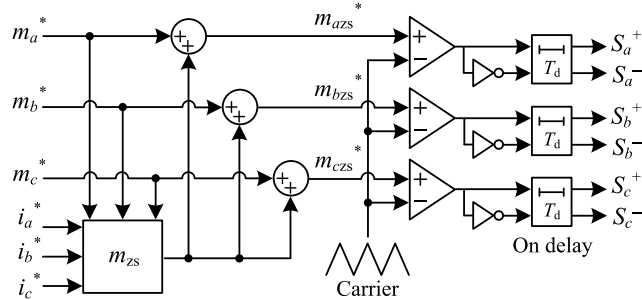


FIGURE 2. Diagram of the DPWM for switching-loss reduction.

lower switching devices in the same bridge; L_x and R_x are the three-phase load inductance and resistance; i_x is the output current of the converter. The AC/DC power transformation is implemented through the modulation scheme which controls the ON/OFF state of six switching devices.

The conventional DPWM for switching-loss reduction is shown in Fig. 2. Firstly, the zero-sequence component m_{zs} is derived according to three-phase original modulation waves m_a^* , m_b^* , m_c^* and reference currents i_a^* , i_b^* , i_c^* . Then, m_{zs} is superimposed with m_a^* , m_b^* , m_c^* forming the final modulation waves m_{azs}^* , m_{bzs}^* , m_{czs}^* . Further, m_{azs}^* , m_{bzs}^* , m_{czs}^* are compared with the triangular carrier and logically inverted generating six signals. Finally, the dead-time T_d is added through the “on delay” term to generate the final drive pulses S_x^+ and S_x^- , thus controlling the ON/OFF state of Q_x^+ and Q_x^- .

The most important step in the DPWM for switching-loss reduction is the calculation of the zero-sequence component m_{zs} , which can be expressed as [28]

$$m_{zs} = -[(1 - 2k_0) + k_0 \cdot m_{\max}^* + (1 - k_0) \cdot m_{\min}^*] \quad (1)$$

where m_{\max}^* and m_{\min}^* are the maximum and minimum values of three-phase original modulation waves m_a^* , m_b^* , m_c^* , respectively; k_0 is an adjustment coefficient. After three-phase modulation waves are superimposed with the zero-sequence component, in each phase there is a $\pi/3$ interval where the amplitude of modulation wave equals to that of the carrier. And the switching devices will not switch in the $\pi/3$ interval, so that the switching loss can be effectively reduced.

The switching loss E_{switch} of the converter can be expressed by a quadratic polynomial equation which is given by [6]

$$E_{\text{switch}} = (A_0 + B_0 \cdot |i_x| + C_0 \cdot |i_x|^2) \quad (2)$$

where A_0 , B_0 , and C_0 are coefficients, $B_0 > 0$ and $C_0 > 0$.

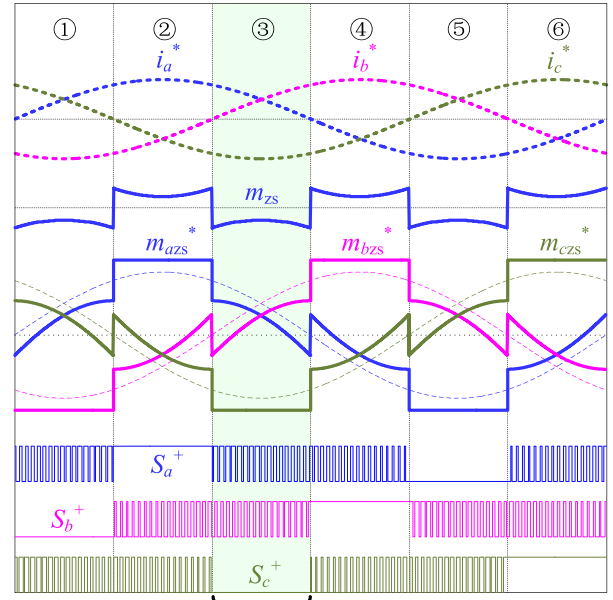


FIGURE 3. Modulation waves and drive pulses of DPWM for switching-loss reduction.

FIGURE 3. Modulation waves and drive pulses of DPWM for switching-loss reduction.

As seen in (2), the switching loss has a positive correlation with the absolute value of the output current $|i_x|$. According to this feature, the position of the superimposed zero-sequence component can be adjusted according to the current, making the device not switch in the $\pi/3$ interval with the largest absolute value of current. Therefore, the minimum switching loss can be achieved. At this time, the adjustment coefficient k_0 can be expressed as

$$k_0 = \begin{cases} 1 & (J > 0) \\ 0 & (J < 0) \end{cases} \quad (3)$$

where J is the sum of the maximum and the minimum values of three-phase reference currents i_a^* , i_b^* , i_c^* , and the expression of J can be given by

$$J = \max(i_a^*, i_b^*, i_c^*) + \min(i_a^*, i_b^*, i_c^*). \quad (4)$$

Based on the above rule of superimposing the zero-sequence component according to the current, modulation waves and drive pulses of the DPWM for switching-loss reduction are shown in Fig. 3. As seen, six intervals ① ~ ⑥ are divided according to polarities of reference currents i_a^* , i_b^* , i_c^* . The current interval, the adjustment coefficient, and the zero-sequence component in the DPWM for switching-loss reduction are summarized in Table 1, where the adjustment coefficient k_0 is derived according to (3) and (4), and the zero-sequence component m_{zs} is calculated according to (1) with the derived k_0 .

As seen in Fig. 3, in each interval, only the absolute value of one phase current remains the largest. The adjustment coefficient k_0 and the zero-sequence component m_{zs} are calculated in each interval, respectively. And the final modulation waves

TABLE 1. Current interval, adjustment coefficient, and zero-sequence component in DPWM for switching-loss reduction.

Current interval	Polarity (i_a^*, i_b^*, i_c^*)	k_0	m_{zs}
①	+ - +	0	$m_{zs} = -1 - m_{\min}^*$
②	+ - -	1	$m_{zs} = 1 - m_{\max}^*$
③	+ + -	0	$m_{zs} = -1 - m_{\min}^*$
④	- + -	1	$m_{zs} = 1 - m_{\max}^*$
⑤	- + +	0	$m_{zs} = -1 - m_{\min}^*$
⑥	- - +	1	$m_{zs} = 1 - m_{\max}^*$

of $m_{azs}^*, m_{bz}^*, m_{cz}^*$ are obtained by superimposing the original modulation waves with the zero-sequence component. In each $\pi/3$ interval, there is one modulation wave, whose amplitude is the same with that of the carrier. And the corresponding drive pulse maintains at high or low level to disable the switching device, achieving the minimum switching loss of the converter. For example, in the ③ interval marked in Fig. 3, $|i_c^*|$ is the largest, after superimposing with m_{zs} , the value of m_{cz}^* equals to the negative amplitude of carrier. Consequently, S_c^+ remains at low level (S_c^- at high level). Q_c^+ and Q_c^- will not switch. Therefore, in the ③ interval, there is no switching loss in the Phase C bridge.

III. CONVENTIONAL TIME-BASED DEAD-TIME COMPENSATION AND ITS MODIFICATION

A. ANALYSIS OF THE CONVENTIONAL TIME-BASED DEAD-TIME COMPENSATION

The “on delay” term in Fig. 2 can generate the dead-time between S_x^+ and S_x^- to prevent the shoot-through failure of the converter. However, output voltage errors related to the current polarity will be generated. When the output current $i_a > 0$, a negative voltage-error pulse with the width of T_d will be generated through the current freewheeling during dead-time, and a positive voltage-error pulse will be generated when $i_a < 0$ [16], [17]. The voltage-error pulses will cause quantities of low-frequency output current harmonics and reduce the DC-link voltage utilization.

Fig. 4 presents a conventional time-based dead-time compensation in one switching period ($i_a > 0$, flowing out of the converter). To compensate the negative voltage-error pulse caused by dead-time ($i_a > 0$), the amplitude of modulation wave m_a^* is increased by m_{dt} . Consequently, the falling edge of the upper drive signal S_a^+ is delayed by $T_d/2$, and its rising edge is advanced by $T_d/2$. At the same time, the rising edge and the falling edge of the lower drive pulse S_a^- is delayed and advanced by $T_d/2$, respectively. As a result, the positive pulse width of the output voltage v_a is extended by T_d , thereby the negative voltage-error pulse is effectively compensated.

Based on properties of similar triangles in Fig. 4, the increase amplitude of the modulation wave can be

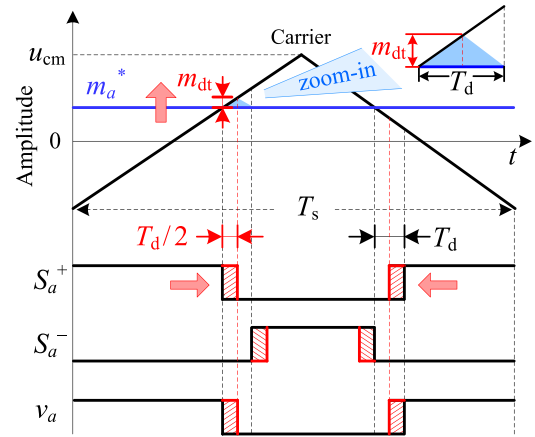


FIGURE 4. Illustration of the conventional time-based dead-time compensation in one switching period ($i_a > 0$).

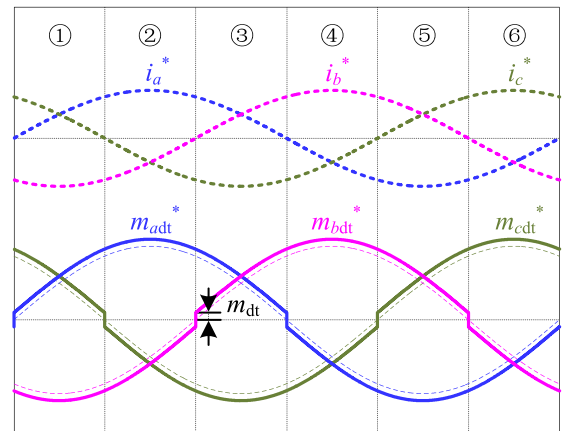


FIGURE 5. Three-phase reference currents and modulation waves in the conventional time-based dead-time compensation.

calculated as

$$m_{dt} = \frac{2u_{cm}}{T_s} T_d \quad (5)$$

where u_{cm} is the amplitude of the carrier; and T_s is the switching period. With the conventional time-based dead-time compensation, the amplitude adjustment of modulation waves in different current intervals are listed in Table 2. And the corresponding three-phase reference currents and modulation waves are shown in Fig. 5.

B. A MODIFIED TIME-BASED DEAD-TIME COMPENSATION

In order to combine the DPWM with the dead-time compensation achieving the performances of low switching loss and low output harmonics, Table 2 is transformed to Table 3, where the amplitude adjustment of modulation waves is presented in each current interval.

It can be seen that, the amplitudes of all the three-phase modulation waves need to be adjusted separately in each current interval. To simplify the calculation and facilitate the combination of the DPWM with the dead-time compensation,

TABLE 2. Amplitude adjustment of modulation waves in the conventional time-based dead-time compensation.

Reference current	Polarity	Amplitude adjustment
i_a^*	+	$m_{adt}^* = m_a^* + m_{dt}$
i_a^*	-	$m_{adt}^* = m_a^* - m_{dt}$
i_b^*	+	$m_{bdt}^* = m_b^* + m_{dt}$
i_b^*	-	$m_{bdt}^* = m_b^* - m_{dt}$
i_c^*	+	$m_{cdt}^* = m_c^* + m_{dt}$
i_c^*	-	$m_{cdt}^* = m_c^* - m_{dt}$

TABLE 3. Amplitude adjustment of modulation waves in different current intervals with the conventional time-based dead-time compensation.

Current interval	Polarity (i_a^*, i_b^*, i_c^*)	Amplitude adjustment
①	+ - +	$m_{adt}^* = m_a^* + m_{dt}, m_{bdt}^* = m_b^* - m_{dt}, m_{cdt}^* = m_c^* + m_{dt}$
②	+ - -	$m_{adt}^* = m_a^* + m_{dt}, m_{bdt}^* = m_b^* - m_{dt}, m_{cdt}^* = m_c^* - m_{dt}$
③	+ + -	$m_{adt}^* = m_a^* + m_{dt}, m_{bdt}^* = m_b^* + m_{dt}, m_{cdt}^* = m_c^* - m_{dt}$
④	- + -	$m_{adt}^* = m_a^* - m_{dt}, m_{bdt}^* = m_b^* + m_{dt}, m_{cdt}^* = m_c^* - m_{dt}$
⑤	- + +	$m_{adt}^* = m_a^* - m_{dt}, m_{bdt}^* = m_b^* + m_{dt}, m_{cdt}^* = m_c^* + m_{dt}$
⑥	- - +	$m_{adt}^* = m_a^* - m_{dt}, m_{bdt}^* = m_b^* - m_{dt}, m_{cdt}^* = m_c^* + m_{dt}$

the conventional time-based dead-time compensation will be modified as follows.

Taking the ③ current interval as an example, the amplitude adjustment of three-phase modulation waves in the conventional time-based dead-time compensation method can be given by

$$\begin{cases} m_{adt}^* = m_a^* + m_{dt} \\ m_{bdt}^* = m_b^* + m_{dt} \\ m_{cdt}^* = m_c^* - m_{dt} \end{cases} \quad (6)$$

In the three-phase converter without the neutral wire, injecting a zero-sequence component does not change the output voltage. Therefore, a zero-sequence component $-m_{dt}$ is superimposed in (6), and the amplitude adjustment is transformed into

$$\begin{cases} m_{adt}^* = m_a^* \\ m_{bdt}^* = m_b^* \\ m_{cdt}^* = m_c^* - 2m_{dt} \end{cases} \quad (7)$$

As seen in (7), after injecting the zero-sequence component of $-m_{dt}$, the dead-time compensation in interval ③ can be achieved by only adjusting the modulation wave of Phase C, while the modulation waves of Phase A and B

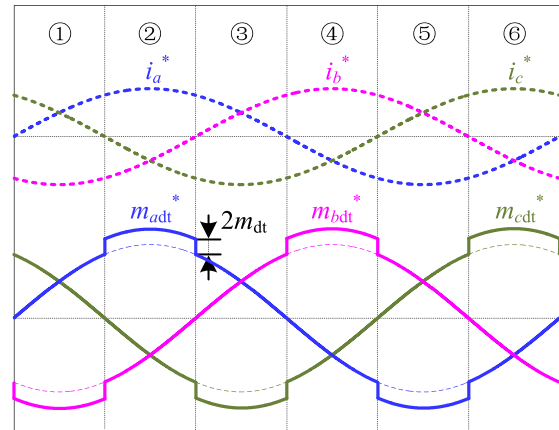


FIGURE 6. Three-phase reference currents and modulation waves in the modified time-based dead-time compensation.

remain unchanged. According to the above modification with zero-sequence component injection, Table 4 shows the amplitude adjustment of modulation waves in different current intervals. As seen, Table 4 is similar with Table 1, where the zero-sequence component is calculated separately in different current intervals. Therefore, with the modification, the dead-time compensation shown in Table 4 can be easily combined with the DPWM shown in Table 1.

Fig. 6 presents the three-phase reference currents and modulation waves in the modified time-based dead-time compensation. Comparing the three-phase modulation waves in Fig. 6 and Fig. 3, it can be seen that, the shape of modulation waves in the modified time-based dead-time compensation has become kind of similar with that of the DPWM for switching-loss reduction. The two schemes will be combined in next section to achieve the performances of switching-loss reduction and dead-time compensation.

It should be noted that, in the conventional time-based dead-time compensation, the amplitude increment of modulation wave is m_{dt} ; while in the modified time-based dead-time compensation, the amplitude increment is doubled as $2m_{dt}$. Therefore, the modified dead-time compensation has a relatively low linear modulation region and is more likely to cause the overmodulation issue. In this paper, through the combination with the DPWM, this drawback of reduced linear modulation region in the modified time-based dead-time compensation will be eliminated.

IV. COMBINED DPWM FOR SWITCHING-LOSS REDUCTION AND DEAD-TIME COMPENSATION

With the combination of the conventional DPWM and the modified time-based dead-time compensation, a new combined DPWM for switching-loss reduction and dead-time compensation is proposed as shown Fig. 7. Firstly, six current intervals are obtained according to the polarities of three-phase reference currents i_a^*, i_b^*, i_c^* . In each current interval, the modified time-based dead-time compensation is used to adjust the amplitude of original three-phase modulation waves m_a^*, m_b^*, m_c^* . Then, the zero-sequence component m_{zs}

TABLE 4. Amplitude adjustment of modulation waves in different current intervals with the modified time-based dead-time compensation.

Current interval	Polarity (i_a^* , i_b^* , i_c^*)	Amplitude adjustment
①	+ - +	$m_{bdt}^* = m_b^* - 2m_{dt}$
②	+ - -	$m_{adt}^* = m_a^* + 2m_{dt}$
③	+ + -	$m_{cdt}^* = m_c^* - 2m_{dt}$
④	- + -	$m_{bdt}^* = m_b^* + 2m_{dt}$
⑤	- + +	$m_{adt}^* = m_a^* - 2m_{dt}$
⑥	- - +	$m_{cdt}^* = m_c^* + 2m_{dt}$

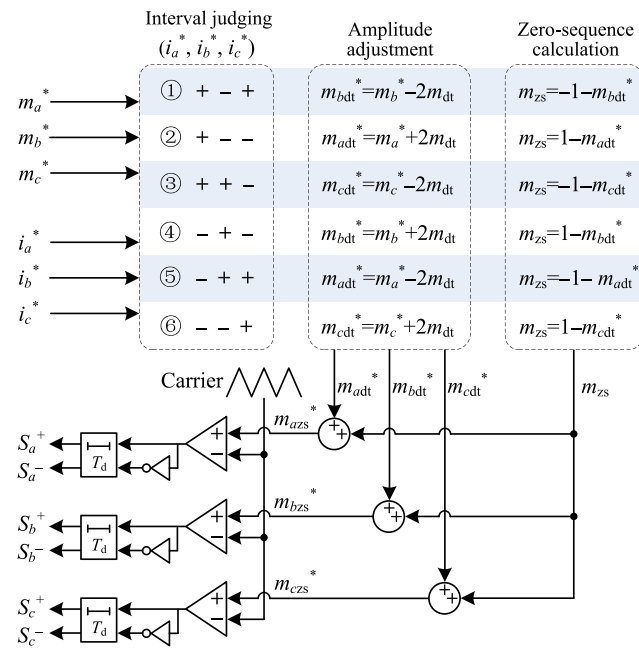


FIGURE 7. Diagram of the combined DPWM for switching-loss reduction and dead-time compensation.

is calculated and superimposed with three-phased modulation waves. Finally, drive pulses are generated by comparing modulation waves with the carrier, and the dead-time is added by the “on-delay” term.

It should be noted that, the zero-sequence component m_{zs} is calculated based on the modulation waves after the amplitude adjustment. If overmodulation happens in the modified time-based dead-time compensation, the amplitude of modulation wave can be compressed again when the zero-sequence component is injected. Therefore, in the combination of the conventional DPWM and the modified time-based dead-time compensation, the reduced linear modulation region and the possible overmodulation can be avoided.

Fig. 8 presents the three-phase reference currents, the zero-sequence component, and the modulation waves of the combined DPWM for switching-loss reduction and dead-time compensation. Although the shape of the zero-sequence

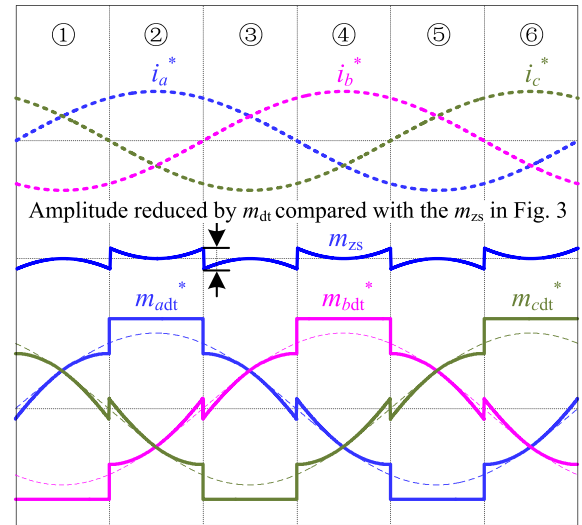


FIGURE 8. Three-phase reference currents, zero-sequence component, and modulation waves of the combined DPWM for switching-loss reduction and dead-time compensation.

component m_{zs} is the same with that of the conventional DPWM in Fig. 3, due to the combination with the modified time-based dead-time compensation, the amplitude of m_{zs} has been reduced by m_{dt} to accommodate to the amplitude adjustment of modulation waves in the modified dead-time compensation.

The new combined DPWM for switching-loss reduction and dead-time compensation has the following characteristics: 1) the current intervals obtained from current polarities are shared by the conventional DPWM and the modified time-based dead-time compensation, which can reduce the calculation burden of digital controllers; 2) in each current interval, the modified time-based dead-time compensation can be implemented by adjusting the amplitude of one-phase modulation wave; 3) through the combination with the conventional DPWM, the drawback of reduced linear modulation region in the modified time-based dead-time compensation is eliminated.

V. PROPOSED COMBINED DPWM BASED ON DSOGI-FLL FOR SWITCHING-LOSS REDUCTION AND DEAD-TIME COMPENSATION

A. DSOGI-FLL FOR CURRENT POLARITY DETECTION

Accurate current polarities are required in all the conventional DPWM, the time-based dead-time compensation, and the combined DPWM. Since high-frequency ripples are inevitable in the output current of converters, it is difficult to accurately determine the current polarity around the zero-crossing. With inaccurate current polarities, on the one hand, the position of the zero-sequence component injection in the DPWM will be affected, and the switching loss cannot be minimized; on the other hand, the dead-time compensation will be also affected, increasing harmonics in output currents.

The DSOGI-FLL [25]– [27] has good characteristics of filtering and frequency adaptability even under harmonic and

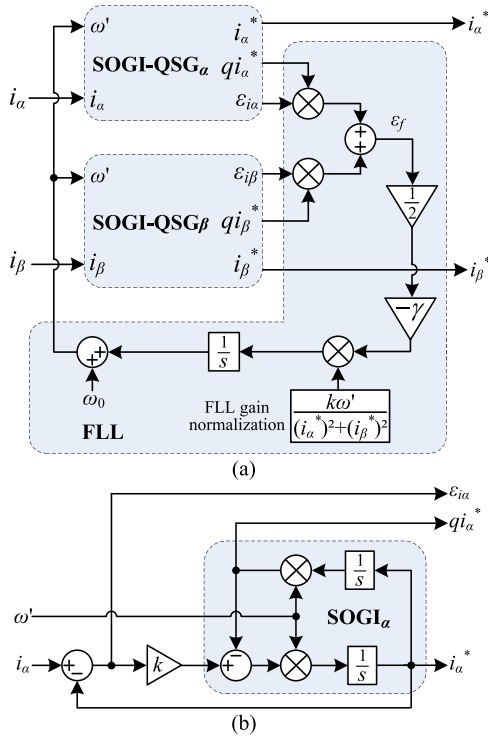


FIGURE 9. Diagrams of the (a) DSOGI-FLL and (b) SOGI-QSG α .

unbalanced conditions, which can provide accurate current polarities for the combined DPWM. Fig. 9 shows the diagrams of DSOGI-FLL and SOGI-QSG α , where ω' is the resonant frequency obtained by FLL. Transfer functions of the SOGI-QSG α can be expressed as

$$SOGI_{\alpha}(s) = \frac{i_{\alpha}^*}{k \varepsilon_{i\alpha}}(s) = \frac{\omega' s}{s^2 + \omega'^2}, \quad (8)$$

$$D_{\alpha}(s) = \frac{i_{\alpha}^*}{i_{\alpha}}(s) = \frac{k \omega' s}{s^2 + k \omega' s + \omega'^2}, \quad (9)$$

$$Q_{\alpha}(s) = \frac{q i_{\alpha}^*}{i_{\alpha}}(s) = \frac{k \omega'^2}{s^2 + k \omega' s + \omega'^2}. \quad (10)$$

When $\omega' = 100\pi$ rad/s and $k = \sqrt{2}$, the frequency responses of $SOGI_{\alpha}(s)$, $D_{\alpha}(s)$, and $Q_{\alpha}(s)$ are plotted in Fig. 10. As seen, $SOGI_{\alpha}(s)$ has an infinite gain at the frequency of ω' , which can achieve a control without steady-state error. $D_{\alpha}(s)$ and $Q_{\alpha}(s)$ show the band-pass and low-pass filtering characteristics, respectively, which can effectively attenuate the high-frequency harmonics in i_{α} . Moreover, $D_{\alpha}(s)$ has a zero-phase response at ω' , indicating that no phase shift exists between i_{α}^* and i_{α} . Therefore, using i_{α}^* as the reference current can accurately obtain the polarity of i_{α} .

B. PROPOSED COMBINED DPWM BASED ON DSOGI-FLL FOR SWITCHING-LOSS REDUCTION AND DEAD-TIME COMPENSATION

With accurate current polarities provided by the DSOGI-FLL, a combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation is proposed as shown

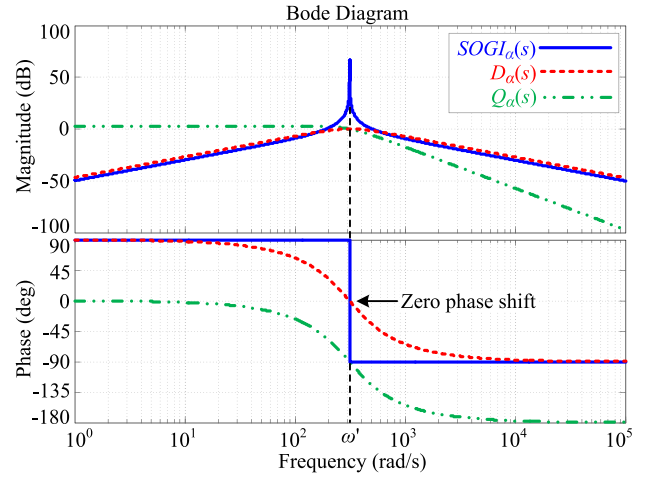


FIGURE 10. Frequency responses of $SOGI_{\alpha}(s)$, $D_{\alpha}(s)$, and $Q_{\alpha}(s)$ when $\omega' = 100\pi$ rad/s and $k = \sqrt{2}$.

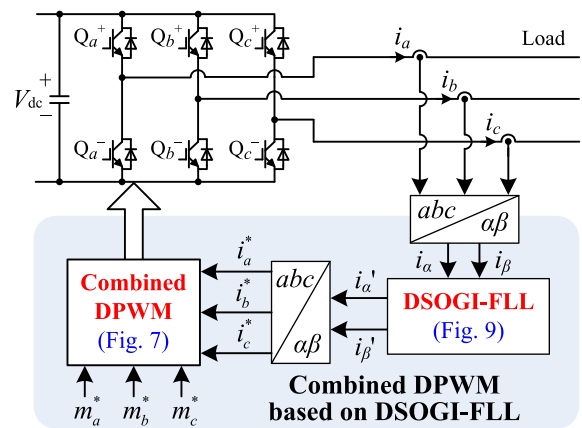


FIGURE 11. Combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation.

in Fig. 11. Firstly, the three-phase output currents i_a , i_b , i_c of the converter are measured by sensors, which are further transformed to the $\alpha\beta$ frame as i_{α} and i_{β} . Then, through the DSOGI-FLL in Fig. 9, the fundamental components i_{α}^* and i_{β}^* are extracted from i_{α} and i_{β} . Afterwards, three-phase reference currents i_a^* , i_b^* , i_c^* are transformed from i_{α}^* and i_{β}^* , which are used for judging different current intervals to implement the combined DPWM in Fig. 7, achieving minimum switching loss and dead-time compensation.

VI. EXPERIMENTAL VERIFICATION

In order to verify the combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation, an experimental setup of the three-phase two-level voltage converter is built as shown in Fig. 12. The DC power supply 62050H-600S from CHROMA is connected to the DC side of the converter, while the three-phase adjustable RL load is connected to the AC side. And the power analyzer WT500 from YOKOGAWA is used to measure both the DC input power and the AC output power, so that the efficiency

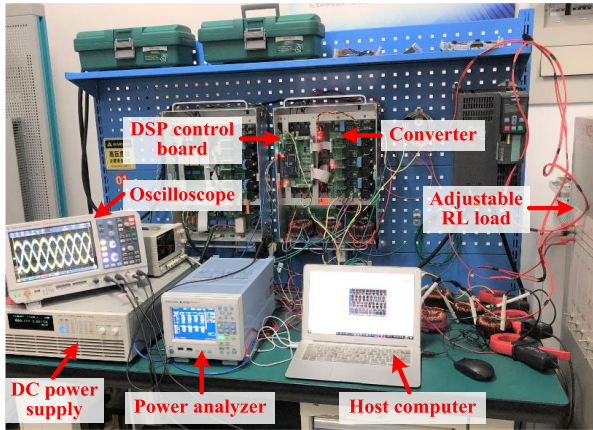


FIGURE 12. Experimental setup of the three-phase two-level converter.

TABLE 5. Experimental parameters.

Symbol	Parameter	Value
V_{dc}	DC-link voltage	600 V
f_s	Switching frequency	20 kHz
T_d	Dead-time	2 μ s
M	Modulation index	0.84
R_a, R_b, R_c	Load resistance	35.5 Ω
L_a, L_b, L_c	Load inductance	3.5 mH

of the converter can be calculated. Experimental parameters are shown in Table 5.

Firstly, the DSOGI-FLL for obtaining accurate current polarities are verified. The conventional SPWM with dead-time is employed. With the DSOGI-FLL shown in Fig. 9, reference currents i_a^*, i_b^*, i_c^* , which can be used for obtaining accurate current polarities, are extracted from three-phase output currents i_a, i_b, i_c . Fig. 13 presents the output current i_a and reference currents i_a^*, i_b^*, i_c^* outputted by a digital-to-analog converter (DAC). As seen, ideal sinusoidal reference currents i_a^*, i_b^*, i_c^* are obtained by the DSOGI-FLL, though both high-frequency and low-frequency current harmonics exist in the output current i_a . And with a zero phase response between i_a and i_a^* as shown in Fig. 10 at the fundamental frequency, a high accuracy of obtained current polarities can be guaranteed. The current polarities will be applied to the dead-time compensation and DPWM schemes in following experiments.

Due to the dead-time effect in the conventional SVPWM, there are relatively large low-frequency harmonics, e.g., 5th and 7th order harmonics, in the output current i_a shown in Fig. 13. And the THD of three-phase currents computed up to 100 kHz are measured as 4.44%, 4.64%, and 4.56%, respectively.

The dead-time effect is further suppressed respectively by the conventional and the modified time-based dead-time compensation schemes. And the modulation wave m_{azs}^* and three-phase output current i_a^*, i_b^*, i_c^* with the two schemes

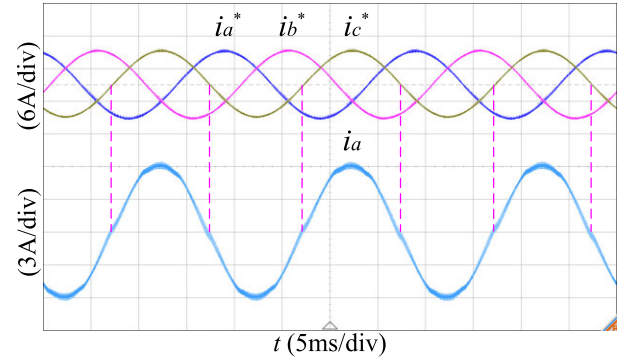


FIGURE 13. Three-phase reference currents i_a^*, i_b^*, i_c^* and the output current i_a .

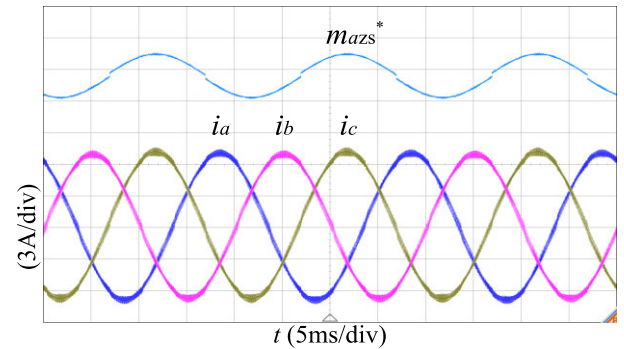


FIGURE 14. Modulation wave m_{azs}^* and three-phase output currents i_a^*, i_b^*, i_c^* with the conventional time-based dead-time compensation.

are shown in Fig. 14 and Fig. 15. The THD of three-phase currents with the two schemes are measured as 3.44%, 3.86%, 3.60% and 3.96%, 4.24%, 4.04%, respectively, which are all lower than those of the conventional SPWM. It should be noted that, the THD with the modified time-based dead-time compensation is slightly larger than that with the conventional time-based dead-time compensation, which is caused by the well-known common drawback of zero-sequence component injection [30]– [32]. In the modified time-based dead-time compensation, the zero-sequence component injection increases the amplitude of current ripples generating extra high-frequency harmonics in the output current. However, the zero-sequence component injection does not affect the low-frequency harmonics which will be presented later from the FFT results shown in Fig. 18.

The conventional DPWM and the proposed combined DPWM based on DSOGI-FLL are employed, respectively. The modulation wave m_{azs}^* and three-phase output currents i_a^*, i_b^*, i_c^* with the two DPWM schemes are shown in Fig. 16 and Fig. 17, respectively. The THD of three-phase currents with the conventional DPWM are measured as 5.46%, 5.62%, 5.48%. And those with the combined DPWM based on DSOGI-FLL are measured as 4.18%, 4.38%, 4.20%. It can be indicated that, the proposed combined DPWM based on DSOGI-FLL can effectively compensate the dead-time effect of the conventional DPWM, improving the output power quality.

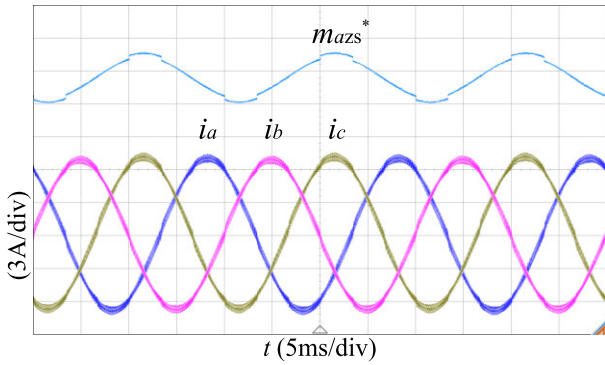


FIGURE 15. Modulation wave m_{azs}^* and three-phase output currents i_a, i_b, i_c with the modified time-based dead-time compensation.

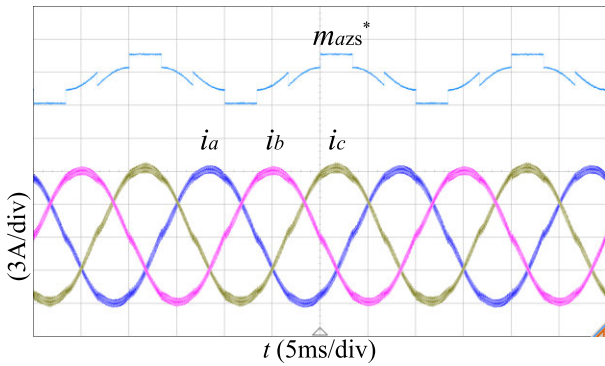


FIGURE 16. Modulation wave m_{azs}^* and three-phase output currents i_a, i_b, i_c using the conventional DPWM with minimum switching loss.

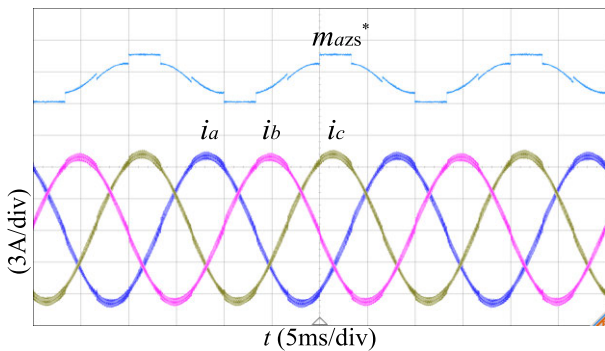


FIGURE 17. Modulation wave m_{azs}^* and three-phase output currents i_a, i_b, i_c with the combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation.

The low-frequency current harmonics of Phase A and efficiencies of the above mentioned modulation schemes are shown in Fig. 18. As seen, with the two time-based dead-time compensations and the proposed combined DPWM based on DSOGI-FLL, the 5th, 7th, and 11th order current harmonics are effectively suppressed compared with those of the conventional SPWM and DPWM.

Since the efficiency can be affected by the operating power, the efficiency comparisons should be carried out respectively without and with the dead-time compensation, which can eliminate voltage errors and increase the operating power. As seen in Fig. 18, in cases without dead-time compensation,

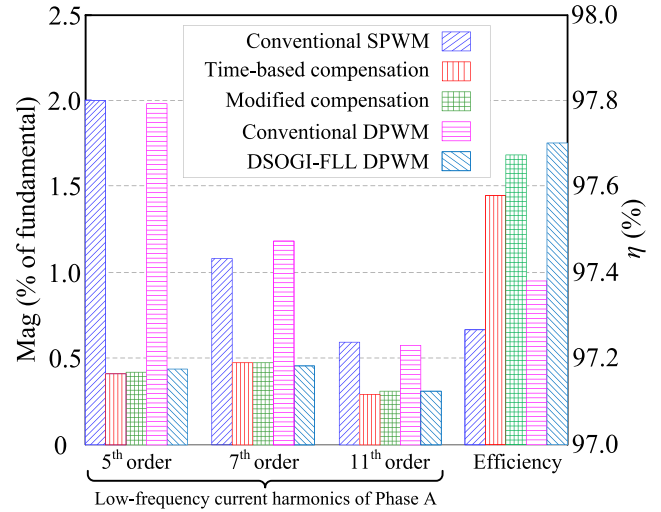


FIGURE 18. Low-frequency current harmonics of Phase A and efficiencies with different modulation schemes.

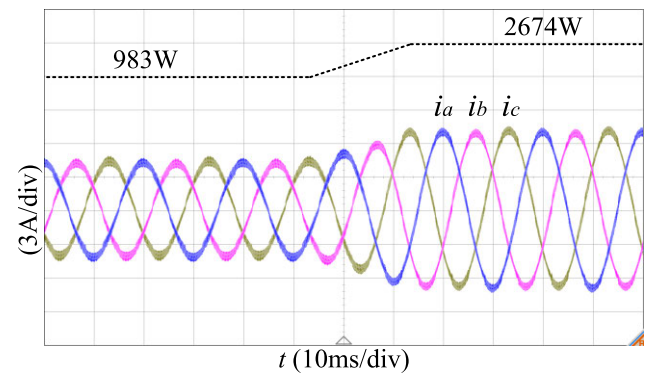


FIGURE 19. Dynamic three-phase currents of the combined DPWM based on DSOGI-FLL with the operating power increasing from 983 to 2674 W.

the efficiency with the conventional DPWM is higher than that with the conventional SPWM. In cases with the dead-time compensation, the efficiency with the proposed combined DPWM based on DSOGI-FLL is higher than those with the conventional and the modified time-based compensations. The efficiency comparisons can verify the effectiveness of DPWM on the loss reduction.

The above harmonic and efficiency comparisons verify that, the proposed combined DPWM based on DSOGI-FLL effectively takes advantages of both the dead-time compensation and the DPWM, achieving a performance of high output power quality and high converter efficiency.

Finally, the dynamic responses of the combined DPWM based on DSOGI-FLL are tested. Fig. 19 presents the dynamic three-phase currents with operating power increasing from 983 to 2674 W. As seen, in the whole power increasing process, the amplitude of currents gradually increase, and no obvious current distortion occurs in the dynamic process. It is indicated that, the combined DPWM based on DSOGI-FLL has a good dynamic adaptability to the power variation.

Fig. 20 further presents the dynamic three-phase currents with the frequency increasing from 60π rad/s (30 Hz) to

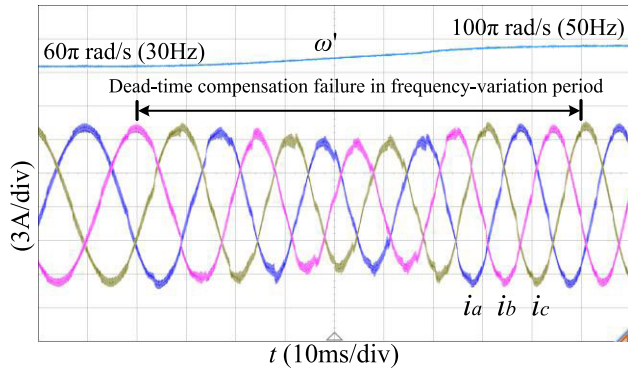


FIGURE 20. Frequency adaptability test of the combined DPWM based on DSOGI-FLL with the current frequency increasing from 60π to 100π rad/s.

100π rad/s (50 Hz). As seen, a dead-time compensation failure happens in the frequency-variation period, distorting the three-phase currents. While the distortion disappears when the dynamic process ends at 100π rad/s. The dead-time compensation failure is caused by the current-polarity error obtained from the DSOGI-FLL, which is inevitable when tracking currents with varying frequencies. Though the output current harmonics are increased in the dynamic process of frequency variation, the three-phase currents still retain sinusoidal, so that the stability of the converter can be guaranteed.

VII. CONCLUSION

The modulation scheme for simultaneously enhancing the efficiency and output power quality of the converter has been investigated in this paper. The time-based dead-time compensation has been modified to be implemented in different current intervals, which has been combined with the conventional DPWM for switching-loss reduction. The DSOGI-FLL has been adopted to detect accurate polarities of three-phase currents with ripples and harmonics. A combined DPWM based on DSOGI-FLL for switching-loss reduction and dead-time compensation has been proposed. The comparison of experimental results with different PWM schemes has verified that, the proposed combined DPWM based on DSOGI-FLL can effectively reduce the switching loss and compensate the dead-time effect, achieving high efficiency and high output power quality for three-phase two-level converters. Besides, the combined DPWM based on DSOGI-FLL has a good dynamic adaptability to power and frequency variations.

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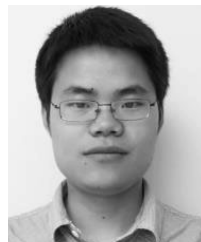
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