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A Serial Access Scheme Design on Memristor-CMOS Hybrid Memory

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ABSTRACT A new serial access scheme for memristor-CMOS hybrid memory cell is proposed, which addresses the limitations of sneak-path current, crosstalk and cell-cell interference. The serial access circuit consists of only one multiplexer and one I/O circuit, implementing memory addressing for memristor memory crossbar array. Memristor is used to store the bit information, and CMOS is used to isolate, control, decode and interoperate the logic. The proposed design is verified with PSPICE simulation utilizing a modified memristor model. Compared with conventional circuitry in parallel access scheme, the dedicated designed serial I/O circuitry for memristor-CMOS hybrid memory is simpler and area saving. The new serial access scheme, juxtaposed with conventional parallel access scheme, can get better performance in some area critical and ultra high frequency memory applications.

INDEX TERMS Memristor, serial access, parallel access, CMOS, nonvolatile memory.

I. INTRODUCTION

With digital electronics developing so fast these years, memory with smaller area occupation becomes more attractive in current integrated circuits and systems. Owing to the advantages of higher storage density and smaller nanometer dimension, the resistive random access memory (RRAM) becomes a competitive candidate to replace the current mainstream memory. Memristor is one of the best types for implementing RRAM among the STT-RAM, PCRAM and memristor. The two-terminal device is based on resistance switching mechanism, where the dynamic resistive state value determines the analog memory state of the device cell. Theoretically postulated by L.Chua in 1971 [1], first experimentally fabricated by HP Labs in 2008 [2], memristor draws much interest in both academia and industria, due to its wonderful characteristics such as nonvolatility, nano dimension, multistate, low power and high density [3]. Passive memristor-based crossbar array with no selector is the most dense memory system certainly [4]. However, the vital problem lies in that the power consumption of this passive structure will be ultra huge especially when the crossbar size is increasingly large. Besides, the sneak path current problem becomes uncontrollable, incurring huge power consumption. Read error for obtaining the targeted memory cell state is also becoming severer with increase in the array size [5]. That is to say, cell to cell interference becomes severer.

Inserting a selector into the memory cell is an effective solution to solve the sneak path current and inhibit the cell to cell interference [6]. In the current fabrication technologies, the one transistor-one memristor (1T1M) cell is a feasible scheme [7]–[9]. Although adopting the transistor will reduce the storage density of the memristor memory to that of transistor based memory. Note that the advantage of nonvolatility remains in the 1T1M structure, which ensures the design still outstands compared with the conventional SRAM cell (six transistors) and DRAM cell (one transistor and one capacitor). Memristor-CMOS hybrid structure applications have been proposed in [8], [10]–[13], showing better competitiveness and potential over conventional CMOS technology in many related electrical circuits and systems.

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When the memristor-based memory is utilized in electronic products, the read and write operations should be carefully considered. The read and write operations have been analyzed in some literatures such as [4], [9], [14]. In those papers the parallel access scheme is adopted for all read and write operations of memory cells, showing the current mainstream methodology. However, a new serial access scheme is proposed in the paper. The serial access scheme takes much smaller area, because n column input/output (I/O) circuits are replaced by one single I/O circuit and one multiplexer, shown in the following parts of the paper. This serial access scheme would be a competitive memory technology in the consumer electronics, especially in some area critical and ultra high frequency memory applications, even showing better performance than the parallel access scheme.

Considering that the parallel access operation can not avoid the cross-talk problem in ultra high frequency, which generally reduce the quality of the communication data. These factors such as transmission frequency and distance between the parallel lines impact the severity of the crosstalk problem. Correspondingly, several cross-talk reduction schemes in integrated circuits have been shown in [15]. Nevertheless, the serial access operation solves the cross-talk problem even in the infinitely high frequency theoretically. Hence the paper sheds some lights on the the serial access scheme.

In this study, a serial access scheme for memristor-CMOS hybrid momory is proposed and simulated. Combining memristor and transistor, a possible area-smaller read and write peripheral circuit is revealed. The rest of the paper is organized as follows: The memristor characteristics are depicted briefly and reviews about memristor based memory design are given in Sect. II. The memory cell using memristor-transistor hybrid approach and corresponding array architecture are presented in Sect. III. Comprehensive simulation results and analysis of the serial access memory structure are discussed in Sect. IV. Finally, Sect. V gives the conclusion.

II. BACKGROUND

A. REVIEWS ABOUT MEMRISTOR MEMORY DESIGN

Memory design is one basic research field for memristor applications. A three transistors and two memristors (3T2M) based memory cell has been proposed in [16], shown in Fig. 1(a). Then a SRAM constructed by the specific cell is analyzed in terms of read/write speed and power, which is much better compared with conventional SRAM technology. Another memory cell is made up by one transmission gate and one memristor (1TG1M) in [17], shown in Fig. 1(b). This SRAM design still remains the nonvolatility, then is analyzed in terms of read/write operation, switching speed (quicker) and energy requirement (lower), showing superior performance. Besides, an impressive memristor crossbar architecture is proposed in [10], shown in Fig. 1(c). The large crossbar array is made by isolating elements and many tiles, in which every tile is made up of the small size passive memristor crossbar. The small size passive crossbar

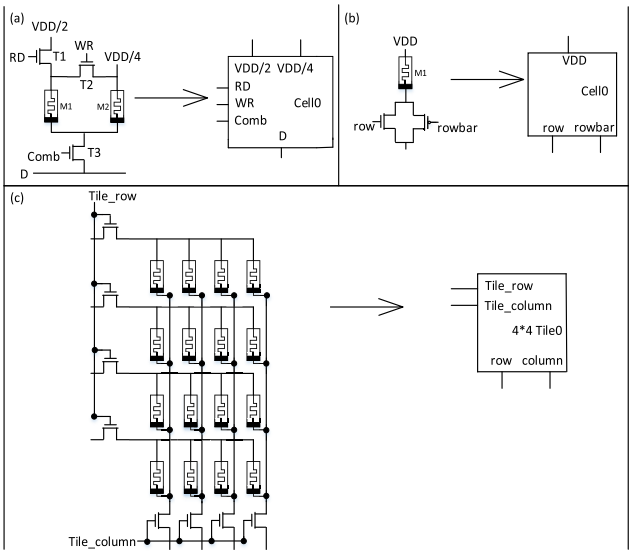

FIGURE 1. Schematics of the cell structure in different memory designs. (a) The cell is composed of 3T2M in [16]. (b) The cell is composed of 1TG1M in [17]. (c) The single tile is composed of 8T16M in [10]. The tile is the basic cell element to construct the memristor memory crossbar array. Each memristor cell inside the tile can be addressable independently.

array can tolerate sneak path current in digital circuit without the isolating element. Isolating elements are inserted among many tiles. Through this specific design, the overall area is relatively smaller, in which every memristor cell just needs about 0.5 transistor or 0.25 transistor (0.5T1M). Obviously the manufacturing process for this architecture will be a little more complex. These three architectures are all adopting the parallel access scheme. However, this paper proposes a new serial access scheme, given by Sect. III.

B. MEMRISTOR CHARACTERISTICS

The TiO_2-based thin film memristor is first fabricated by the HP Labs [2]. Since then the memristor switching mechanism and models have been studied widely. One typical fabricated prototype TiO_2 thin film has a certain width D, sandwiched between two metal contacts. This thin film consists of two layers. The one is a highly resistive undoped layer, made up of pure TiO_2. The other one is a highly conductive doped layer with width $w(t)$, made up of TiO_{2-x}.

The state variable $w(t)$ determines the overall resistance of the memristor (memristance). The parameter of memristor $x(t)$ are the normalization of $w(t)$ by Eq. (4), which can depict the intrinsic property of memristor more clearly. Note that the varying range of $x(t)$ is between 0 and 1, where $x(t) = 0/x(t) = 1$ means that the current memristance is R_{off}/R_{on}. R_{off} is the maximum memristance when the memristor is in the high resistive state (HRS), defined as logic 0. R_{on} is the minimum memristance when the memristor is in the low resistive state (LRS), defined as logic 1. When a positive voltage is applied to the doped layer, the doped region expands, thus the memristance decreases. Similarly, when a negative

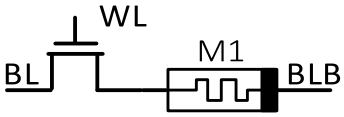

FIGURE 2. Schematic of the single cell structure.

voltage is applied to the doped layer, the doped layer shrinks, thus the memristance increases [14]. That is to say, memristance can be tuned to any arbitrary desired resistive state in the permissible range when applied voltage/current amplitude and duration time are appropriate. The HP TiO_2 memristor model is defined by the following equations [2], [18]:

$$v(t) = M(t)i(t) \tag{1}$$

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{on}}{D^2} * i(t) \tag{2}$$

$$M(x) = R_{on}x(t) + R_{off}(1 - x(t)) \tag{3}$$

$$x(t) = \frac{w(t)}{D} \tag{4}$$

Here, $x(t)$ is the normalized state variable of memristor, $w(t)$ is the thickness of the conductive doped region varying with time, D is the thickness of the TiO_2 thin film, μ_v is the average ion mobility, $v(t)$ and $i(t)$ are voltage and current that apply across the memristor. A window function [18] is adopted to approximate the nonlinear behavior of memristor, where the memristor behavior becomes more nonlinear with increase in the parameter p.

Utilizing the memristor threshold and analog tuning characteristics [4], the memristance will not change in the reading operation when the absolute value of applied voltage is less than threshold. Assuming the absolute value of positive and negative threshold voltages both are 1V, the small voltage less than threshold is used in the read operation. On the other hand, when the applied voltage is larger than the threshold, the memristance will change correspondingly depending on the applied voltage in the write operation.

III. MEMRISTOR-BASED MEMORY CELL AND ARCHITECTURE DESIGN

A. BIT CELL

The nonvolatile memristor based memory cell is the same as that in papers [8], [9], whose structure is shown in Fig. 2. The 1T1M cell is made of only one access transistor and one memristor, which ensures its compatibility with current CMOS technology. The interface connections to other cells and the I/O circuitry are shown. The negative terminal of the memristor is connected to the bitline bar (BLB), while the positive terminal of the memristor is connected to the drain terminal of the transistor. The source terminal of the transistor is connected to bitline (BL) and the wordline (WL) is used to control the gate terminal of the transistor.

When the WL is at logic one state, the gate terminal of NMOS T1 is in ON state. Then the current can be passed in both directions to read or write the state of memristor. When the WL is at logic zero state, the gate terminal of NMOS T1 is in OFF state. The chosen memristor is in the locked state and no current can flow through it, meaning that the memristance changes negligibly. Note that no standby energy is needed to maintain the stored information for the memristor when the supply power is off, indicating the cell design supports nonvolatile memory.

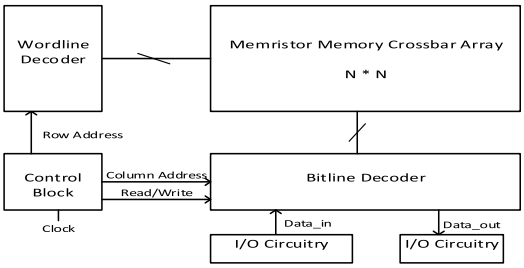

FIGURE 3. Block diagram of the memristor based memory crossbar array architecture.

Then the 1T1M cell is utilized to design the memory array architecture, whose structure is shown in Fig. 3. The array contains some key blocks, such as control block (to generate the control signals to trigger memory access), the wordline/bitline decoding block (to select the specific row/column), the I/O block (to sense and transfer the input data into the array or output data out of the array). These control signals and logic are similar to that in conventional SRAM-based memory [19].

B. PARALLEL AND SERIAL ACCESS MEMORY ARCHITECTURE

The conventional parallel memory array architecture in [9] is shown in Fig. 4. CMOS-based logic is used for selecting and sensing the data, while the memristor element is used as a nonvolatile storage cell. General read, write, address, data in and data out operations are executed when control signals are correctly configured, respectively. These interface signals used for accessing the array are also compatible with mainstream CMOS-based memory. The I/O circuitry for one column of the array is shown in Fig. 5. EN_Write and EN_Read, V_Precharge are the write enable, read enable and supply voltage of the BL for read access. TG is the abbreviation of transmission gate. V_ref is the reference voltage terminal for the comparator. The Data_in and Data_out signals are the input and output pin for read and write operations. All BLBs and BLs of the cells in one column are shorted together respectively, then fed into the corresponding I/O circuitry. Note that there is one I/O circuit in every column. The timing sequence of these control signals are discussed in the following Simulation Section.

When EN_Read is being activated, the memristor's unidirectional read operation is shown in the dashed line in Fig. 5. The arrow in the dashed line indicates the current flow of read operation. When EN_Write is being activated, considering writing LRS or HRS into memristor, the memristor's write operation is bidirectional, shown in the dashed-dotted line

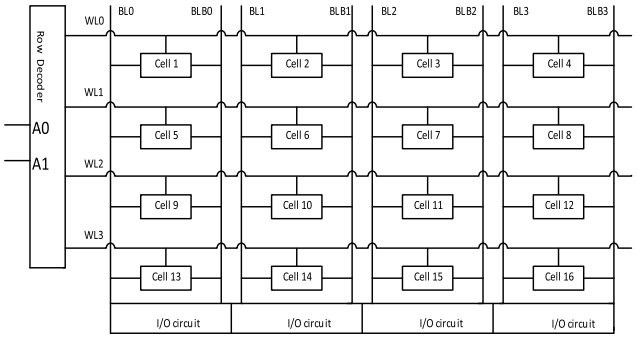

FIGURE 4. Schematic of parallel access scheme for the memristor memory crossbar array.

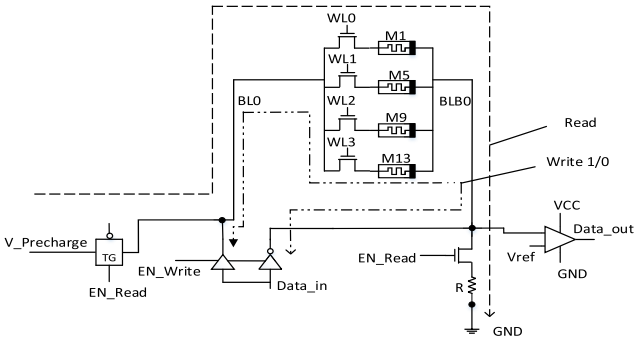

FIGURE 5. Schematic of the proposed I/O circuitry for one slice in the general memristor memory crossbar array. The circuit current flow for read operation is shown in the dashed line, unidirectionally. The circuit current flow for write operation is shown in the dashed-dotted line, bidirectionally.

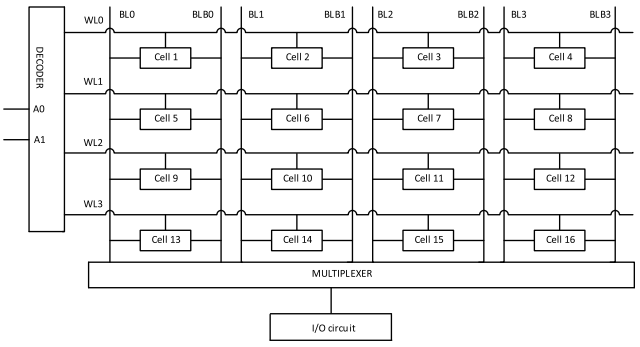

FIGURE 6. Schematic of the proposed serial access scheme for the memristor memory crossbar array.

in Fig. 5. The hollow arrow in the dashed-dotted line indicates the current flow of writing LRS into memristor, meanwhile the solid arrow in the dashed-dotted line indicates the current flow of writing HRS into memristor.

The improved serial memory array architecture is shown in Fig. 6. A column multiplexer is added to decode the column, making the I/O circuitry can be shared among all columns instead that every column needs an I/O circuit, shown in Fig. 7. This simpler method will be of benefit in area saving for the circuit.

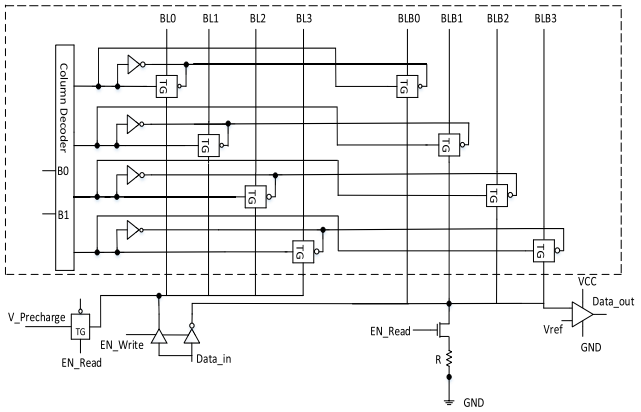

FIGURE 7. Schematic of the proposed I/O circuitry for the serial access scheme in the memristor memory crossbar array. The circuit implementation of the multiplexer is shown in the dashed line. The I/O circuit is the same with that for parallel access scheme, shown out of the dashed line.

TABLE 1. Transistor count comparison between parallel access scheme and proposed serial access scheme.

n-input	parallel scheme in [9]	proposed serial scheme
4	72T	40T (22T+18T)
8	144T	94T (76T+18T)
16	288T	194T (176T+18T)

The comparison of the memristor and transistor counts between the two structures is shown in Table 1. The row decoder and memory cell element are the same for the parallel and serial memory array architecture. The differences between these two structures are the column multiplexer and I/O circuit. Assuming that every I/O circuit consists of 18 transistors. Supposing that there are n columns, for conventional parallel memory array architecture, it contains about $18*n$ transistors for the whole I/O block. Considering the proposed serial memory array architecture, it contains only one I/O circuit and one multiplexer. The 4-input, 8-input and 16-input multiplexer is made up of 22, 76 and 176 transistors, respectively. When the number of array column size n is larger, the multiplexer and I/O circuit in the serial access scheme for memory array architecture saves much more transistors, compared with that in parallel access scheme. Considering that there are many arrays in a large capacity storage, the transistor numbers saved by this scheme will be substantial.

IV. SIMULATION AND DISCUSSION OF THE MEMORY DESIGN

We use the modified SPICE netlist in [18] for the memristor to start the PSPICE simulation in CADENCE environment, validating the correct functionality of serial access architecture. Firstly the timing sequence simulation for memory access is explained in orders: Writing 1 into *Cell*_1 starts at 0ms. Writing 0 into *Cell*_1 starts at 1ms. Reading 0 from *Cell*_1 starts at 2ms. Writing 0 into *Cell*_1 starts at 3ms. Writing 1 into *Cell*_1 starts at 4ms. Reading 1 from *Cell*_1 starts at 5ms.

Taking Fig. 6 and Fig. 7 as an example, when the row decoder and column decode inputs A0, A1, B0 and B1 are all equal to zero, The first row and first column are selected, meaning that the specific memristor cell *Cell*_1 is chosen. The circuit parameters are as following: R = 10kΩ (the value is the geometric mean of R_{off} and R_{on}), $V_{Precharge} = 0.8$V (lower than memristor threshold 1V), $V_{ref} = 0.6$V. The ionic mobility of memristor μ_v plays a key role in determining the writing speed of the memristor based memory. In this paper, μ_v is set to $10^{-12}m^2s^{-1}V^{-1}$ to accommodate the low varying rate of general CMOS chips to show the memristance varying waveform.

Data_in = 1 is used to implement writing LRS into memristor and the current flows from BLB to BL. Data_in = 0 is used to implement writing HRS into memristor and the current flows from BL to BLB. EN_Write is the enable write signal. EN_Read is used to read the temporary memristance with V_Precharge.

There are four cases for single cell read and write operations. The detailed configurations of signals are explained in orders.

- Write 1: When writing LRS into the memristor, the signals should be set as follows: Data_in = 1, EN_Write = 1, V_Precharge = 0V, EN_Read = 0. Then the memristance of *Cell*_1 will be tuned to the LRS state (from 0ms).
- Write 0: When writing HRS into the memristor, the signals should be set as follows: Data_in = 0, EN_Write = 1, EN_Read = 0, V_Precharge = 0V. Then the memristance of *Cell*_1 will be tuned to the HRS state (from 1ms).
- Read 0: When reading out the memristor resistive state, the signals should be set as follows: EN_Write = 0, V_Precharge = 5V, EN_Read = 1. If the memristor is in the HRS state, the analog output is 0.288V, which is less than V_{ref}, then the digital output is 0V, meaning that the chosen cell *Cell*_1 is in the HRS state (from 2ms).
- Read 1: Similarly, when reading out the memristor resistive state, the signals should be set as follows (same as the case of Read 0): EN_Write = 0, V_Precharge = 5V, EN_Read = 1. If the memristor is in the LRS state, the analog output is 0.617V, which is larger than V_{ref}, then the digital output is 5V, meaning that the chosen cell *Cell*_1 is in the LRS state (from 5ms).

Note that for read operation, the signal Analog output is the criterion, which has some connections with memristance. However for write operation, the signal Memristance is the criterion, which has no connections with the signal Analog output. The four cases of read and write operations for the chosen memristor cell are shown in Fig. 8. The simulation experiment result matches with the theoretical result. The memristance is tuning correctly according to the control signals. The relative sensing margin is calculated as (0.617-0.288)/0.8 = 41.1%, which is wide enough to distinguish the LRS state and the HRS state. The read and write

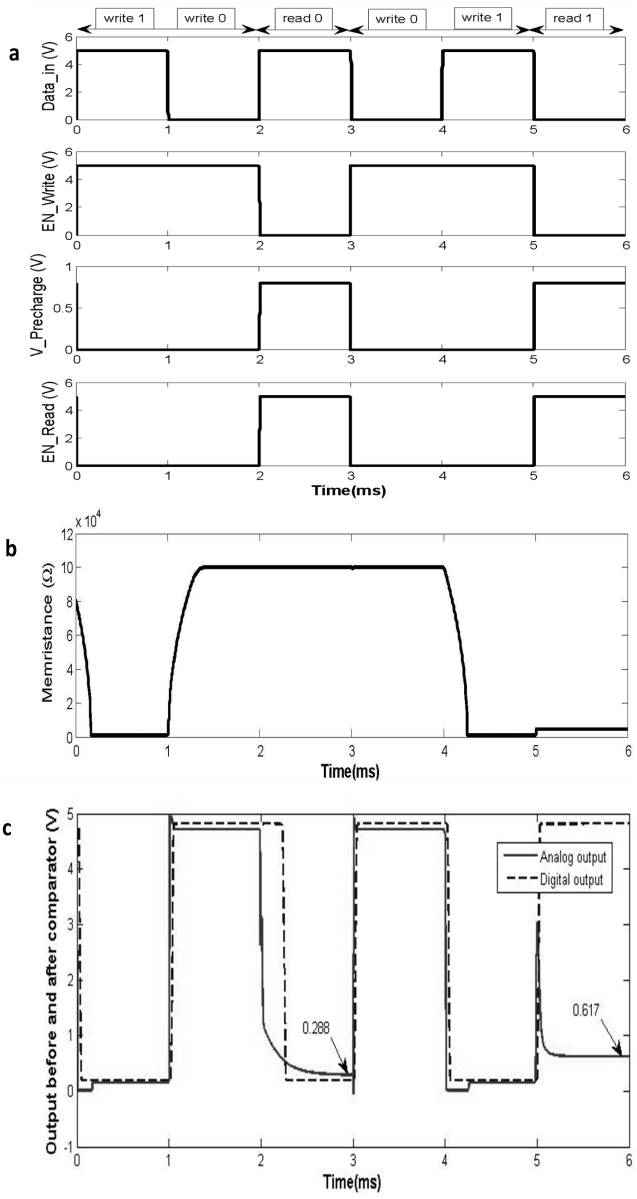

FIGURE 8. Simulation of the memory consecutive serial access operations. a, The input control signals for consecutive read and write operations. b, The memristance of chosen cell is tuning according to the write control signals. c, The analog output and digital output signals for read operations. Note that reading the chosen memristor which is in OFF state, the analog output is 0.288V (less than V_{ref}). While reading the chosen memristor which is in ON state, the analog output is 0.617V (larger than V_{ref}). Thus the chosen cell state can be identified clearly. The signal Analog output is the analog Data_out for the input terminal of comparator while the signal Digital output is the digital Data_out for the output terminal of comparator.

power consumptions are 9.1uW and 157.5uW respectively, which are similar with that (32.3uW and 136.1uW) in [16]. The read power is smaller because the memristor threshold reduces the power consumption in this design.

Then the state of cells that are chosen and unchosen are in shown Fig. 9. Only the chosen cell will change correctly according to the control signals, while other unchosen cells remain the same state, indicating the robustness against

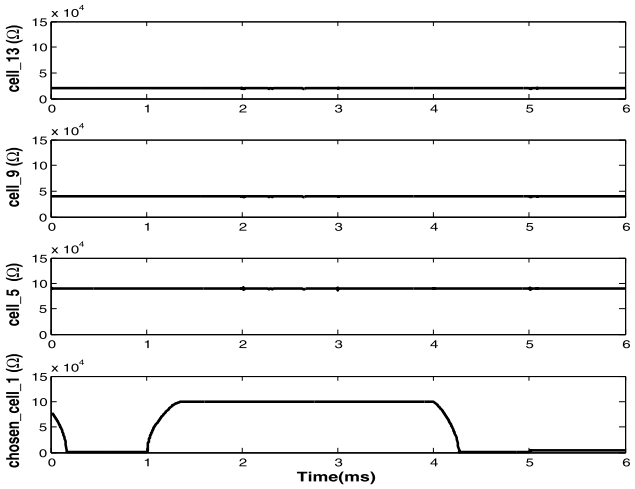

FIGURE 9. Simulation of chosen and unchosen bit cells state. The memristance of the chosen cell is changing according to the control signals. While the memristances of the unchosen bit cells remain almost the same value, verifying the robustness of the design against interference from the surrounding cells.

TABLE 2. Access and response latencies between the parallel access scheme and proposed serial access scheme.

operation mode	write 1	write 0	read 1	read 0
parallel scheme in [9]	50ns	54ns	52ns	90ns
proposed serial scheme	56ns	58ns	55ns	94ns

interference from the surrounding cells. Besides, the interference problem is mainly solved by the isolating element transistor in 1T1M hybrid structure. Compared with conventional parallel access scheme, there is almost no difference in the interference for the serial access scheme, meaning that the isolating element is effective for overcoming the interference.

Comparing the serial scheme simulation with the parallel scheme simulation on the hundred nanosecond time scale (μ_v is set to $10^{-8}m^2s^{-1}V^{-1}$), the measured access latency difference and response latency difference between the two schemes are shown in Table 2, which are mainly caused by the column multiplexer. Through the data calculation, the latency degradation is no more than 12% ((56-50)/50 = 12%). On the other hand, combined with Table 1, the saved area for the proposed serial scheme gets at least more 32.6% improvement compared with the parallel scheme.

Furthermore, the consecutive read and write operations of many memory cells in different locations are considered, simulation results in each following step is similar to that in the first step. In the first step, the address signals are set as follows: A0 = 1, A1 = 1, B0 = 0, B1 = 0. The memristance of *Cell*_13 is changed according to the signal Data_in (from 0ms to 6ms). In the next step, the address signals are set as follows: A0 = 1, A1 = 1, B0 = 1, B1 = 0. The memristance of the *Cell*_14 is changed according to the signal Data_in (from 6ms to 12ms, the signal waveform in this time slot is the same as that in the time slot from 0ms to 6ms). Note that users can define the Data_in signal waveform with their need. These accessing operations for multiple cells start with write

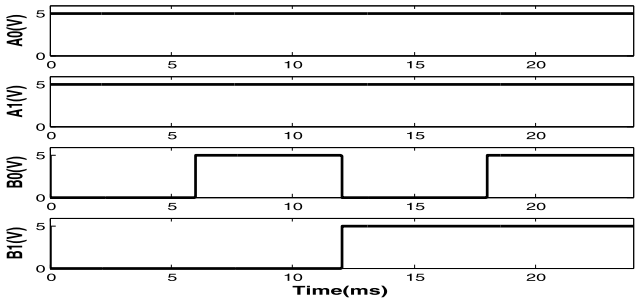

FIGURE 10. Waveform of row and column address signals in the read and write operations for an entire row at once. Note that the first bit, second bit and third bit and fourth bit of the fourth row are selected in orders by these sequential signals.

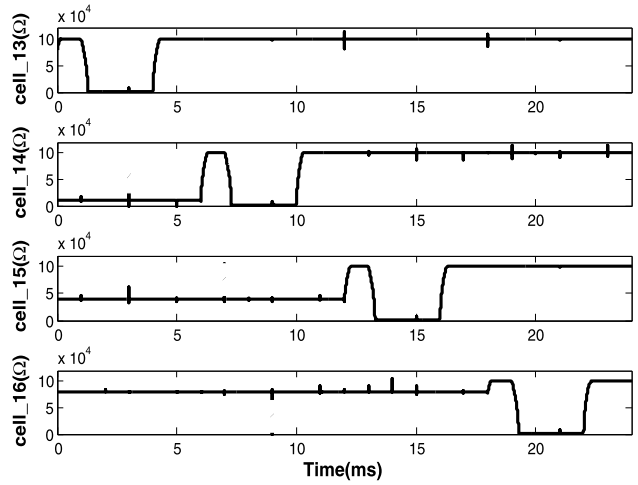

FIGURE 11. Simulation of read and write operations for an entire row at once. The read and write operations for the first bit, second bit, third bit and fourth bit of the fourth row are shown in orders according to the corresponding row and column address signals shown in Fig. 10. Note that only the memristance of chosen cell is changed according to the read and write signals, which are similar to that in Fig. 8, meanwhile the memristance of unchosen cells remain the same as the previous memristance value.

0 to show the difference with that in Fig. 8, thus broadening the generality of the serial scheme for memory design. The timing diagrams for *Cell*_15 and *Cell*_16 are similar with that in *Cell*_13, shown in Fig. 10 and Fig. 11. The simulation results verify that the consecutive access operations for different memory cells such as accessing an entire word at once work correctly.

V. CONCLUSION

A serial access scheme on memristor based memory is proposed in this paper. In comparison to parallel access scheme, the serial access scheme shows the advantages of taking smaller area overhead and overcoming the cross-talk issues. Timing sequence diagrams of read and write operations for the memory architecture are shown. Simulation results verify the feasibility of the scheme. The memory cell is compatible with conventional SRAM module, which has its own advantages in portable devices and consumer electronics (such as smart glasses and smart micro robots). Taking

note that whatever serial access scheme is temporarily ahead of parallel access scheme or vice versa, the serial access scheme is important in some specific applications, even is better against the parallel access scheme in some area critical and high frequency occasions. Furthermore, the combination of serial access scheme and parallel access scheme can be applied to improve the memristor-CMOS hybrid memory performance. More work needs to be done for memristor-CMOS hybrid nonvolatile memory in terms of lower power, faster speed and better compatibility.

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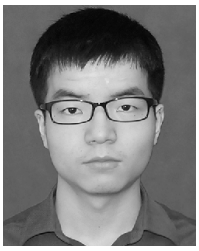

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