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Influence of a Proposed Switching Method on Reliability and Total Harmonic Distortion of the Quasi Z–Source Inverters

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ABSTRACT An Improved Sinusoidal Pulse Width Modulation (ISPWM) technique carried out to obtain pure sine waves for voltage and current signals in Quasi Z-Sourc Inverters (QZSIs) in the load side is given in this study. This switching method can be examined to two and multi-phase approaches simply through the addition of the same controller structure to per phase. This is the main advantage of the proposed converter to obtain higher voltage gains at the output ends of this inverter. The idea is to generate a positive rectified voltage at the output point of the QZSI and positive and negative rectified voltages at the output terminals of the QZSI in two-phase approaches to improve the quality of the output voltage of the F-Bridge Inverter (FBI). These rectified voltages are applied to the Full-Bridge Inverter (FBI) block and pure sine waves to obtain the load current and voltages. 1.34% of the Total Harmonic Distortion (THD) for the output voltage has been reported in the one-phase system while 0.88% of THD has been obtained in the two-phase approach. Besides, the reliability of the QZSI was tested through the Mean Time to Failure (MTTF) analysis with the values of the proposed components. The calculations show a very good result for the long-life of the converter. All experimental and simulations steps have been obtained for the same values of the components to support and confirm the accuracy and correctness of the proposed IMSPW. For the states of single-phase and two-phase converters, a 50 Hz sine-wave with 220 V and 440 V peak to peak amplitude has been acquired. Evaluations of the quality of the voltage and current waveforms related to different active (Resistive, P) and reactive (combination of Resistance and Inductance, QL) loads have been carried out. Experimental results show confirmation for all simulation and mathematical results.

INDEX TERMS Sinusoidal pulse width modulation (SPWM), F-bridge inverter (FBI), total harmonic distortion (THD), mean time to failure analysis (MTTFA).

I. INTRODUCTION

Recently, high voltage inverters have been more commonly used since they have the ability to generate the output voltages with suitable harmonic distortion by means of simple control methods. [1] has proposed the use of multi-level inverters in the structures of various approaches, including Flexible Alternating Current Transmission Systems (FACTs), High-Voltage Direct Current (HVDC) transmissions, ac drives, and active filters, to handle the voltage limitation and the currents spikes of the power switches. Multi-level inverters are highly appropriate for high power utilization owing to their favorable features among which are high-power generation, common voltage reduction, and appropriate harmonic for the output waveforms and lower dv/dt level for the output voltages [2]. On the other hand, among some of the most significant advantages of the multi-level inverters are reducing the THD, losses, Electromagnetic Interference (EMI) and the stress of power switches [3].

Traditional Voltage Source (VSI) and Current Source Inverters (CSI) have several common problems such as the inability to use the buck-boost converter in their structure

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and the necessity to apply one buck or boost converter. VSI main circuit and CSI cannot be used for one another and other main circuits are not interchangeable. Besides, their reliability is affected due to EMI noise. Some studies have been conducted in investigating the inverters' structures so as to connect to micro-grid applications [2]–[7]. Inverters can be categorized into two structures: isolated and non-isolated structures. In terms of the weight, size, and cost, among isolated inverters are a high-frequency transformer, also known as fly-back inverters [8]–[11], serial connection of DC-DC converter and a full-bridge inverter [12], [13] and serial connection of a DC-DC converter, a transformer and an ac-ac converter [14]. Nonetheless, these topologies are able to generate a high voltage gain and have advantages in terms of safety, but complicated control structures are features that all have. The classical square wave inverter that is applied in low and medium powers contains various drawbacks, such as the production of low-level harmonics at the output voltage. One of the solutions to achieve a voltage of almost no harmonics in high power converters is the use of PWM control techniques. The goal of the PWM techniques is to generate a sine voltage wave, with limited amplitude and frequency values. PWM switching strategies express issues such as THDs and the effective use of the DC bus bands as well as issues such as electromagnetic interference (EMI), switching losses, and a better spread of harmonic spectrum.

Pulse width modulation technique (PWM) is applied to have the achievement of the variable voltage and variable frequency in DC-AC and AC-DC converters. This switching technique is commonly applied in some applications such as variable speed drives (VSDs), uninterruptible power supplies (UPS), static frequency changers (SFCs), and so on [15]. There are some methods for producing PWM waveforms among which the most commonly used cases are PWM based triangular carrier (TCPWM) and PWM based spatial vector (SVPWM). In TCPWM methods, such as PWM sinusoidal-triangular (SPWM), there is a comparison of PWM signals with three-phase reference modulating signals with the triangular carrier. The frequency of the carrier signal is much higher than the modulator signal. The size and frequency of the modulator signal determine the size and frequency of the main component on the line side. In SVPWM methods, a turning reference vector is used as a voltage reference instead of a three-phase modulating waveform. In this method, the size and frequency of the reference voltage vector control the size and frequency of the main component on the line side. The primary drawbacks of these control techniques are the complicacy of mathematical analysis for the control process and the complexity of the application [16]. There has been a comparison between specific harmonic elimination (SHE-PWM) and Single carrier sinusoidal PWM (PWM-SC) in [17]. The voltage injection method into the reference signal is examined in [18]. A pre-calculated PWM method is given in [19]. A multi-cell cascade inverter structure is introduced in [20] and repetitive control structure is illustrated in [21]–[23]. In all of these structures, the THD value ranges between 5% and 8 % for voltage, and particularly current signals. Besides, cascade topologies use more power switches; therefore, it makes them have more complexity and size, higher cost, and lower efficiency. This study has contributed much to the simultaneous control of the power switches by SPWM topology. We mainly focus on quasi Z source inverter structure as the Z source topology requires LC network placement at the DC source side, so input and output are connected to the common ground point that prevents the generation of dispersion current in the structure which is a vital element in renewable energy sources practices. A modern, inexpensive and small controller structure for semi Z source inverters that is appropriate to apply in the aforesaid grid-connected applications. As the voltage curve is generally linear in the full-bridge inverter structure, the reference waveform is likely to be a sinusoid.

An improved SPWM method for the one-phase and multi-phases approaches of the QZSIs has been proposed in this study. Considering that in per time interval, merely one of the power switches is in on mode and another one is in off state, the same control signal can easily be produced by the controller. Also, driving another MOSFET can be achieved in a NOT state. A mathematical analysis related to a QZSI has been given and the controller is designed based on these calculations. Simulation results demonstrate that when the second load is switched on, no difference is observed in the output voltage signal and the change in the current wave is observed at an acceptable level.

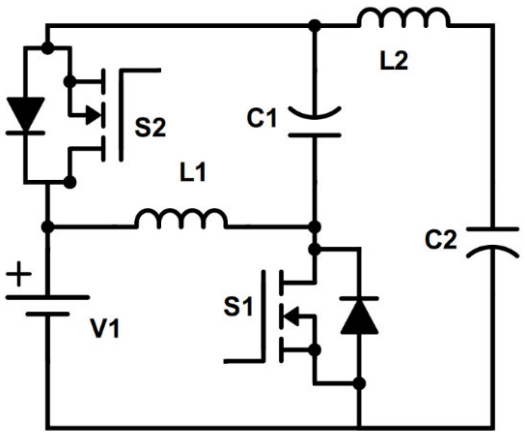
Besides, the conventional SPWM control signals and equations have been given together while the simple and novel aspect of the proposed control equation has been proved. Also, the voltage and current stresses on power switches will be presented to apply MATLAB/SIMULINK. The values of all components are selected through the equations and the failure of life along with an MTTF analysis. Finally, an experimental prototype is given along with results.

II. PROPOSED SPWM CONTROL METHOD

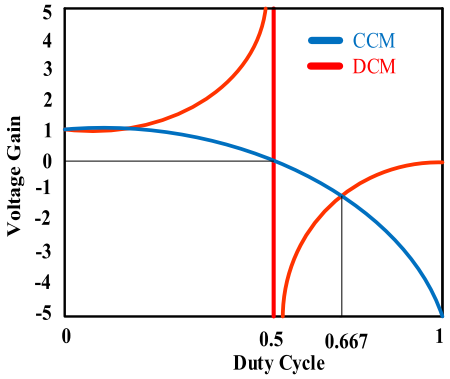
Figure 1(a) includes the common structure of the QZSI. The circuit is comprised of two power switches, two capacitors, and two inductors. This converter is highly advantageous in that this structure does not contain any use of a transformer. Figure 1(b) demonstrates the voltage gain of the QZSI versus the duty cycle (D) of the switch S1 for both Continuous (CCM) and Discontinuous Current Modes (DCM). The DCM state is generally not selected due to the current problem related to heavy loads. For the CCM state, as is clear from the figure, for duty cycles ranging between 0 and 0.5, this converter can highlight a positive voltage while for ($0.5<D<0.667$) it will produce a negative voltage and for $D=0.5$ the output of the converter is equal with zero.

Different values of the duty cycles that represent the state of all components are shown in Figure 2.

Figures 2(a) and (b) demonstrate the state of the converter for ($0<D<0.5$) while figures 2(c) and (d) exemplify the conditions for ($0.5<d<0.667$).



(a)



(b)

FIGURE 1. (a) conventional QZSI, (b) Voltage gain of QZSI versus Duty cycles for both CCM and DCM states.

It is seen per both work-conditions that in a per interval of a period, only one power switch is in ON mode and another one is in OFF state. For the first state (0<D<0.5), when the switch S_1 is in ON mode, inductor L_1 will be charged through this switch by the DC source and L_2 will be charged by Capacitor C_2. Where the switch S_2 is in ON mode, both inductors turn into sources. The output voltage on the load side will have a positive value for these values of the duty cycles. In the second state (0.5<D<0.667), when the switch S_1 is conducted, both of the inductors operate as sources and thus, C_1 and C_2 will be charged and for the time interval when the switch S_2 is in ON mode, input DC voltage source and capacitors will charge the inductors again and the output voltage on load will be negative.

For the steady-state analysis of a quasi Z source inverter, the voltages on capacitors C_1 and C_2 have been taken as V_{C1} and V_{C2} respectively. Furthermore, the direction of voltages on capacitors and currents for the inductors has been taken into account based on Figure 2.

The steady-state calculations have been carried out depending on capacitor charge balance and inductor voltage-second balance principles. For the inductor L_1, in a time period we can have:

$$V_{C1} \times D + (V_{C2} - V_{in}) \times (1 - D) = \int_0^{T_S} V_{L1} \times dt = 0 \quad (1)$$

where the same principle is considered for the inductor L2:

$$V_{in} \times D + (V_O - V_{C1}) \times (1 - D) = \int_0^{T_S} V_{L2} \times dt = 0 \quad (2)$$

From these equations, the following equation can be obtained:

$$V_{C1} = V_{in} \quad (3)$$

$$\frac{V_O}{V_{in}} = \frac{1 - 2D}{1 - D} \quad (4)$$

And, based on the capacitor charge balanced principle for the capacitors C_1 and C_2 in a time period, the following equation is provided:

$$V_{C1} = \frac{D}{1 - D} V_{in} \quad (5)$$

$$I_{L2} = -I_O \quad (6)$$

$$I_{L1} = -\frac{D}{1 - D} I_O \quad (7)$$

By having a sinusoidal voltage in load side of the inverter as (8):

$$V_O = V \sin \omega t \quad (8)$$

The modulation index can be found as:

$$M = \frac{V}{V_{in}} \quad (9)$$

By substituting the equations (8), (9) into (4), the duty cycle of the switch M_1 can be obtained as:

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \quad (10)$$

As stated earlier, only one of the power MOSFETs will be in ON sate at the same time, thus the duty cycle of the second switch shall be as follows:

$$D' = 1 - D = \frac{1}{2 - M \sin \omega t} \quad (11)$$

Considering the same phases for the output current and voltage waveforms, for the duty cycle D=0.667 and modulation index M=1 and $\omega t = 3\pi/2$, the maximum current and voltage on switch S_1 will be equal to three times of input current and voltage respectively.

For both ON and OFF states of the switch, we can obtain the voltage and current signals of the switch S_1 from the equations below:

$$I_O = I \sin \omega t \quad (12)$$

$$V_S = V_{in} + V_C = \frac{1}{1 - D} V_{in} = (2 - M \sin \omega t) V_{in} \quad (13)$$

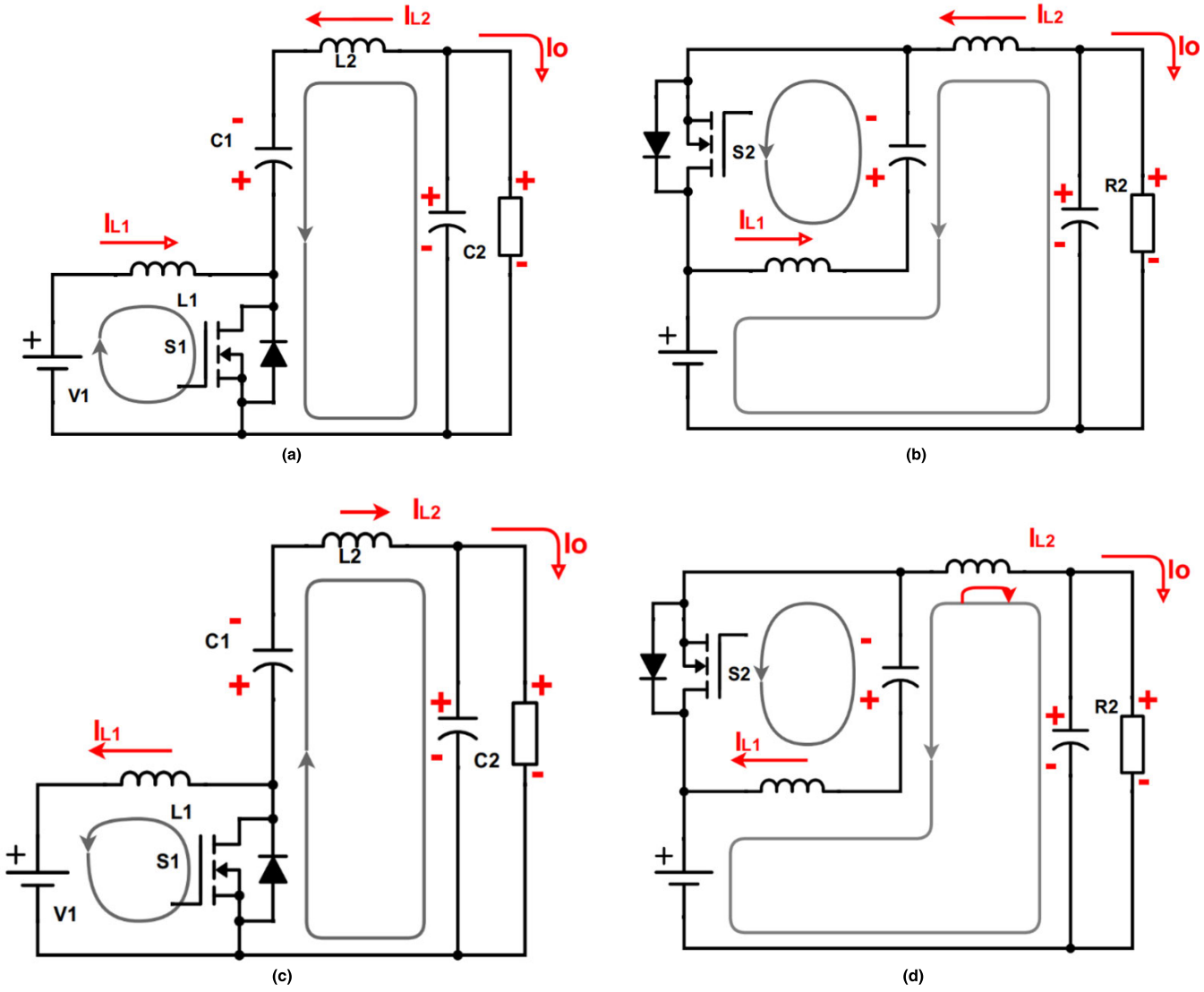


FIGURE 2. QZSI operation mode for (0<D<0.5), when switches (a), (c) S1 and (b), (d) S2 conduct.

$$I_S = I_{L1} + I_{L2} = -\frac{1}{1-D} I_O = -(2\sin\omega t - M(\sin\omega t)^2) I \tag{14}$$

The voltage and current of the switch S_1 for both off and on sates based on (13) and (14) are shown in Figures 3(a) and (b).

The voltage on capacitor C_1 can be derived through (5) and (10) as follows:

$$V_{C1} = \frac{D}{1-D} V_{in} = (1 - M\sin\omega t) V_{in} \tag{15}$$

The graphical illustration of this equation is shown in Figure 4(a). It is clearly observed that the maximum voltage on capacitor C_1 is $2V_{in}$ which occurs when the duty cycle is 0.667 and angular frequency is ωt=3π/2. The graphical behavior of the inductor L_1 current is presented in Figure 4(b).

$$I_{L1} = -\frac{D}{1-D} I_O = -(\sin\omega t - M(\sin\omega t)^2) I_{in} \tag{16}$$

The graph demonstrates that the maximum current of the inductor is $2I_{in}$ when the duty cycle is 0.667 and ωt=3π/2 too. So as can be understood, these values of duty cycles and angular frequency are critical for this converter.

The voltage and current fluctuations for the capacitor C_1 and inductor L_1 can be obtained from (17) and (18):

$$\Delta V_{C1} = \frac{(1-D) T_S I_{L1}}{C_1} = \frac{-\sin\omega t + M(\sin\omega t)^2 T_S I}{(2 - M\sin\omega t) C_1} \tag{17}$$

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{in} T_S D}{L_1} = \frac{V_{in} T_S (1 - \sin\omega t)}{L_1 (2 - M\sin\omega t)} \tag{18}$$

The same solution can be applied to obtain the same equations for C_2 and L_2.

The component selection process should be carried out based on these graphics and equations.

For example, for capacitors the equations (15) and (17) should be considered based on the peak ripple requirement of the voltage through Figure 4a and in the same way,

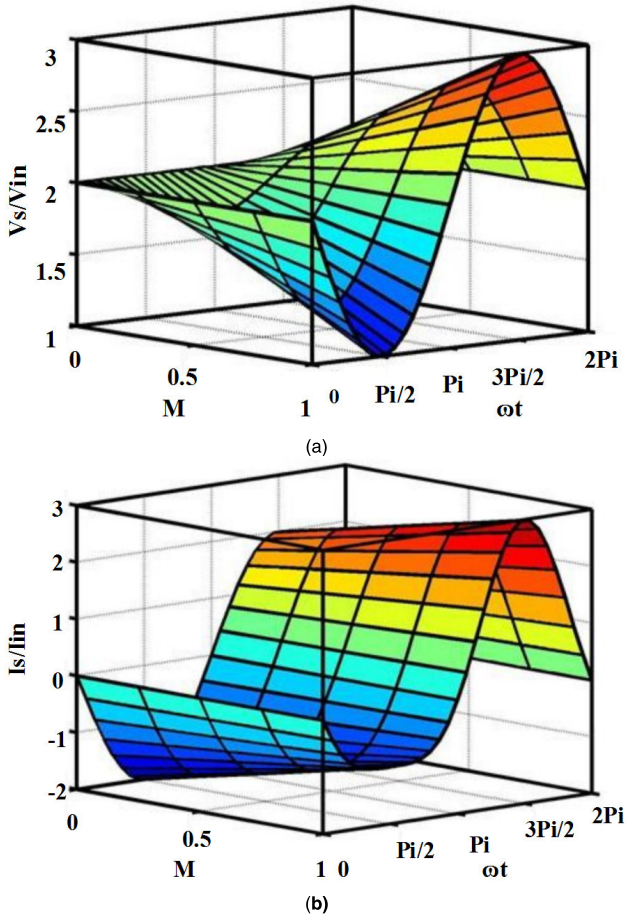


FIGURE 3. (a) OFF state, (b) ON state of the switch S1.

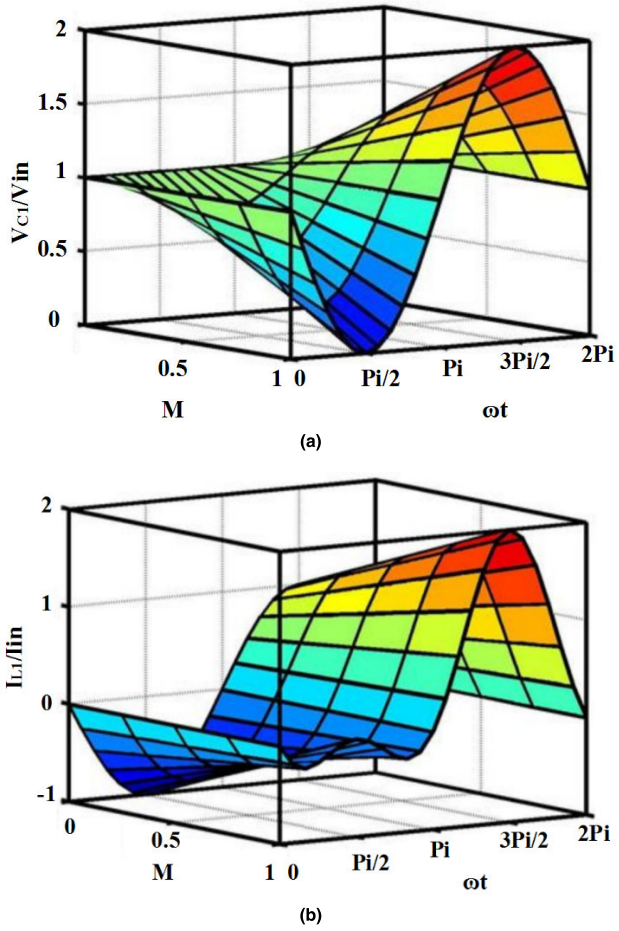


FIGURE 4. Voltage on (a) capacitor C1 and (b) current through inductor L1 for different work-conditions.

the inductors can be chosen through (16) and (18) and Figure 4b. Therefore, in the worst condition in the one-phase mode and heavy loads with adding in three steps, by considering a 15 A ripple from the positive peak to negative peak for the currents of the inductors, with 150 V as input voltage, D=0.667 and 50KHz as the switching frequency through (18), the values of the inductors will obtain $L_1 = L_2 = 130\ \mu$H.

Also, by 30% of ripple for C_1 and 3% for the C_2 as the output capacitor, the C_1 and C_2 will obtain 1μF and 10μF through (17), respectively.

The experimental results of simulation have been given based on these components' values obtained after a mathematical analysis.

The conventional SPWM techniques are carried out based on (10).

As the quasi Z-source inverter's voltage waveform is non-linear, the reference wave can be rewritten as follows:

$$D = \frac{1 - |M \sin \omega t|}{2 - |M \sin \omega t|} \tag{19}$$

$$D' = \frac{1}{2 - |M \sin \omega t|} \tag{20}$$

D and D' represent the duty cycle values for switch S1 and S2, respectively. Figure 6(a) and (b) show the conventional and proposed SPWM waves and the generated pulses through these equations, respectively.

Figure 6(b) represents D' (PWM signal for switch S_2), while figure 6(a) is based on equation (10) and for the switch S_1.

Through the comparison of these two equations, the main advantage of the proposed controller equation is it is much simpler to conduct.

The results for one-phase and two-phase converters were added here. Figures 7 and 8 present the one-phase and two-phase structure of the QZSI along with the proposed controller. In the one-phase approach, as shown in Figure 7(a), the output of the converter is connected to the FBI block to generate a pure sinusoidal voltage wave. The FBI side can include different loads that will be added to the system's output nodes in desired times. These loads can be seen in this Figure. Figure 7(b) shows the proposed controller and can be compared with (20).

Through the proposed two-phase Z-source topology and the adjustment of the modulation index for per phase and by making a change on the input voltage V_{in}, the output voltage magnitude will be fixed.

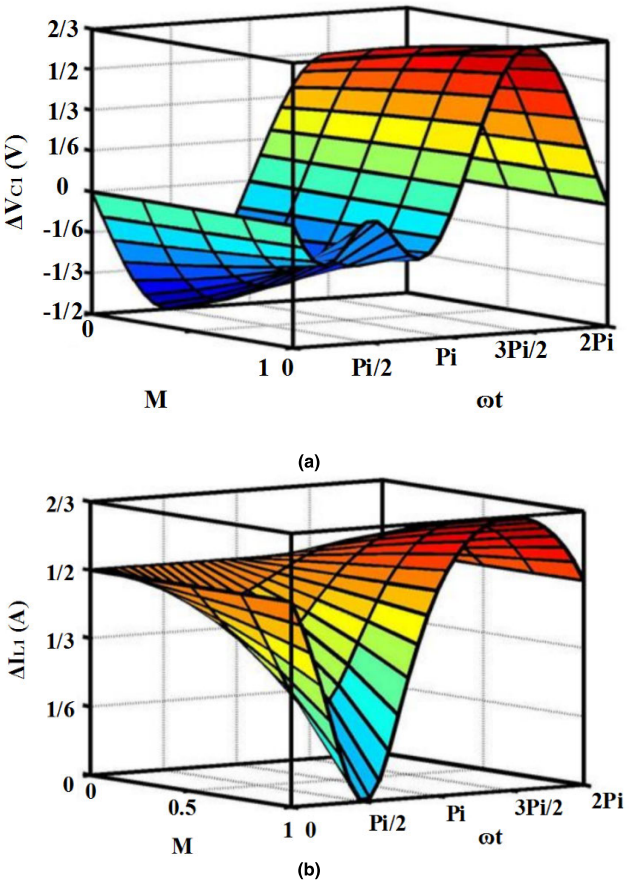


FIGURE 5. Voltage ripple on (a) capacitor C1 and (b) current ripple of the inductor L1.

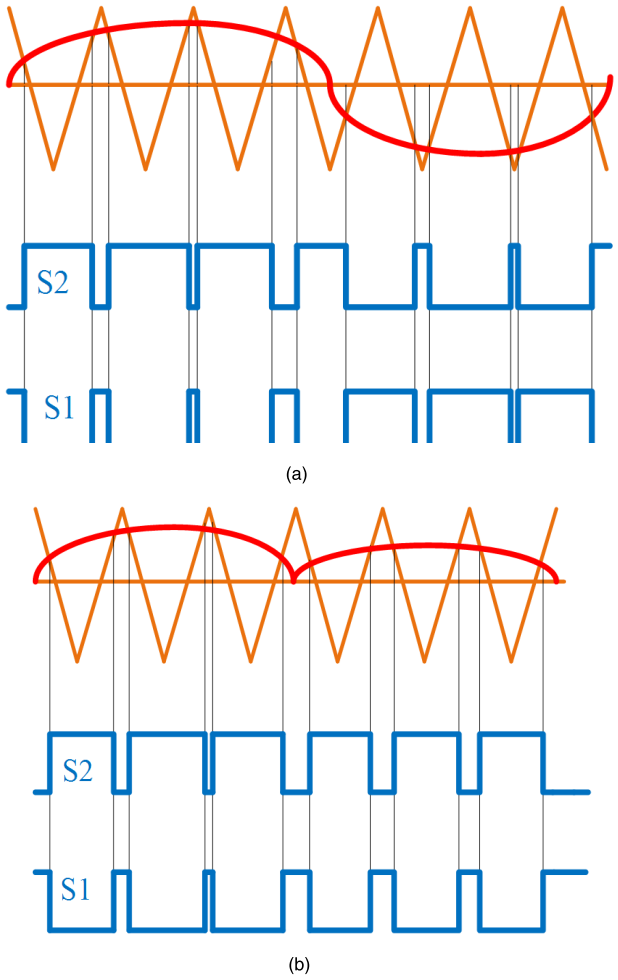


FIGURE 6. (a) Conventional and (b) proposed SPWM.

As discussed previously, in the two-phase approach, one of the outputs is a positive rectified sinusoidal wave while another block generates a negative voltage.

Thus, the phase difference between these two blocks will equal to π. If V1 and V2 show the output voltages of these blocks respectively, the following equation can be obtained on the load side through Figure 8(a):

$$V_1 = |V \sin(\omega t)| \tag{21}$$

$$V_2 = -|V \sin(\omega t + 180)| \tag{22}$$

$$V_{12} = V_{ac} = V(|\sin(\omega t)| - |\sin(\omega t + 180)|) = 2V\,|\sin(\omega t)| \tag{23}$$

III. SIMULATION RESULTS

The simulation results for one-phase and two-phase approaches based on the presented mathematical analysis in section 2 are shown in Figure 9. A 220 V AC and a 440 V AC peak to peak output voltage are planned to be obtained for the one-phase system and the two-phase system, respectively.

Based on Figures 7(a) and 8(a), for both approaches, three parallel loads have been added to the FBI side in specified times to assess the controller's ability to generate different values of the currents.

During the first step of the simulation, converters are considered to work with a load by 190 W, resistive active load and by 50VAR as the inductive reactive load through MATLAB/SIMULINK. At the t = 0.25 and 0.45 Sec, the second and third loads with the same values are added to the output ends along with an analysis of the performance of the converter.

As shown in Figure 9(a) and (b), the expected 220 and 440 V AC voltages have been obtained in the output nodes of the converter. Figures 9(c) and (d) confirm that the current will increase if the second and third loads are added. The critical feature of the controller is that no change is observed in voltage waveforms when the loads are added to the output. Another important point is the current levels for the two-phase system, and as can be seen, it is half of the current for the one-phase system as is expected. Figures 9(g) to (l) illustrate the current waveforms for the inductors. All these figures can easily support our ideas related to the (18) and all sentences related to this equation for components' values.

Also, Figures 10(a) and (b) illustrate the controller's ability to activate and deactivate the power switches for the QZSI block. As can be seen in per time interval,

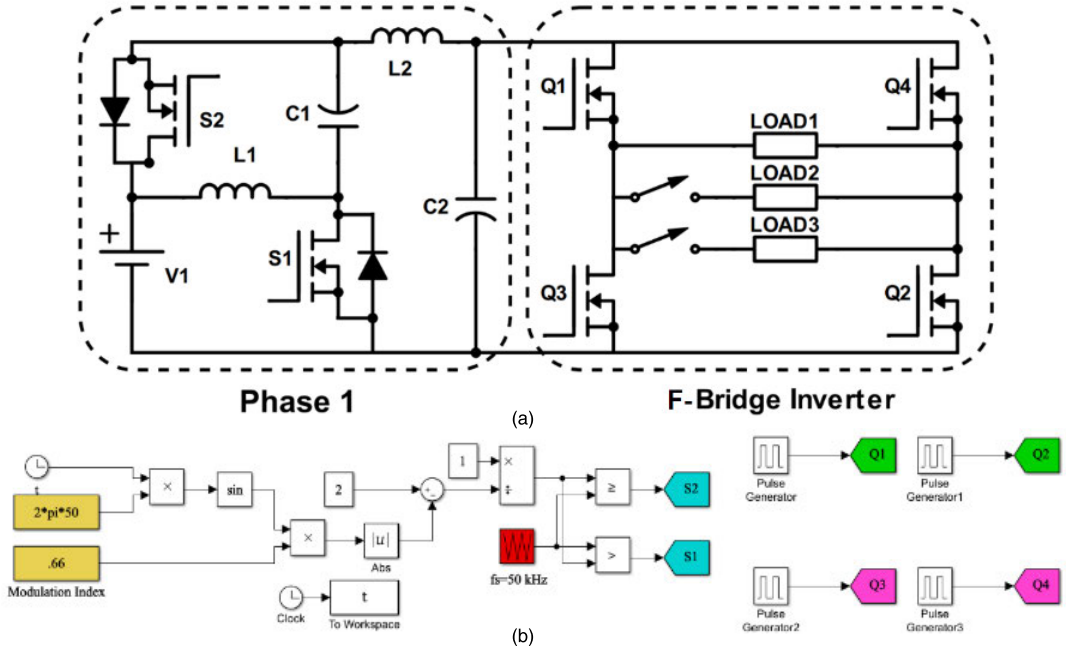


FIGURE 7. (a) Connection between QZSI and FBI and (b) controller schematic.

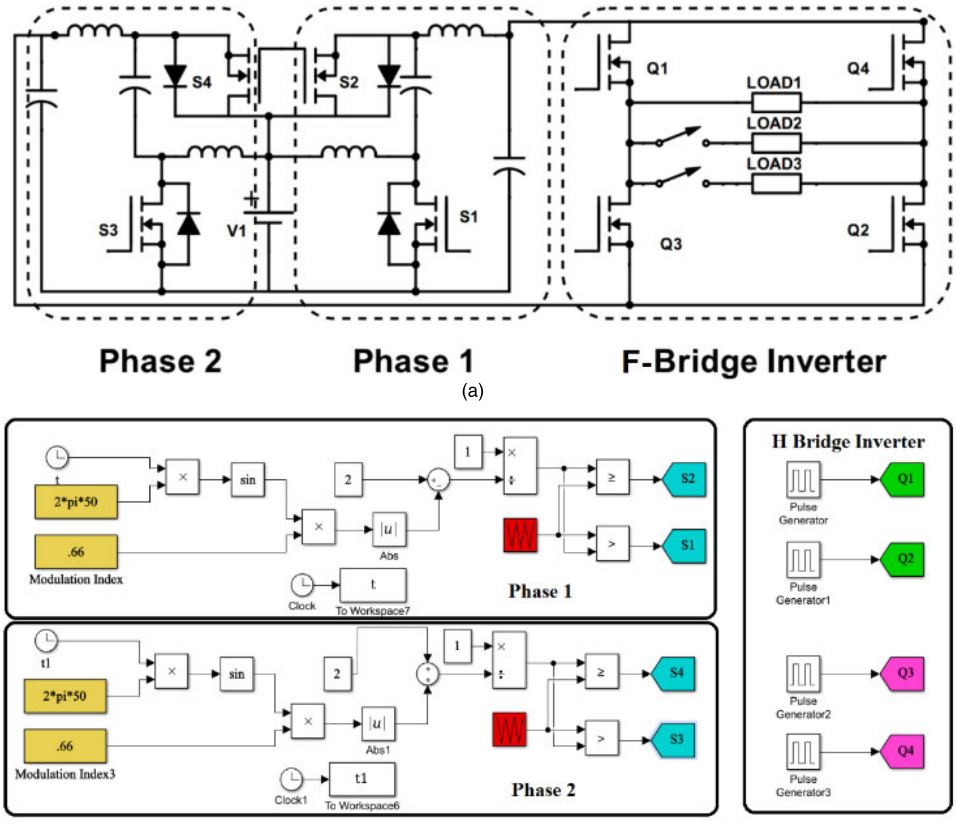


FIGURE 8. (a) Connection schematic for the two-phase QZSI and FBI block. (b) Proposed controllers.

only one of the power MOSFETs will receive the pulses in gate-source pins. Under the projected ISPWM, the output voltage on the load side has an acceptable THD as shown in Figures 10(c) and (d). As has been reported in section 1,

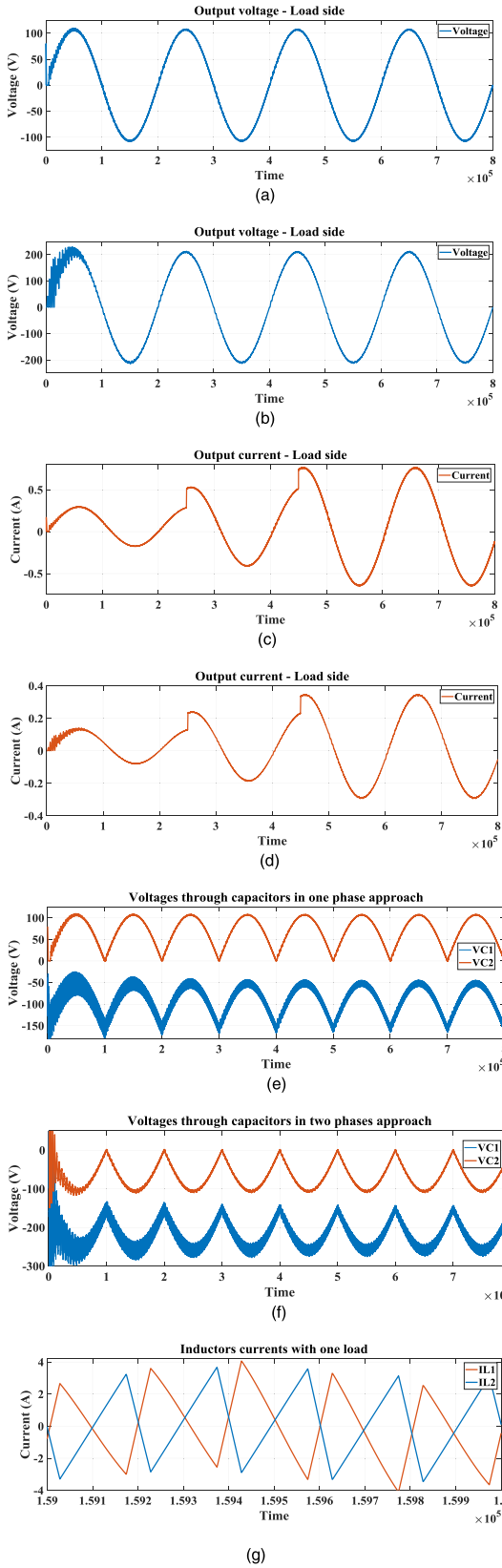


FIGURE 9. **Simulation results for one-phase and two-phase systems. (a) and (b) output voltages, (c) and (d) output currents, (e) and (f): voltages on capacitors, currents through inductors with (g), (h): one load, (i), (j): two loads and (k), (l): three loads.**

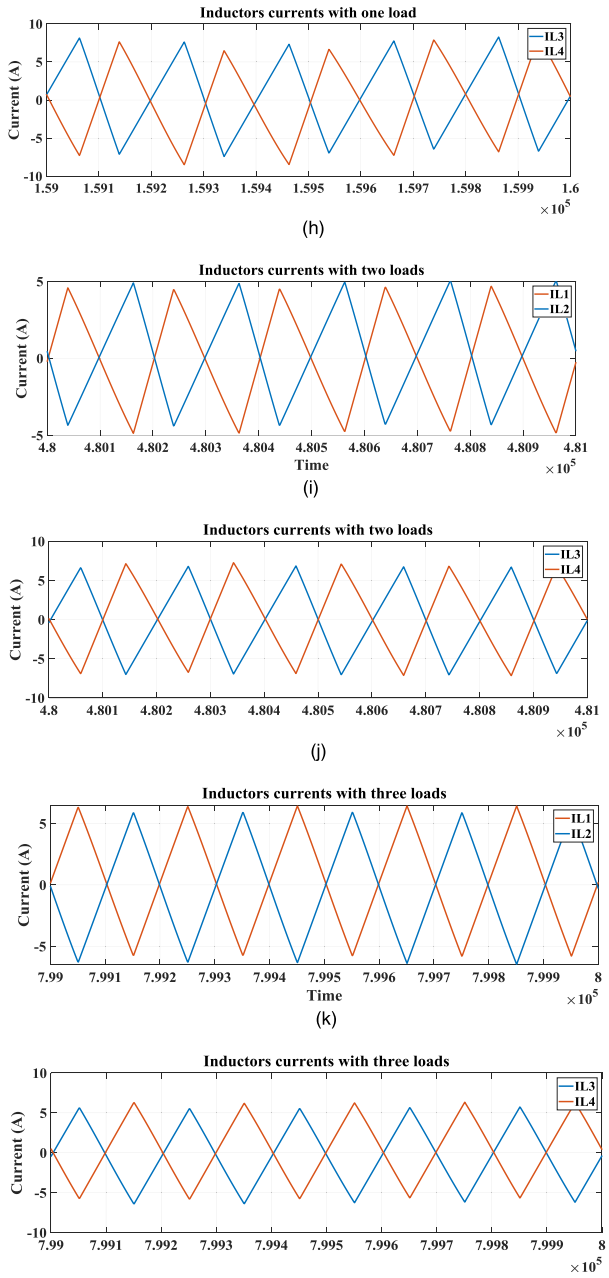


FIGURE 9. ***(Continued.)*** **Simulation results for one-phase and two-phase systems. (a) and (b) output voltages, (c) and (d) output currents, (e) and (f): voltages on capacitors, currents through inductors with (g), (h): one load, (i), (j): two loads and (k), (l): three loads.**

there have been a great number of studies that show converters with a THD value ranging between 3-5 %. Therefore, the performance of this controller can be assessed especially for the two-phase system. This reveals that for multiphase systems, the lower amount of THDs can be obtained. Figure 11 shows a comparison for the quality assessment for the obtained voltage and current waves between the proposed ISPWM and the method is presented in [24]. The extended prototypes of [24] can be found in references [25]–[29].

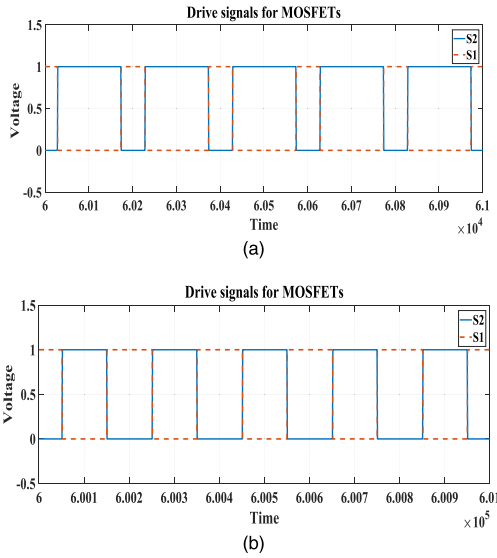


FIGURE 10. Generated PWM by proposed controller for (a) one-phase and (b) two-phase system. Obtained THD values for the (c) one-phase and (d) two-phase system.

This comparison was conducted to achieve a 660 V AC peak to peak voltage with about 2A of load current in the one-phase approach. By considering the 50 Hz for the output voltage and current signals, a small collation confirms the performance of the proposed controller especially at the zero points and its ability to show a pure sinusoidal signal without over or undershoots.

IV. FAILURE RATE CALCULATION

Reliability analysis is carried out for any system to evaluate the ability of components in the circuit that work under

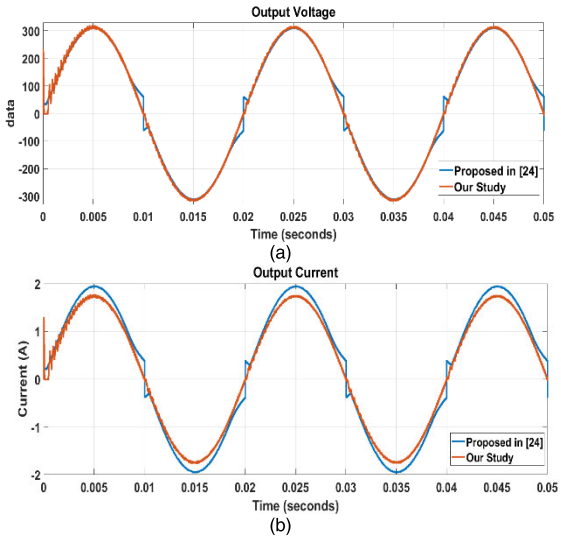


FIGURE 11. The quality of the (a) voltage and (b) current signals in the proposed and one's presented in [24].

different conditions in a specific time duration. Environmental factors such as humidity and temperature can be some of these conditions. Based on [30], there are specific equations per electronic component that can give the failure life of that component. Finally, all failure lives should be collected to give the Mean-Time to Failure for the system. All equations and calculations for the reliability tests are given in this section.

A. CAPACITORS

Capacitor parameter can be obtained from (24):

$$\lambda_P = \lambda_b \pi_{CV} \pi_Q \pi_E \, failures/10^6 h \tag{24}$$

In this equation, λ_p refers to the failure life of the capacitor. The thermal life of a capacitor π_b can be obtained from (25) and the π_{CV}, π_Q and π_E refer to the temperature, quality and environmental factors, respectively.

$$\lambda_b = 0.00115 \left[\left[\left(\frac{S}{0.4} \right)^5 + 1 \right] \exp\left(2.5 \frac{(T+273)}{358}\right)^{18} \right] \tag{25}$$

where, S:

$$S = \frac{Operating\ Voltage}{Rated\ Voltage} = \frac{VDC + \sqrt{2} V_{ac\,rms}}{V_{DC\,rated}} \tag{26}$$

For S = 0.1 and T=70°C, the λp will be equal with 0.00037. Since two capacitors with 1 and 10μF values are used in the structure, with $\pi_{CV} = 1.4C^{0.12}$ [30], this factor will be obtained as 0.26676 for the capacitor C=1μF and 0.35166 for the capacitor C = 10μ. π_Q and π_E have been considered equal with 10 for the fixed ground and unknown screening level for the converter. Thus, for the failure life for both capacitors can be gained from (27):

$$\lambda_P = \begin{Bmatrix} 0.00037 \times 0.26676 \times 10 \times 10 = 0.00987 \, for\ C = 1\mu F \\ 0.00037 \times 0.35166 \times 10 \times 10 = 0.01301 \, for\ C = 10\mu F \end{Bmatrix} failures/10^6 h \tag{27}$$

B. INDUCTORS

For an inductor, this parameter can be obtained from (28):

$$\lambda_P = \lambda_b \pi_C \pi_Q \pi_E \, failures/10^6 h \tag{28}$$

And the λ_p is obtained from (29):

$$\lambda_b = 0.000335 \left[\exp(2.5 \frac{(T_{HS} + 273)}{329})^{15.6} \right] \tag{29}$$

T_{HS} in (29) is the temperature of the inductor's hot-spot according to (°C) and is presented in (30):

$$T_{HS} = [T_A + 1.1(\Delta T)]^\circ C \tag{30}$$

ΔT represents the average temperature rise in the environment. For the temperature 75°C, the λ_b will be equal with 0.0023, where for a 130 μH inductor, the π_C is 1.0, π_Q and π_E are equal with 3.0 and 6.0, respectively. Thus, for our proposed inductors, the failure life can be obtained as:

$$\lambda_P = \{0.0023 \times 1 \times 3 \times 6 = 0.0414 \ for \ L = 130\mu H\} \\ failures/10^6 h \tag{31}$$

C. POWER MOSFETS

Power MOSFET's failure life can be presented in (32):

$$\lambda_P = \lambda_b \pi_T \pi_Q \pi_E \, failures/10^6 h \tag{32}$$

The base failure rate λ_b is 0.0083 for a power MOSFET. The unknown parameter in this equation is the π_T, that is the thermal factor for this component and can be calculated from (33):

$$\pi_T = \exp \left[-2489 (\frac{1}{T_j + 273} - \frac{1}{298}) \right] \tag{33}$$

For Tj=75°C, π_T is equal with 3.0, where for this device, by a fixed grounded and commercial quality, π_Q and π_E will be equal with 5.5 and 2.0, respectively. Thus, the failure rate of this component will be:

$$\lambda_P = 0.0083 \times 3 \times 5.5 \times 2 = 0.2739 \ failures/10^6 h \tag{34}$$

D. MTTF CALCULATION FOR SYSTEM

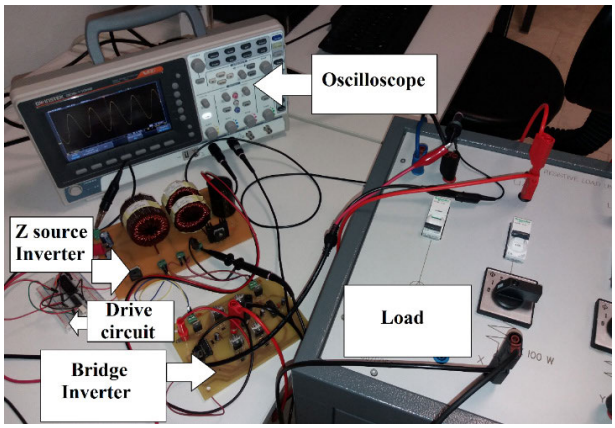
The failure rate for the system can be obtained by adding the failure rate of all components:

$$\lambda_{CONVETER} = (2 \times \lambda_{MOSFET}) + (\lambda_{C_1} + \lambda_{C_2}) + (\lambda_{L_1} + \lambda_{L_2}) \\ = 0.65348 \, failures/10^6 h \tag{35}$$

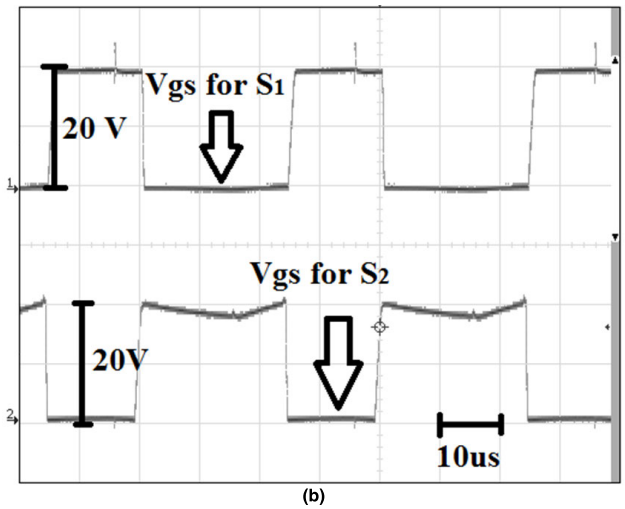
The Mean-Time to Failure (MTTF) is calculated from (36) for this converter:

$$MTTF = \frac{1}{\lambda_{CONVERTER}} \, hours = 1530268 \, hours \tag{36}$$

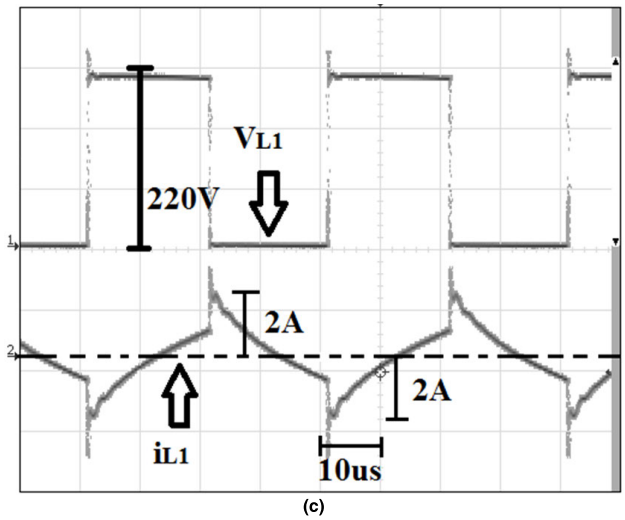
The obtained value is considerable for an electrical circuit.



(a)



(b)



(c)

FIGURE 12. (a) hardware prototype, (b) Gate-Source voltages for S1 and S2 power switches in Z-source side, (c) voltage and current waveforms for L1.

V. EXPERIMENTAL RESULTS

The theoretical and simulation results are planned to be confirmed after A 300W laboratory prototype is tested. The same value of the components for the capacitors and inductors is

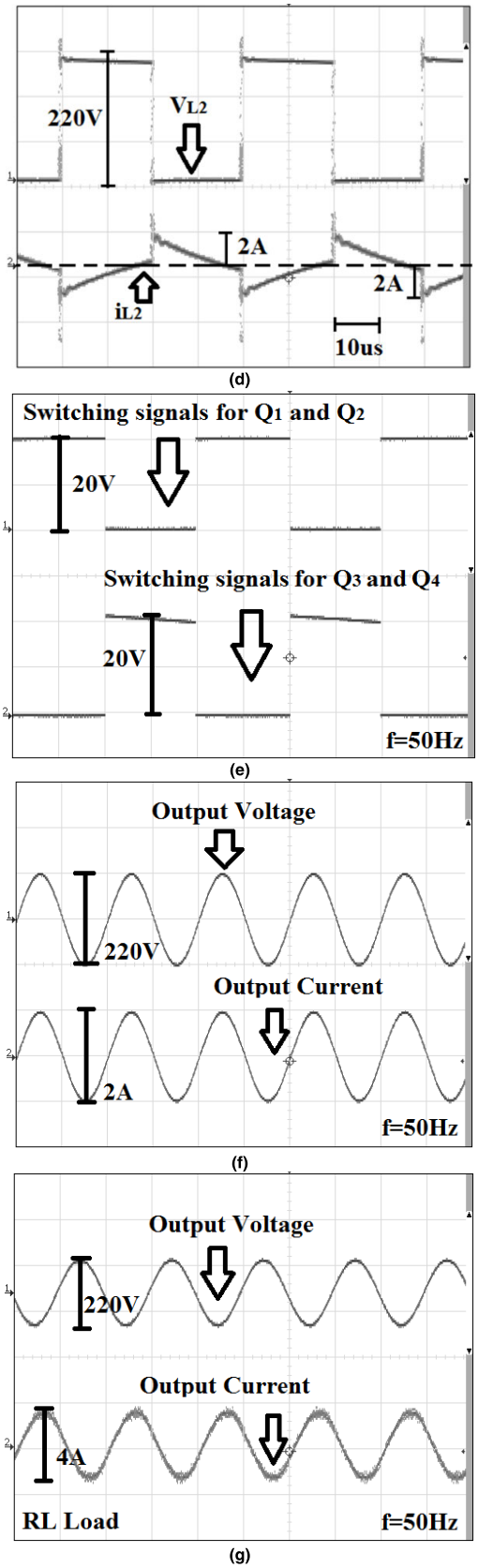


FIGURE 12. *(Continued.)* **(d) voltage and current waveforms for L2, (e) switching signals for bridge side, (f) output voltage and current waveforms for bridge side under R and (g) RL loads.**

selected through the use of two 75 Ω loads. Figure 12 presents the experimental results for our proposed converter.

Figure 12a illustrates the implemented prototype. Figure 12b shows the gate-source voltages for power switches of the Z-source converter. The state of the switches easily can confirm the theoretical conditions.

Based on these terms, when one of the switches is activated another one goes to the OFF state and vice versa. This figure shows that the switching circuit easily can generate these contradictory signals. Figures 12c and 12d present the voltage and current signals on the inductors L_1 and L_2 respectively.

These figures can confirm many of the equations especially (6), (7) and (16).

Figure 2 presents the state of the output voltage for the Z source inverter in both CCM and DCM working conditions. Since the Continuous Conduction Mode is analyzed in this study, the blue cure in this figure should be considered. Since for the modulation index M=0.667, a signal with gain $G = -1$ can be obtained, this value will be selected for power switches in Z-source inverter side. for obtaining the higer gains, this index can be changed based on figure 2.

Based on our selected modulation index (M=0.667), the same voltages on input and output sides are expected. So, based on the charge and discharge processes of the inductors, the voltage on these inductors changes between input DC voltage and zero. Also, because of the inherent behavior of the inductors, triangular current waves are expected to flow through the inductors.

Figure 12e shows the switching signals for the bridge inverter side and can guarantee that in per time interval, one pair of power MOSFETs on this side can be activated in order to obtain a full sinusoidal voltage and current waveforms on the load side.

During the first step, a 220 V AC peak to peak voltage with 50Hz frequency was obtained with a 75 Ω resistive load. This state can be tracked through figure 12f. Since the RMS value of this voltage is around 157 V, a 2 A as the RMS current obtained for this resistance that meets our expectations. Furthermore, when the second load with the same value is applied, this current is received to 4 A RMS showing that the total resistance at the load side is received around 37 Ω. This state is shown in figure 12g. Also, a small inductor with 10μH inductance value is considered to be series to this Resistive load. So, as can be seen, a phase difference can be reported by this figure.

VI. CONCLUSION

An improved SPWM technique for QZS based inverters has been proposed in this study. Connecting this structure to the FBI block has advantages such as lack of need to the harmonic limiter circuits and the ability to generate a pure sinusoidal voltage and current waveforms for the load side. In this study, 0.88% and 1.34 % of the THD have been reported for two-phase and one-phase systems, respectively. The performance of the controller clearly reveals that only

one of the power MOSFETs can be conducted at the same time depending on the work condition of the QZSI. Obtaining the higher gains is possible by applying the higher modulation indexes for the power switches in the Z Source inverter side. All mathematical analyses were presented and components values were selected based on these equations. A group of simulations has been conducted to obtain the voltage on the capacitor C_1 and current value passes through inductor L_1. The ripple values for these parameters are presented by curves based on mathematical proofs as well as voltage and current stresses on the power switch S1 illustrated.

The Mean-Time to Failure (MTTF) analysis is conducted to calculate the long life of the circuit under 70°C to 75°C which is not a normal working temperature for the components to force the elements for the reliability analysis. A very good result has been found. Besides, the same values have been used for the simulation and application to confirm the theoretical results. A 300 W laboratory prototype was implemented and the related results were presented.

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