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# Dual Lumped Ports Technique and Its Applications in Modeling of Planar Schottky Diode in THz Band

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**ABSTRACT** Micro-coaxial probe technique (MCPT) is widely used in three-dimensional electromagnetic (3-D EM) modeling of planar Schottky barrier diodes (SBDs) for the design of terahertz multipliers and mixers. However, the inconsistency of port numbers between 3-D EM model and intrinsic model of diode has been pending for years due to the lack of alternative internal port techniques. In this paper, after investigating port techniques available for field simulation software, a novel dual lumped ports technique (DLPT) is proposed to replace the MCPT for removing its non-physical grounding requirement, which makes the defined internal ports have definite physical meaning. Moreover, the proposed DLPT possesses higher accuracy than MCPT for the elimination of epitaxial layer penetration and additional consideration of port coupling effect. Detail technical procedures for DLPT are presented for internal double ports implementation. To verify its feasibility and accuracy at terahertz band, a 110 GHz broadband tripler was designed utilizing the proposed DLPT and the measured results agree well with the simulated ones. Furthermore, a series of frequency multipliers designed by MCPT are post-analyzed with the same models derived from DLPT. Finally, a slight discrepancy is observed between MCPT and DLPT, and the latter coincides better with the measured results. All these results indicate that the proposed DLPT is validated to be effective and accurate for the design of diode frequency multipliers and mixers in terahertz region.

**INDEX TERMS** Micro-coaxial probe technique, dual lumped ports technique, 3-D EM model, schottky barrier diode, diode modeling, frequency multipliers, mixers, terahertz.

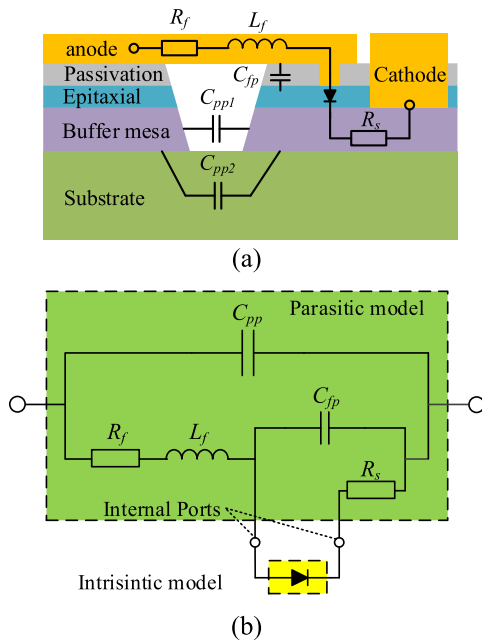
## I. INTRODUCTION

Terahertz technology has great potential applications such as broadband communication, precision guidance, atmospheric physics, radio astronomy, object imaging, remote wireless sensing, biological spectroscopic instruments [1], [2]. Many space-based instruments, security check systems and planetary observation platforms have been successfully developed with THz heterodyne receivers. Found in many terahertz components and systems, Schottky barrier diode (SBD) continues to be the most popular THz device. As a low-parasitic device that works well into terahertz region at room-temperature, Schottky diodes can provide substantial capabilities of power generation, signal detection and frequency conversion for a range of practical THz applications [3]. Examples including mixers that work up to 3.2 THz [4]

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and frequency multipliers that work up to 2.7 THz [5] have been demonstrated successfully. The development of these components benefits from the advances of diode manufacturing technology [6], modeling technology [7], circuit design method [8] and block manufacturing technology [9].

The design of frequency multipliers and mixers working in THz region relies on accurate diode models, which are still under investigation and development to improve the generality and accuracy. When the frequency rises to millimeter wave and terahertz band, the package structure of diode will introduce great geometry dependent parasitic parameters, as shown in Fig. 1(a). The circuit performance would have been deteriorated consequently if these parasitic parameters didn't be taken into consideration. According to the parasitic topology, a small signal lumped equivalent-circuit (LEC) model, including parasitic model and intrinsic model, can be established in Fig. 1(b). The LEC model needs to determine appropriate lumped elements' values by curve fitting in the



**FIGURE 1. Planar Schottky diode structure. (a) Cross-sectional view; (b) Small signal lumped equivalent-circuit model.**

required frequency band [10], [11]. However, this method is limited by the practical measured frequency range. Moreover, for some special high frequency effects, such as eddy current effect [12] and skin effect, the LEC model lacks of accurate characterization.

Physical-based numerical model [13], also named as 3-D EM model, was proposed for higher accuracy and better generality of diode model. Unlike the LEC model, the 3-D EM model characterizes the high frequency parasitic effects induced by complex passive structures around the Schottky junction by finite element method (FEM). In order to extract the embedding impedance at the reference plane of Schottky diodes, a micro-coaxial probe is inserted at the exact location of each Schottky junction and a wave port is assigned at the end of the coaxial probe, as described in [14]–[16]. Then, the simulated results are imported as scatter matrix into Agilent Advanced Design System (ADS) for further combination with the intrinsic model of diode. Finally, harmonic balance simulation is executed to predict the nonlinear behavior of diodes. This method has become a general modeling technique for SBDs, and is widely used in the design of terahertz Schottky diode multipliers [17]–[23], mixers [24]–[29] and detectors [30]–[31].

However, when combining the S parameters with the intrinsic SPICE model of the diode, one will encounter an issue that the port numbers between 3-D EM model and intrinsic model of diode is inconsistent. This dilemma is caused due to the fact that there is only one port defined at each Schottky junction while the diode is intrinsically a two-terminal device. The classical solution is to introduce a grounding path, i.e. one port of the intrinsic model connects to the defined internal port of 3-D EM model while the other

port connects to ground, as presented in [29]. Then it results in an inconsistency with the actual connection approach of diode compared with Fig. 1(b), where the diode is embedded in series from the anode to the cathode, rather than parallel to the ground. Based on the classical MCPT and non-intuitive grounding solution for diode, the measured results from great numbers of successful demonstrations are considered to be close to the simulated ones. However, such a grounding path doesn't exist in the actual diode chip and such internal port setting can't distinguish the anode port and the cathode port due to lacking of definite physical meaning, which may lead to wrong phase relationship if one of the intrinsic models is embedded into 3-D model in a wrong polarity. In addition, the accuracy of MCPT used for diode modelling is still questionable for the MCPT approach will modify the geometry near the junction, which can lead to inaccuracies in modeling the impedance of diodes.

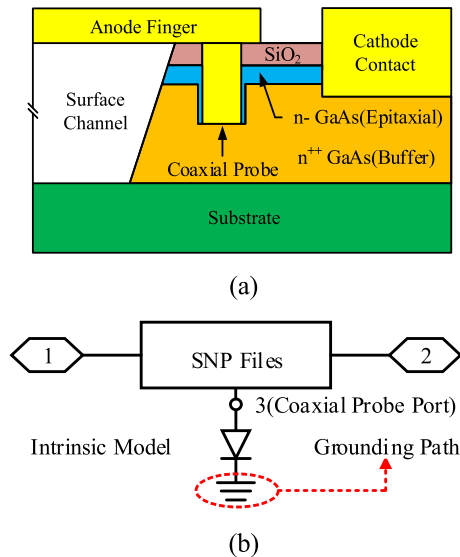
In this paper, a novel DLPT is proposed to replace MCPT for solving the problem mentioned above. Theoretical analysis and modeling methods for different internal port techniques are introduced and compared in detail. To verify its feasibility at terahertz band, a series of frequency multipliers are designed and post-analyzed based on the proposed DLPT. The final results are compared and discussed. This paper is organized as follows: different internal port techniques for 3-D EM modeling of planar SBDs are presented in Section II, which is followed by an experimental demonstration of the proposed DLPT by a 110 GHz tripler in Section III. The feasibility and accuracy of the DLPT for general frequency multipliers are discussed in Section IV, and conclusions are given in Section V.

**II. METHODS**

Internal port technique is one of the key technologies of 3-D EM modeling method, which provides the basis for the modeling of the intrinsic and non-intrinsic parts of diode separately. In order to overcome the defects of traditional MCPT, a novel DLPT is proposed in this paper. To the best of the author's knowledge, this novel port technique is proposed for 3-D EM modeling of diode for the first time in the literature. This section is devoted to giving a detailed introduction of these two internal port techniques and comparison of intrinsic model embedding methods for 3-D EM modeling of diode.

**A. MICRO-COAXIAL PROBE TECHNIQUE (MCPT)**

3-D EM model of diode based on MCPT was proposed by J. L. Hesler in 1996 when designing terahertz harmonic mixers [14]. This method needs to establish the three-dimensional physical model of package according to the electromagnetic characteristics of diode layer structure accurately in the field simulation software such as High Frequency Structure Simulator (HFSS). Since HFSS doesn't support enclosed wave ports, a coaxial probe technique was proposed in the process of diode modelling. As depicted in Fig. 2(a), the anode probe penetrates through the epitaxial layer and continues to extend into the buffer layer to set an internal wave port at the end of



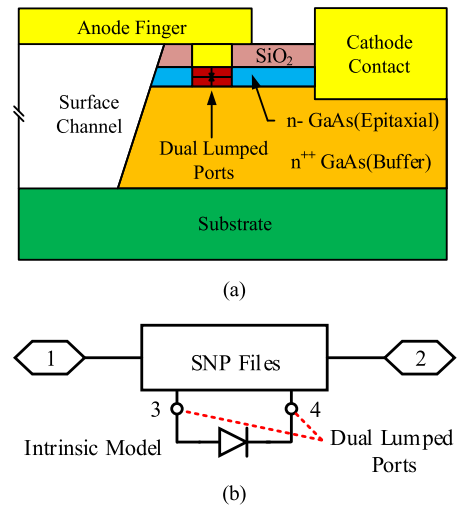
**FIGURE 2.** MCPT and diode embedding method. (a) Cross-sectional view of MCPT; (b) 3-D EM model of diode based on MCPT (Port 3 represents coaxial probe port).

the probe. Thanks to the high conductivity of the buffer layer due to heavy doping, the internal wave port at the Schottky junction can be supported by assigning the buffer layer as PEC material. In addition, a suitable de-embedding distance for the wave port is needed to push the reference plane to the boundary between the epitaxial layer and the buffer layer.

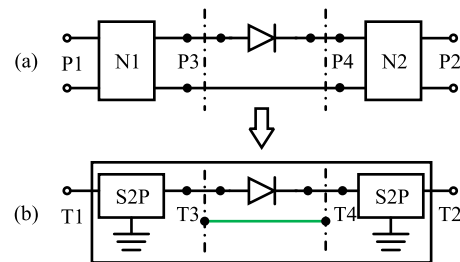
The coaxial probe port can be used not only to simulate the linear part of diode and extract the parasitic effects, but also to provide an interface connecting the linear parasitic part and the non-linear intrinsic part of SBDs. However, since only one port is set at the Schottky junction, only one end of the intrinsic model of the diode can be embedded in the 3-D EM model while the other end is connected to the ground, as shown in Fig. 2(b). This model is in conflict with the small signal LEC model shown in Fig. 1(b), in which the diode intrinsic model is connected in series between the anode and the cathode rather than parallel to the ground. Considering this dilemma, a dual-port technique at the Schottky junction has always been expected in order to embed the intrinsic model of diode in a natural way. Besides, the discrepancy caused by the geometry modification near the junction should be corrected to improve the accuracy of the 3-D EM model, especially when frequency rises up to terahertz region.

**B. DUAL LUMPED PORTS TECHNIQUE (DLPT)**

On the basis of investigating port techniques available for field simulation software, a novel DLPT at the Schottky junction is proposed to realize the natural embedding of intrinsic model of diode in 3-D EM model. Unlike the MCPT, the DLPT doesn't require the anode to penetrate the epitaxial layer anymore, but only needs to insert two adjacent rectangular sheets into the gap (epi layer) between the anode and the buffer layer, and assign as lumped ports with integral line pointing to each other. As depicted in Fig. 3(a),



**FIGURE 3.** DLPT and diode embedding method. (a) Cross-sectional view of DLPT (Red rectangle sheets represent lumped ports with integrated line points to each other); (b) 3-D EM model of diode based on DLPT (Port 3 and 4 represent dual lumped ports).



**FIGURE 4.** Cascade equivalent network of the diode based circuit.

the two red rectangular sheets under the probe represent dual lumped ports and the port impedance are both set as a real value(e.g., 50 Ω).

The proposed DLPT at the Schottky junction not only achieves automatic port phase matching, but also makes the defined internal ports have explicit physical meaning: the lumped port near the anode represents the anode port, and that near the buffer layer represents the cathode port. In this way, a one-to-one correspondence relationship between the internal ports of the 3-D EM model and the ports of the intrinsic model is established. Therefore, the intrinsic model of diode can be embedded into the 3-D EM model naturally according to the port correspondence relationship and the non-physical grounding path required in MCPT is no longer needed, as shown in Fig. 3(b). It should be noted that the intrinsic model of diode is essentially embedded into the 3-D EM model in series configuration through DLPT, which is in consistency with the small signal LEC model shown in Fig. 1(b).

**C. COMPARISION OF MCPT AND DLPT**

If these two port techniques discussed above are applied to establish different models for the same diode, an important question is whether there are any differences between these models. If any, which one has higher precision is worth

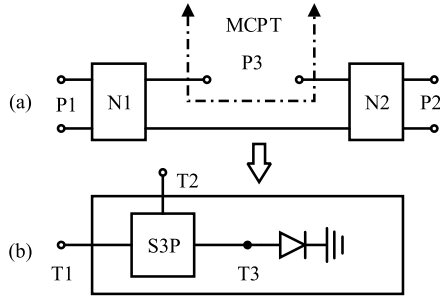


FIGURE 5. Cascade equivalent network of the diode based circuit using MCPT.

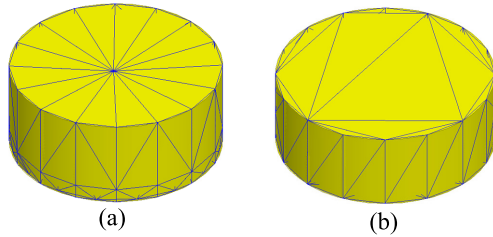


FIGURE 6. Meshing results of anode probe. (a) MCPT; (b) DLPT.

exploring. For the terahertz diode based circuits, no matter what circuit structure is adopted, how many diodes are used, or what transmission line form is utilized, each single diode and its external circuits can be equivalent to the cascaded network [32] as shown in Fig. 4(a). P3 and P4 represent anode and cathode reference plane, respectively, while P1 and P2 connects to other circuits. Then, the passive sub-networks are computed by full-wave simulation and the scatter matrixes are exported to harmonic balance simulator. It should be noted that the coupling effects between reference planes P3 and P4 must be taken into consideration, which may otherwise lead to impedance mismatch or frequency offset in the required frequency range. Fig. 4(b) illustrated the port coupling effect using a green line between T3 and T4.

However, if the MCPT is used as an internal port in Fig. 4(a), the coupling effect between P3 and P4 (the coupling between the anode probe and the buffer layer) is neglected due the penetration of the anode probe to the buffer layer as shown in Fig. 2 (a), which is regarded as a half-infinite uniform coaxial line. Furthermore, the four-port cascade equivalent network (Fig. 4(a)) is transformed into a three-port equivalent network (Fig. 5(a)) without considering the coupling effect, which is demonstrated through microwave network theory [32]. And then, the scatter matrix is exported into ADS with T3 connected to the intrinsic model of diode as an internal signal source, as shown in Fig. 5(b).

Similar to MCPT, the equivalent procedure using DLPT can also be demonstrated. What's the difference from MCPT is that, if the DLPT is used as an internal port in Fig. 4(a), the coupling effect between P3 and P4 will be taken into account because the original structural geometry of the anode probe is retained. Furthermore, the edge effect and coupling effect will affect the meshing of the anode probe when the model is being solved. Fig. 6 depicts the meshing results

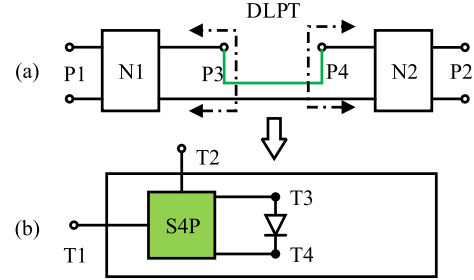


FIGURE 7. Cascade equivalent network of the diode based circuit using DLPT (Green line and filling represent the consideration of coupling effect).

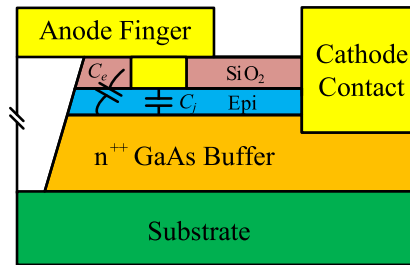


FIGURE 8. Edge capacitance represents the coupling effect near the anode probe.

of anode probe when adopting different internal port techniques at the same frequency. The anode solved by MCPT features rotationally symmetrical mesh partition, as shown in Fig. 6(a), indicating that the edge effect and coupling effect are neglected. The meshing result of DLPT in Fig. 6(b) has non-uniform meshing partitioning characteristics, which further indicates that the edge effect and coupling effect have been taken into account. Fig. 7 shows cascade equivalent network of diode based circuit using DLPT. The green line represents the coupling effect between internal ports. The green filling means that the coupling effect has been computed and included in the SNP files.

Considering the planar structure of the diode shown in Fig. 8, suppose that an edge capacitor  $C_e$  represents the coupling effect between anode probe and buffer layer, and  $C_j$  is the barrier capacitor of the diode. Then a discrepancy factor  $\eta$  can be defined to represent the discrepancy degree between MCPT and DLPT, as described in Equation (1). Generally,  $C_e$  is much smaller than  $C_j$ , so  $\eta$  tends to be very small. When the anode area is large, especially for frequency multiplication diodes, it can be predicted that a small difference exists between DLPT and MCPT. In this case, due to the additional consideration of port coupling effect, DLPT has higher accuracy than MCPT.

$$\eta = \frac{C_e}{C_j + C_e} \quad (1)$$

Through the above analysis, the advantages of DLPT over MCPT can be summarized as follows:

- 1) The ports defined by DLPT at the Schottky junction have definite physical meaning and DLPT eliminates the non-physical grounding requirement by MCPT;

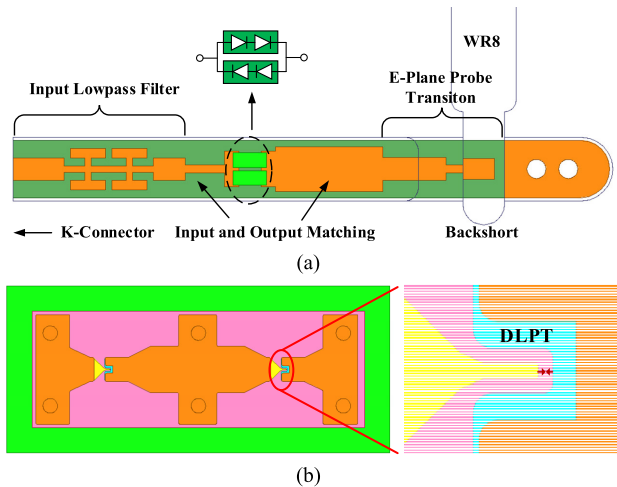


FIGURE 9. The schematic configuration and internal DLPT settings. (a) The schematic configuration of the 110GHz frequency tripler; (b) DLPT setting for 3-D EM modelling of DBES105a.

- 2) There is no need for penetration of epitaxial layer by DLPT and the coupling between the anode probe and the buffer layer is taken into consideration. Therefore, DLPT has higher accuracy than MCPT;
- 3) Buffer layer can be set as lossy conductor instead of ideal conductor which is required by MCPT. Therefore, the loss caused by buffer layer can be computed in the 3-D EM model;

III. DEMONSTRATION

In order to verify the proposed DLPT, a 110 GHz broadband tripler based on DLPT was designed by utilizing two commercial gallium arsenide Schottky varistor diodes DBES105a from United Monolithic Semiconductor (UMS) Inc. The diode, with cut-off frequency up to 3 THz, is a flip-chip dual Schottky junctions chip based on UMS-BES (Buried Epilayer Schottky) diode process featuring a very thin epitaxial layer thickness (100nm) and subsequently a low break-down voltage (-5V).

The schematic configuration of the tripler is shown in Fig. 9(a). The two diodes were arranged in anti-parallel configuration to form balanced structure and there is no need for additional filter to suppress even harmonics. In order to determine the embedding impedance of the diodes, a pair of dual lumped ports were assigned at the gap between the anode probe and the buffer layer. As illustrated in Fig. 9(b), the integral line directions of lumped ports point to each other for realizing correct phase relationship.

The whole nonlinear equivalent circuit model of anti-parallel diodes pair is constructed with the parasitic parameters derived from the 3-D EM model and the intrinsic SPICE parameters of the Schottky barrier, as depicted Fig. 10. Then the tripler was designed through the field-circuit iteration. Finally, the tripler was fabricated, assembled and measured. The whole circuit of the tripler is fabricated on RT/Rogers 5880 substrate with thickness of 0.127mm, housed in split

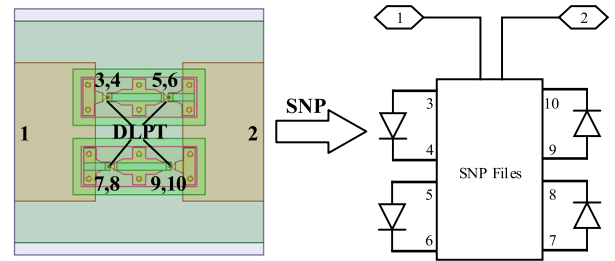


FIGURE 10. The 3-D EM model of DBES105a arranged in anti-parallel configuration based on DLPT.

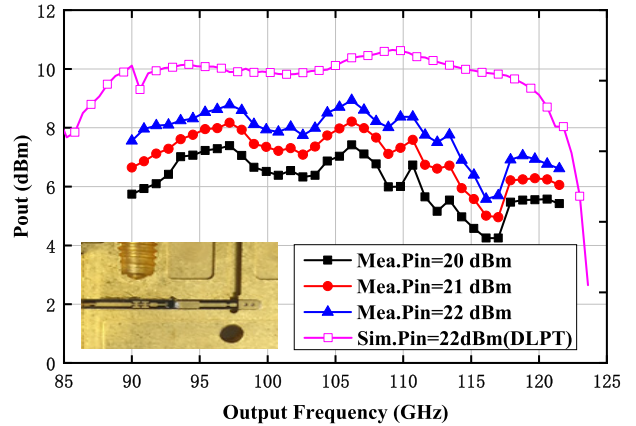


FIGURE 11. Measured output power under 20, 21 and 22 dBm input power.

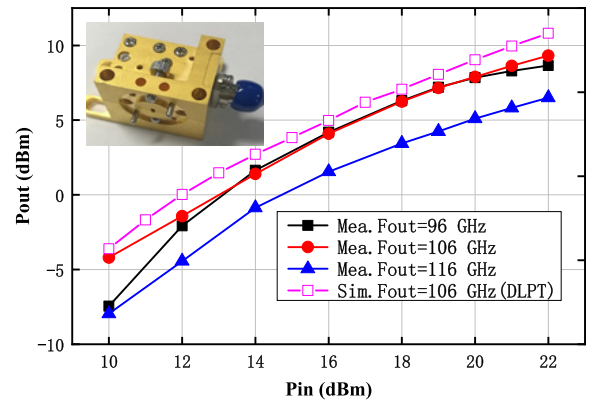


FIGURE 12. Measured output power varies as a function of input power at 96 GHz, 106 GHz, and 116 GHz.

waveguide blocks. The results are given in Fig. 11 and Fig. 12 with the insets of the fabricated tripler.

Fig. 11 gives the measured output power under different input power. The measured results show that with 20~22dBm input power at Ka-band, the tripler reaches maximum 9 dBm output power at 106 GHz and achieves 2.3%~5.5% efficiency across 90~120 GHz frequency band. The measured output power is consistent in the trends with the simulated curves based on DLPT, which indicates that DLPT is effective and accurate for the design of frequency multipliers. It should be noted that the measured output power drop suddenly around 116 GHz, which may be caused by impedance retroversion of the diodes.

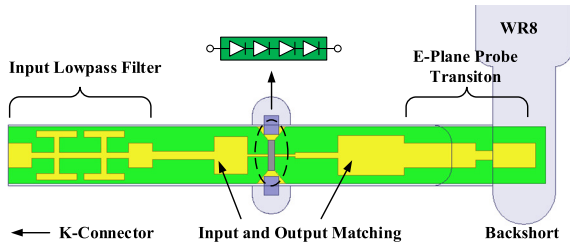


FIGURE 13. The structure of the 110 GHz tripler.

TABLE 1. Comparison of tripler with the state of the arts.

Ref.	Harmonic	Pin (dBm)	Effi. (%)	Freq. (GHz)
[33]	2	20	2~5	135~160
[34]	3	20	0.6~2.5	60~110
[35]	3	20~23	1~3	105~120
[20]	3	17	4~5	135~150
<b>This work</b>	<b>3</b>	<b>20~22</b>	<b>2.3~5.5</b>	<b>90~120</b>

Fig. 12 gives the results of output power as a function of input power at three different frequencies. Output power increases with the increase of input power, and then the tripler enters the saturation state gradually, which agrees with the simulated trend. As a summary, Table 1 gives the comparison between the designed tripler with the state of the arts.

IV. DISCUSSION

In our previous work, a 110 GHz tripler, a 160 GHz doubler [22], and a 220 GHz doubler [21] were designed, assembled and measured. In order to verify the validity and accuracy of the proposed DLPT further and find out the difference between DLPT and MCPT, several post-simulation analyses were performed on these frequency multipliers designed based on MCPT. In this process, the original 3-D EM models of diode established by MCPT were modified and replaced by the models based on DLPT for comparison while other simulation conditions were kept unchanged.

A. 110GHZ TRIPLER

As shown in Fig. 13, a 110 GHz tripler based on a 4-anode diode chip arranged in series in the same direction was designed using the 3-D EM model established by MCPT. The diode used in this design has an anode area of 28  $\mu\text{m}^2$ , zero-biased junction capacitance of 3fF, series resistance of 8  $\Omega$  and cut-off frequency of 3.6 THz.

The simulated and measured results of the tripler are given in Fig. 14. From the figure, it can be seen that there are some differences between the measured results and the simulated ones based on MCPT, including the deterioration of conversion efficiency and a certain degree of frequency offset. When the diode model was replaced with the model based on DLPT, the simulated efficiency curve agrees better with the measured results. This indicates that a slight discrepancy does exist between DLPT and MCPT, and the former exhibits

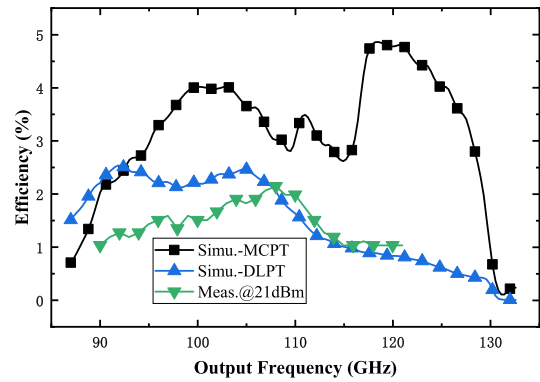


FIGURE 14. The structure of the 110 GHz tripler based on a 4-anode diode chip.

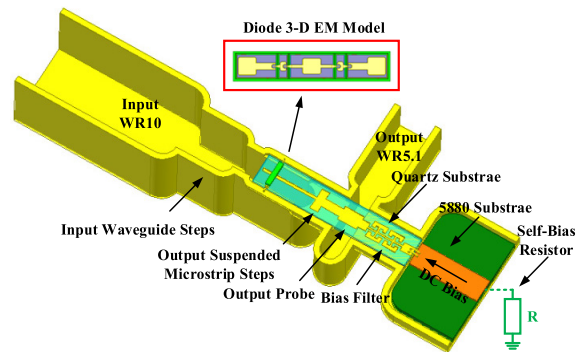


FIGURE 15. The configuration of the 135-190 GHz balanced frequency doubler.

a higher accuracy. This conclusion is consistent with the prediction in Section II.

B. 160GHZ DOUBLER

A 135-190 GHz self-biased broadband frequency doubler based on planar Schottky diodes was designed and measured. The diode used in this design is produced by Teratech company in UK and has four anodes arranged in anti-series configuration. The diodes use an epitaxial layer doping density of  $2 \times 10^{17} \text{ cm}^{-3}$  and diode anode area of  $6.6 \mu\text{m}^2$ , resulting a calculated zero-bias capacitance of 9.8 fF, a series resistance of 4.1  $\Omega$  and corresponding cut-off frequency of 2.2 THz. The configuration of the doubler is shown in Fig. 15. Unlike traditional bias schemes, the diodes are biased in resistive mode by a self-bias resistor, thus no additional bias voltage is needed for the doubler. The simulated and measured results are given in Fig. 16. The measured results show that the doubler exhibits a 3 dB bandwidth of 34% from 135 GHz to 190 GHz with a conversion efficiency of above 4% when pumped by a 100mW input power. It can be seen that the doubler exhibits an average conversion loss of 11 dB in the range of 140-180 GHz and the measured results agree well with the simulated results in terms of trends, except that a 2~3 dB deterioration of conversion loss is observed, which becomes more serious with the increasing frequency.

Similarly, the original model was replaced by the model based on DLPT and the simulated results were added

TABLE 2. Comparison of different internal port techniques for diode 3-D EM modeling.

Internal Port Techniques	Epitaxy Penetration	Junction Port Numbers	Grounding Path	Buffer Layer Material	Total Port Numbers	Calculating Port Coupling effect
MCPT	Yes	1	Yes	PEC	N+2	No
DLPT	No	2	No	PEC/LC*	2*N+2	Yes

N is the number of Schottky junctions in the 3-D EM model.  
LC\* represents lossy conductor.

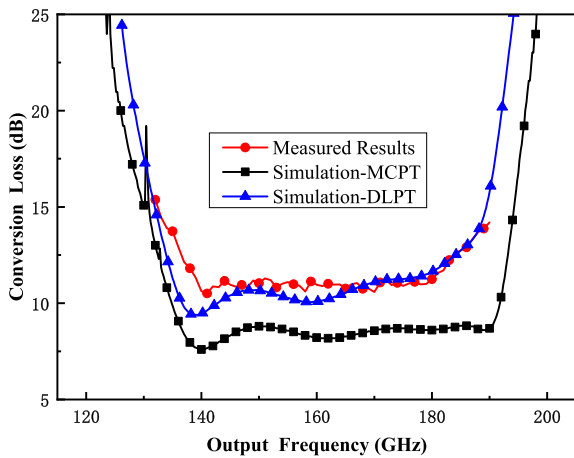


FIGURE 16. Simulated and measured results of the 160 GHz doubler.

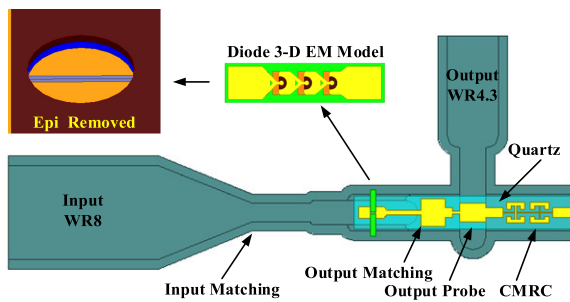


FIGURE 17. The configuration of the 220GHz frequency doubler.

in Fig. 16. The simulated conversion loss based on MCPT and DLPT are both in good agreement with the measured results in terms of curve trend. However, it is interesting that the simulated results based on DLPT coincide better with the measured results than the simulated ones based on MCPT. This further indicates that there are some differences between these two port techniques, and DLPT is more accurate than MCPT.

### C. 220GHZ DOUBLER

A 220 GHz high efficiency doubler based on ACST 5VA40-13 varactor diode chip was designed, as shown in Fig. 17. The diode has a relatively large anode area of about 38  $\mu\text{m}^2$  and a series resistance of 4.2  $\Omega$ , resulting a zero-biased junction capacitance of 40 fF, a cut-off frequency of 0.88 THz. In order to further verify the existence of port coupling effect, the epitaxial layer around the dual lumped

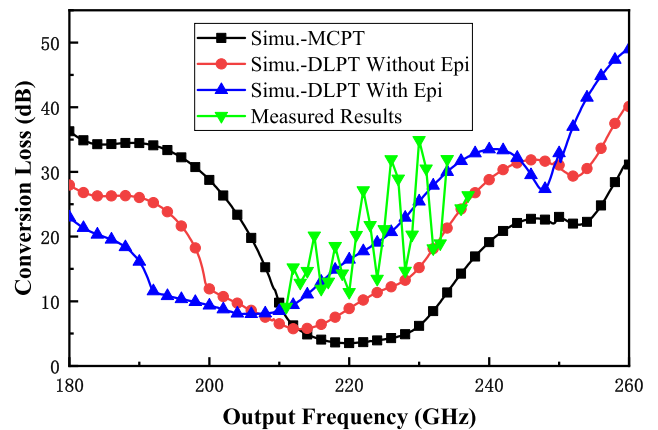


FIGURE 18. Simulated results of the 220 GHz doubler with and without removal of the epitaxial layer around the dual lumped ports.

ports is removed, which will reduce the strength of port coupling effect. In other words, the coupling capacitance  $C_e$  will be reduced. According to (1), when  $C_e$  is getting small, the discrepancy factor  $\eta$  will reduce, which means the discrepancy between DLPT and MCPT will decline.

The simulated conversion loss of the 220 GHz doubler is given in Fig. 18. It can be seen that the center frequency of the doubler shifts to lower frequency when the diode model based on MCPT is replaced by the model based on DLPT with epitaxial layer. Meanwhile, the simulated results based on DLPT without epitaxial layer under the anode probe are in the middle of the two simulated ones described above, which demonstrates that the port coupling effect does exist and DLPT is more accurate than MCPT for taking this effect into account. Although the measured results are rather volatile, they are still distributed on both sides of the simulated results based on DLPT.

From the above discussion, it can be known that the effectiveness of DLPT is demonstrated further. Moreover, a slight discrepancy between DLPT and MCPT is observed in these post-simulation comparison examples of frequency multipliers working at THz region (especially for anode with large area), which indicates that port coupling effect does exist. Furthermore, the better coincidence between post-simulation analysis by DLPT and the measured results indicates that the proposed DLPT is not only feasible for the design of terahertz frequency multipliers and mixer, but also possesses higher accuracy than MCPT for the additional consideration of port

coupling effect. Table 2 summarizes the characteristics of internal port techniques discussed in this paper for 3-D EM modeling of planar SBD.

## V. CONCLUSION

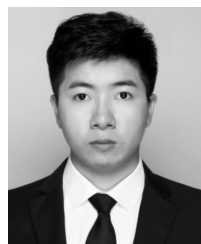
In this paper, a novel DLPT for 3-D EM modeling of planar SBD is proposed. Theoretical analysis and modeling methods for different internal port techniques are introduced and compared in detail. Through the design and post-simulation analysis of a series of frequency multipliers, the proposed DLPT is demonstrated to be effective for 3-D EM modeling of planar SBD in the terahertz band, and more accurate than traditional MCPT for the additional consideration of port coupling effect. Moreover, the internal ports defined by DLPT have clear physical meaning, by which the natural embedding of the intrinsic model of diode can be realized without the need for non-physical grounding path. The proposed DLPT is a good alternative of internal port techniques for diode 3-D EM modeling in the development of terahertz mixers, frequency multipliers and other diode based circuits.

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