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An Ultra-Compact On-Chip Reconfigurable Bandpass Filter With Semi-Lumped Topology by Using GaAs pHEMT Technology

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ABSTRACT A semi-lumped reconfigurable on-chip bandpass filter with GaAs pHEMT technology is presented in this paper. Three order tunable bandpass filter is designed with serial lumped capacitors, parallel resonators, and reconfigurable components. The operating bands are adjusted by field effect transistors and its corresponding gate bias circuits with GaAs technology. The semi-lumped topology, intending to reduce the size of the circuit, is employed to construct the parallel resonators, which are implemented with short-ended stubs and metal-insulator-metal capacitors. The equivalent circuit model is built to interpret the mechanism of the on-chip reconfigurable bandpass filter. Compared with the traditional tunable filters, an ultra-compactness feature and low insertion loss are obtained with the proposed design. The size of the on-chip filter is only 0.8×1.07 mm ^{2}, which is equivalent to $0.08\times0.11\ \lambda_g^2$ at 10 GHz. The presented filter is reconfigurable in two frequency bands, one is centered at 10 GHz with a fraction bandwidth (FBW) of 24.94% and the other is operated at 8.8 GHz with a FBW of 13.35%. The tuning range of the FBW is 30.6%. Good agreements are observed between the simulated and measured S-parameters.

INDEX TERMS GaAs pHEMT, miniaturized, on-chip, reconfigurable bandpass filter, semi-lumped topology.

I. INTRODUCTION

Reconfigurable filters are highly regarded as their ability to operate multiple frequency bands with a reducing complexity of the microwave systems [1]–[3]. However, traditional tunable filters are designed with printed circuit board (PCB) processing, which make the circuit size is too large to implement for circuit system integration. Therefore, it is necessary to achieve miniaturization as much as possible while maintaining the good performance of the reconfigurable filter [4]–[7].

Several tunable methods are reported in the previous literatures. A reconfigurable filter is designed by the principle of the lateral signal interaction [9]. Switching between multiple modes is implemented with RF p-i-n diodes. A tunable BPF with a LC lumped structure is proposed in [10]. The bandwidth, center frequency, and filter order can be adjusted by changing the values of multiple varactors. DGS structure with varactor also can be used to design tunable bandpass filters [11]–[13]. A reconfigurable microstrip filter with a distributed topology is shown in [14]. Compact size and low insertion loss are obtained with resistors loaded on the odd-symmetric plane of the dual-mode open-loop resonator. However, the above tunable filters are all designed on the PCB process. Under such circumstance, the larger size hinders its application to the high integrated circuit system. Therefore, several on-chip bandpass filters with miniaturized dimension are presented. In [15], a new millimeter wave bandpass filter using a coplanar waveguide structure is

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realized by silicon-based technology [16]. However, a large insertion loss is observed with a high loss tangent of the silicon-based substrate.

Gallium arsenide (GaAs) technology with a low dielectric loss characteristic is employed for the filter design. In [17], the E-type dual-mode filter is designed with GaAs substrate. For the above aforementioned GaAs structures, the on chip filters are mostly designed with the distributed topology, which could enlarge the filter dimension. Usually, the lumped topology can be utilized to reduce the circuit size significantly. However, it cannot be applied in the high frequency as the parasitic effects are introduced. Furthermore, few work about reconfigurable on chip filters with GaAs technology are reported. A multi-channel bandpass filter-bank is proposed by using GaAs technique [18]. However, large size with multiple filter structures are detrimental to achieving high integration. Therefore, it is imperative to investigate the measures to minimize the dimension of the reconfigurable on-chip filter associated with good transmission performances.

In this paper, a semi-lumped reconfigurable on-chip bandpass filter structure by using GaAs technology is presented. In order to meet the requirement of the X-band radar or communication system, a compact and reconfigurable on-chip filter is designed for the multi-functional RF front-end circuits. The proposed filter is composed of serial lumped capacitors, parallel resonators and reconfigurable components. The semi-lumped topology is employed for the parallel resonator to reduce the dimension. The equivalent circuit model is developed to explain the mechanism of the reconfigurable bandpass filter. An ultra-compactness size is obtained with the proposed design compared with the traditional tunable filters.

The outline of the paper is organized as follows. In section II, the circuit structure, design theory, and the equivalent circuit model of the tunable filter are analyzed. In Section III, an on-chip circuit sample is fabricated and measured with GaAs pHEMT technology to validate the design. A good consistency is obtained between the simulations and measurement results. Finally, the conclusion is achieved in Section IV.

II. GUIDELINES FOR MANUSCRIPT PREPARATION

A. STRUCTURE DESIGN AND ITS EQUIVALENT CIRCUIT MODEL

The structure diagram and the side view of the designed reconfigurable filter are shown in Fig. 1. As can be seen from Fig. 1(a), a three order tunable bandpass filter is designed with serial lumped metal-insulator-metal (MIM) capacitors, parallel resonators, and reconfigurable components. Four series MIM capacitors $C_1 - C_4$ is embedded to shorten the length of the main transmission line. A semi-lumped topology is employed to design the parallel resonators, which is realized by a short-end metal stub and a parallel grounded MIM capacitor. The length and width of the short-end metal stub are denoted as L_{TL1} and W_{TL1}, respectively. The grounding

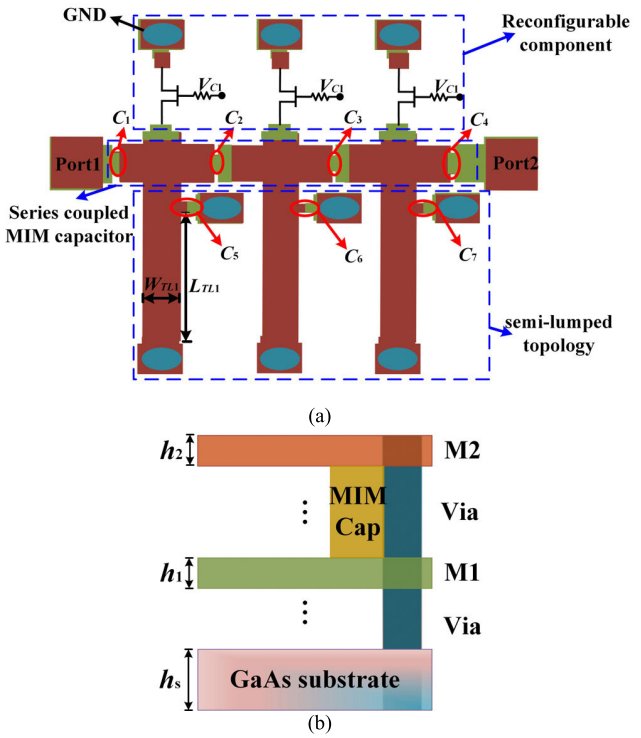

FIGURE 1. The configuration of the designed reconfigurable BPF: (a) the structure diagram and (b) the stack-up from the side view.

hole is connected to GND, as shown in Fig 1. Moreover, the reconfigurable component is achieved with field effect transistors (FET) V_{C1} and its corresponding gate bias circuits. Generally, the state of the FET can be controlled by applying different bias voltages to the FET gates.

The metal stack-up of the selected 0.25 μm GaAs pHEMT technology is presented in Fig. 1(b). From the figure, the metal layers, denoted as M2 and M1, are employed to implement the presented filter structure. Furthermore, the parallel plate MIM capacitor is also formed by the adjacent metal layers of M1 and M2. The thicknesses of the M2 and M1 layers are h_2 and h_1, respectively, and the height of the GaAs substrate is denoted as h_s.

In order to analyze the working principle of the filter in detail, a corresponding equivalent circuit model is demonstrated in Fig. 2. From the figure, the characteristic admittance and electrical length of the short-end metal stubs TL_1-TL_3 are denoted as Y_{00} and θ_{00}, respectively. J_{01} and J_{12} are treated as admittance inverter constants, which are marked as blue dot dashed and red dashed lines, respectively. Moreover, for the parallel resonators designed by semi-lumped topology, the short-end stub is utilized to instead the lumped inductor L, as shown in the green dotted lines.

According to the design theory of the capacitive coupled parallel resonator filter [19], serial lumped MIM capacitor C_1-C_4 can be calculated as:

$$J_{01} = \sqrt{\frac{FBW}{\omega_0 L g_0 g_1 Z_0}} \tag{1}$$

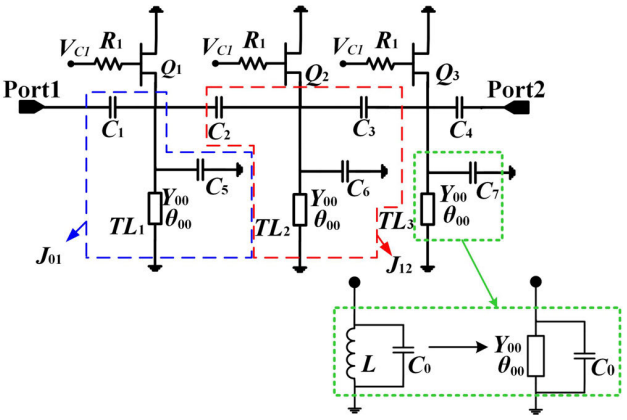

FIGURE 2. The equivalent circuit model of the proposed reconfigurable filter.

$$J_{12} = \frac{FBW}{\omega_0 L\sqrt{g_1 g_2}} \tag{2}$$

$$C_1 = C_4 = \frac{J_{01}}{\omega_0\sqrt{1-(J_{01}Z_0)^2}} \tag{3}$$

$$C_2 = C_3 = \frac{J_{12}}{\omega_0} \tag{4}$$

where $\omega_0 = 2\pi f_0, f_0$ is the center frequency of the passband, FBW represents the relative fractional bandwidth, Z_0 is the characteristic impedance of 50 Ω, g_0, g_1 and g_2 are the values of the selected filter prototype.

For the semi-lumped topology, the characteristic impedance Y_{00} of the short-ended metal stub can be calculated by the equivalent LC resonator:

$$\omega_0 = \frac{1}{\sqrt{LC_0}} \tag{5}$$

$$Y_{00} = \sqrt{\frac{C_0}{L}} \tag{6}$$

The value of the electrical length θ_{00} of the short-ended metal stub can be obtained by formula (7), which is resonated at frequency ω_0:

$$\frac{Y_{00}cot\theta_{00}}{j} + j\omega_0 C_0 = 0 \tag{7}$$

$$\theta_{00} = \arctan\frac{Y_{00}}{\omega_0 C_0} \tag{8}$$

Moreover, the capacitances C_5, C_6 and C_7 within the parallel resonator can be calculated as:

$$C_5 = C_6 = C_7 = \frac{1}{\omega_0^2 L} - \frac{C_1}{1+(\omega_0 C_1 Z_0)^2} - \frac{J_{12}}{\omega_0} \tag{9}$$

In the above analysis, the characteristic admittance Y_{00} of the short-ended metal stub within the semi-lumped parallel resonator can be achieved with the formulas (5)-(8). Then, based on the transmission theory [19], the width W_{TL1} of short-ended metal stubs can be calculated by:

$$\frac{W_{TL1}}{h_s} = \begin{cases} \dfrac{8e^A}{e^{2A}-2}, & W_{TL1}/h_s < 2 \\ \dfrac{2}{\pi}\left[B-1-\ln(2B1) + \dfrac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23+\dfrac{0.11}{\varepsilon_r}\right)\right], & W_{TL1}/h_s > 2 \end{cases} \tag{10}$$

$$A = \frac{1}{60Y_{00}}\sqrt{\frac{\varepsilon_r+1}{2}} + \frac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23+\frac{0.11}{\varepsilon_r}\right) \tag{11}$$

$$B = \frac{377Y_{00}\pi}{2\sqrt{\varepsilon_r}} \tag{12}$$

where ε_r is the relative dielectric constant of the GaAs substrate, h_s is the thickness of the GaAs substrate.

Based on the above analysis, the specific circuit parameters can be calculated with the target filter performances. According to the assuming parameter of FBW, the values of $C_1 - C_4$ can be deduced by formulas (1)-(4). Furthermore, C_5, C_6 and C_7 can be derived from equations (3), (4) and (9). Then, the values of the characteristic admittance Y_{00} and θ_{00} of the short-end metal stubs can be derived by equations of (5)-(8). The width W_{TL1} of the short-end metal stub can be obtained by equations (10)-(12).

B. TRANSMISSION CHARACTERISTICS ANALYSIS OF THE PROPOSED RECONFIGURABLE FILTER

As explained in the analysis of Fig. 2, the reconfigurability of the frequency band is achieved by changing the values of C_5, C_6, C_7 and L in the parallel resonator. From the figure, the FET is connected in parallel with the short-ended metal stub. And the values of C_5, C_6, C_7 and L are changed by tuning the switching state of the FET. In Fig. 4, the equivalent circuit models of the reconfigurable filter are depicted when FETs are at different states. As can be seen from the figure, if the FET is located at off-state and can be composed by the inductance L, the off-capacitance C_{off}, and the off-conductance G_{off}. Since the inductance L and the off-conductance G_{off} are small, the relevant parameters can be ignored in the circuit analysis. Otherwise, the voltage of the gate bias is higher than the cutoff voltage, the status of the FET turns to on-state and is equivalent to the inductance L and the on-conductance G_{on}.

According to the aforementioned discussions in section A, the component values of the reconfigurable filter can be obtained with the theoretic analysis. Then, the transmission behaviors of the filter can be induced correspondingly. Furthermore, the effects of the component values on the propagation characteristics are also analyzed.

Therefore, the resonant frequency of the parallel resonator varies with the different states of the FET, thereby realizing the reconfigurability of the frequency band. If FETs are in the off-state, the equivalent circuit model of the reconfigurable filter is shown in Fig. 3(a). The new capacitors formed by the equivalent capacitance of off-state Coff in parallel with C_5, C_6 and C'_7 are labeled as C'_5, C'_6 and C'_7, respectively.

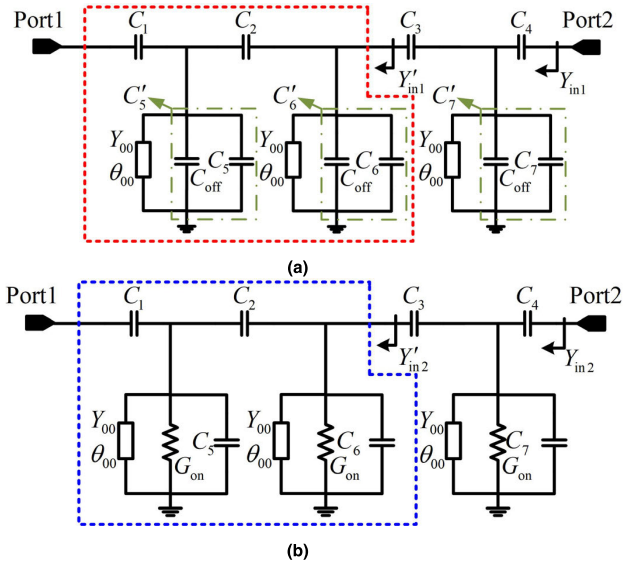

FIGURE 3. The equivalent circuit model of the reconfigurable filter when FETs are at different states: (a) off-state and (b) on-state.

As can be seen from Fig. 3, the input admittance of the filter is analyzed by two divisions. One is the admittance from port 2 to port 1 that is represented as Y_{in1}, which can be derived as:

$$Y_{\text{in1}} = \frac{Y_{C3}^2}{Y_{C7} + j\omega C_{off} - jY_{00}\cot\theta_{00} + \frac{Y_{C1}Y_0}{Y_{C1}+Y_0}} + Y'_{in1} \quad (13)$$

where $Y_{\text{c1}} - 1/j\omega_0 C_1$, $Y_{\text{c3}} = -1/j\omega_0 C_3$, $Y_{\text{c7}} = j\omega_0 C_7$, Y_0 is expressed as the characteristic admittance of the port1.

The other is the admittance marked within the dotted line, which is expressed as Y'_{in1} and can be determined as:

$$\begin{aligned} Y'_{\text{in1}} &= \frac{Y_{C2}^2}{Y_{C6} + j\omega C_{off} - jY_{00}\cot\theta_{00} + \frac{Y_{C4}Y_0}{Y_{C4}+Y_0}} \\ &\quad + Y_{C5} + j\omega C_{off} - jY_{00}\cot\theta_{00} \\ &\cong \frac{Y_{C2}^2(Y_{C4}+Y_0)}{Y_{C4}Y_0} \end{aligned} \quad (14)$$

where $Y_{\text{c2}} = -1/j\omega_0 C_2$, $Y_{\text{c4}} = -1/j\omega_0 C_4$, $Y_{\text{c5}} = j\omega_0 C_5$, $Y_{\text{c6}} = j\omega_0 C_6$.

According to the relationship between the ABCD matrix and the scattering matrix with the theory of microwave network, the transmission behavior can be derived from equations (10) and (11):

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_{\text{in1}} & 1 \end{bmatrix} \quad (15)$$

$$S_{21} = \frac{2}{A + BY_0 + C/Y_0 + D} \quad (16)$$

$$\begin{aligned} S_{21} &= \frac{2Y_0}{2Y_0 + \text{Re}\{Y_{\text{in1}}\}} \\ &= \frac{2Y_0}{2Y_0 + \frac{Y_{C2}^2(Y_{C4}+Y_0)}{Y_{C4}Y_0} + \frac{Y_{C3}^2(Y_{C1}+Y_0)}{Y_{C1}Y_0}} \end{aligned} \quad (17)$$

Similarly, if FETs are in the on-state, the equivalent circuit model is shown in Fig. 3(b). The equivalent conductance is denoted as G_{on}. From the figure, the input admittance of the filter can be also analyzed with two divisions.

One is that the admittance of port 2 to port 1is represented as Y_{in2}, which can be calculated as:

$$Y_{\text{in2}} = \frac{Y_{C3}^2}{Y_{C7} + G_{on} - jY_{00}\cot\theta_{00} + \frac{Y_{C1}Y_0}{Y_{C1}+Y_0}} + Y'_{in2} \quad (18)$$

The other is that the admittance of the dotted line in Fig. 4 is expressed as $Y'_{\text{in 2}}$, which can be determined as:

$$\begin{aligned} Y'_{\text{in2}} &= \frac{Y_{C2}^2}{Y_{C6} + G_{on} - jY_{00}\cot\theta_{00} + \frac{Y_{C4}Y_0}{Y_{C4}+Y_0}} \\ &\quad + Y_{C5} + G_{on} - jY_{00}\cot\theta_{00} \\ &\cong G_{on} + \frac{Y_{C2}^2}{G_{on}} \end{aligned} \quad (19)$$

Similarly, the insertion loss can be derived from equations (18) and (19):

$$S'_{21} = \frac{2Y_0}{2Y_0 + \text{Re}\{Y_{\text{in1}}\}} = \frac{2Y_0}{2Y_0 + G_{on}} \quad (20)$$

Based on the above formulas (13)-(20), the transmission responses at different states of the FET are analyzed. If FETs are in the off-state, the insertion loss is affected by the series coupling capacitors $C_1 - C_4$. Otherwise, the insertion loss is influenced by the on-state equivalent conductance G_{on}.

In order to verify the effectiveness of the equivalent circuit model of the presented reconfigurable filter, the ideal circuit model results and EM simulation predictions are both given in Fig. 4 for comparison. As can be seen from the figure, the center frequency can be adjusted with the state of the FET. Moreover, as be seen from Fig. 4(a), a large insertion loss about -7 dB is observed at the on-state, while the loss is decrease to -4 dB at the off-state. It is mainly because that the equivalent resistance of the FET at the on-state is larger than the corresponding value at the off-state, which also can be verified in Fig. 3. Furthermore, when the FET locates at on-state, the equivalent resistance would be enlarged with increasing of the width of the gate. Some slight discrepancies are observed between the result of the circuit model and the EM simulator. The main reason is mainly due that the circuit model is ideal. But for the full wave electromagnetic simulation, the coupling between the transmission line, parasitic effects of the FETs, and the accuracy of the process design kit will have serious influence on the transmission behaviors of the on-chip filter.

Furthermore, the effects of the component parameters on the propagation characteristics of the tuable filter are analyzed. The on-state equivalent conductance G_{on} and off-state equivalent capacitance C_{off} are affected by the change of the total gate length W_{g} of the FET, which is employed to observe the variation trend of the transmission poles. In order to interpret the variation of the transmission poles clearly, the influence of the width of the FET gate is analyzed. As shown in Fig. 5(a), when the FETs are in the on-state, the resonate

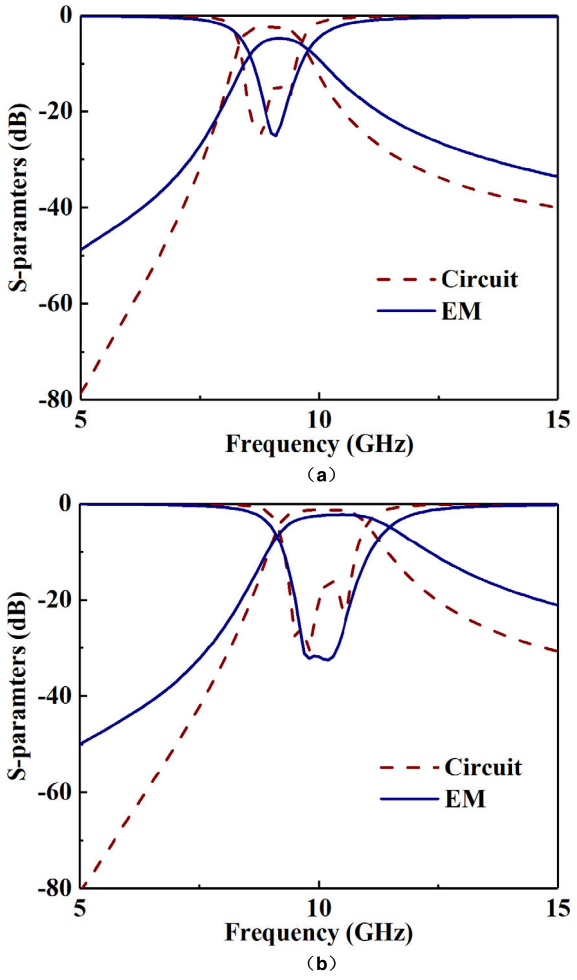

FIGURE 4. Comparison between the equivalent circuit results and EM simulations of the reconfigurable filter with: (a) on-state FET and (b) off-state FET.

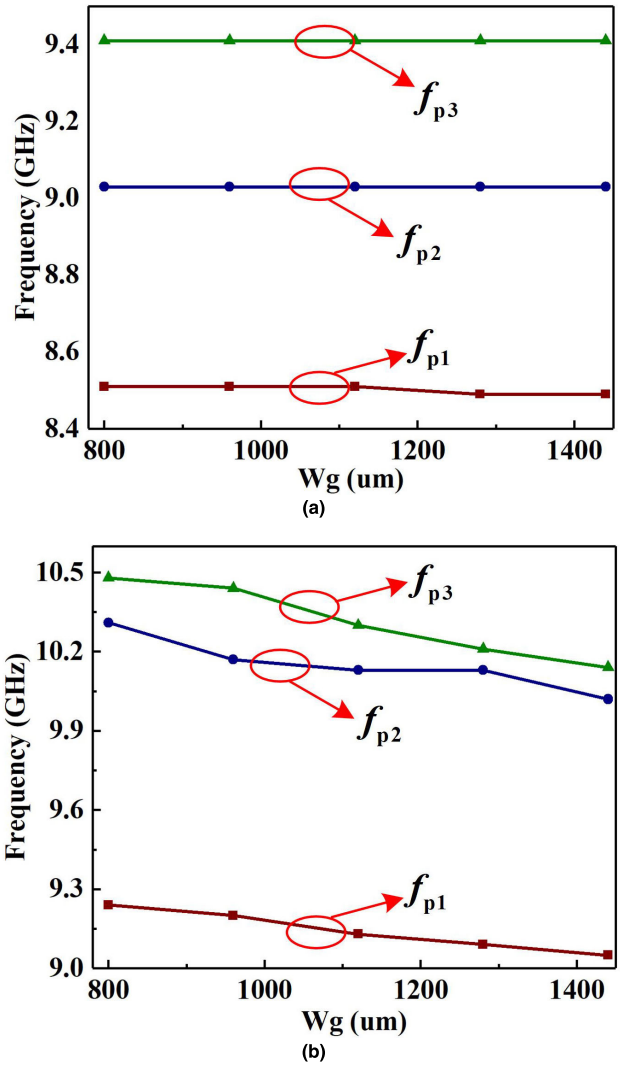

FIGURE 5. The influence of the parameters of the proposed filter on the positions of transmission pole: (a) Wg (on-state FET), (b) Wg (off-state FET).

frequencies of the transmission poles f_{p1}, f_{p2}, and f_{p3} are almost unchanged with the variations of the total gate width W_g. In other words, the on-state equivalent conductance G_{on} has little effect on the transmission poles. Moreover, as can be seen from Fig. 5(b), when the FETs are in the off-state, the transmission poles f_{p1}, f_{p2}, and f_{p3} move towards the band of the lower frequency with increasing of W_g, indicating that the transmission pole positions can be changed with the off-state equivalent capacitance C_{off}.

In Fig. 6, the influence of the capacitances within the semi-lumped topology on the transmission response is also analyzed. For the designed three order bandpass filter, the capacitors $C'_5 - C'_7$ of the parallel resonator are identical. From the figure, the center frequency of the filter would be moved to a low band with increasing of $C'_5 - C'_7$. In addition, the FBW of the filter would be narrowed by increasing the values of $C'_5 - C'_7$. Moreover, it also can be inferred from the figure that FBW becomes smaller with the decrease of the center frequency, which is also verified from the formulas (1)-(4).

Moreover, as indicated in Fig. 6, the tuning range of the filter is determined by the variation of the capacitors C'_5-C'_7. From Fig. 3, when the FET locates at off-state, an equivalent capacitance is observed. In order to change the tuning range of the filter, the equivalent capacitances at the off-state need to be varied associated with the correspondingly gate width of the FET. However, the insertion loss would also be influenced with the large equivalent resistance of the FET at the on-state, which is also clarified in Fig. 4. Therefore, it is a trade-off between the frequency tuning range and the insertion loss of the filter.

Usually, for the traditional on-chip circuit, lumped element circuits with different topologies of inductors, resistors and capacitors are employed to design the filter. However, owing to the effect of the lumped inductor, large size, lower Q value, and high insertion loss would be introduced with the filter. Therefore, in order to make the design on-chip filter more compact and integrated, a semi-lumped topology with

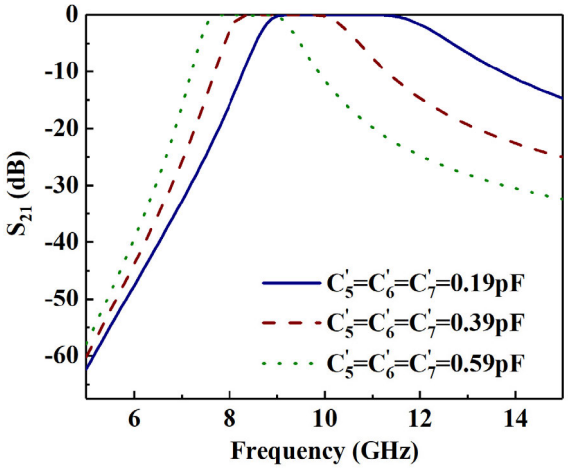

FIGURE 6. Transmission response of the proposed bandpass filter with the variation of C'_5, C'_6 and C'_7.

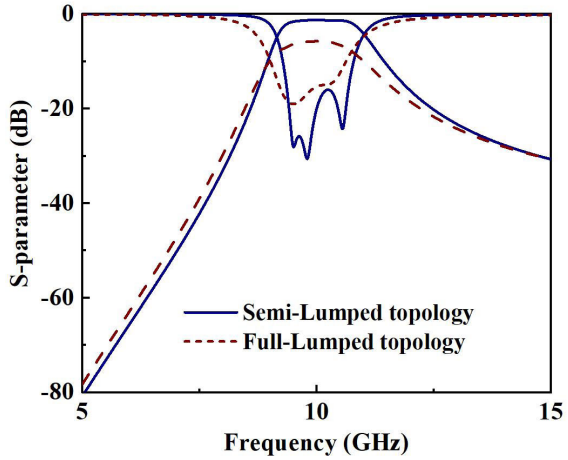

FIGURE 7. Comparison of the filter performances between the semi-lumped topology and the full-lumped topology.

short-end metal stub and a parallel grounded MIM capacitor is employed to design the parallel resonators of the filter.

Moreover, the transmission behaviors between the presented design of the semi-lumped topology and the full-lumped circuits are both depicted in Fig. 7 for comparison. By using the shunt-stub to instead the lumped inductor, the insertion loss of the filter would be decreased with the high Q value. In comparison with the conventional full-lumped circuits, good performances of miniaturized size, high Q value, and low insertion loss are achieved with the presented semi-lumped topology of the filter. The proposed design would be more suitable for the microwave on-chip filter structure.

According to the above analysis, the specific design procedures of the proposed reconfigurable filter can be summarized as follow:

1) Firstly, based on the tradeoff among chip size, optimization difficulty, and design rules of the GaAs processing, the value of the inductance within the *LC* parallel resonator is determined. Then, from equations (1)-(4), the serial coupling capacitors $C_1 - C_4$ can be derived with the desired center frequency and the FBW of the tunable filter.

2) Secondly, The electrical length θ_{00} and the characteristic admittance Y_{00} of the short-end metal stub of the parallel resonator can be obtained with the values of the *LC* parallel resonator by the formulas (5)-(8).

3) Thirdly, the parallel resonant capacitors $C_5 - C_7$ can be obtained from the desired center frequency and the serial coupling capacitor C_1 of the tunable filter with equation (9).

4) Then, the short-end metal stub is paralleled with the FET to constitute the reconfigurable component, which is employed to tune the resonate frequency of the on-chip filter.

5) Finally, the structure parameters of the presented tunable on-chip filter are optimized with the EM simulator based on the design predictions.

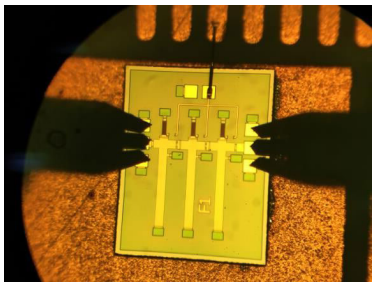

FIGURE 8. The photo of the presented reconfigurable filter under the microscope.

III. VERIFICATION OF THE SIMULATION AND MEASUREMENT

In order to validate the presented reconfigurable on-chip filter, a prototype is designed and fabricated with the 0.25 μm GaAs pHEMT technology. The used substrate is GaAs with a dielectric constant ε_r of 12.9, a thickness h_s of 0.1mm, and a loss tangent δ of 0.001. The photo of the manufacturing sample under the microscope is shown in Fig. 8. The size of the on-chip tunable filter is 0.8 $\times$1.07 mm ^{2}, excluding the pads, which is equivalent to 0.08$\times$ 0.11 λg^2 at 10 GHz. The measurement is accomplished by vector network analyzer Keysight N5244 and semi-automatic wafer probe station Cascade Summit 12000B.

The simulation and measurement results are described in Fig. 8 for comparison. As shown in Fig. 9(a), when the FET is located at on-state, the filter is centered at 8.8 GHz, with FBW of 13.35% and the return loss of 25 dB. From the Fig. 9(b), if the FET is turned to off-state, the measured operating band is centered at 10 GHz, the FBW of 24.94% from 8.89 to 11.32 GHz, the insertion loss of 4.1 dB, and the return loss of 20 dB. Moreover, the out-of-band rejection level is better than 40 dB in the stop bands. The difference between the simulation results and the measurement results is mainly due to the parasitic parameters, manufacturing tolerances of the GaAs FET, and the conductance loss of the transmission line. Moreover, the calibration tolerances for the on-chip measurements are also taken effects on the measurement results.

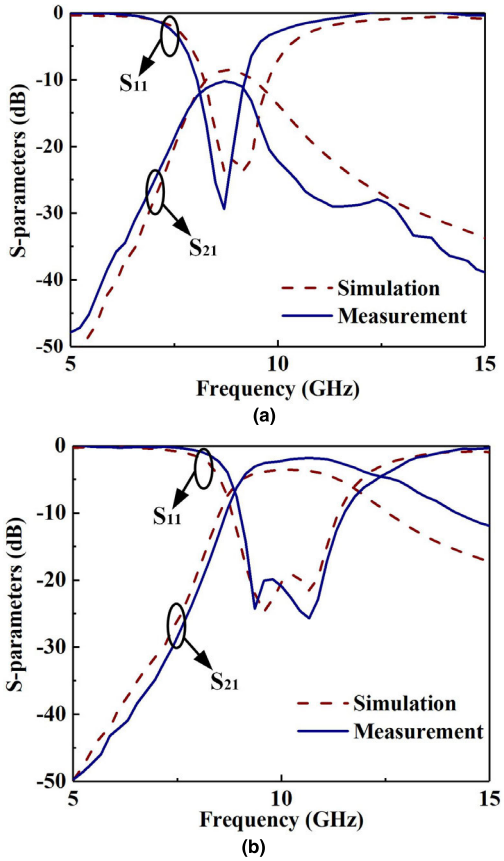

FIGURE 9. Comparison of simulation and measurement results of the proposed reconfigurable on-chip filter: (a) the on-state FET and (b) the off-state FET.

TABLE 1. Comparisons with some of the tunable filter in references.

Ref.	Method	f_c (GHz)	FBW Tuning Range	Size ($\lambda_g \times \lambda_g$)	IL (dB)
[4]	RF-MEMS	16.3	17.7%	0.94×2.17	-1.7
[5]	BST Varactor	1.8	17.7%	0.27×0.33	-2
[6]	Varactor diodes	0.92	6%	0.12×0.16	-3.5
[7]	Varactor diodes	2	15%	N/A	-4.5
[15]	COMS Switch	10.5	66%	0.08×0.06	N/A
[18]	GaAs pHEMT	12	50%	0.43×0.16	-4.2
This work	GaAs pHEMT	10	30.6%	0.08×0.11	-4.1

Finally, the performances of the proposed reconfigurable filter and some reported ones are listed in Table 1 for comparison. From the table, most of the reconfigurable filters are designed with traditional tunable components of varactors and the PCB process, which result in an enlarged dimension of the circuit [4]–[8]. Few works about reconfigurable on chip filter with GaAs technology are reported. In [18], a tunable filter bank with GaAs pHEMT varactor is presented with large size. Moreover, in order to clarify clearly the performance of the reconfigurable filter, the tuning range of the FBW is employed to evaluate [15]. The specific definition of the parameters is also described as $\mathrm{FBW}_{\mathrm{TunableRange}} = (f_{HT} - f_{LT})/f_0$. Among them, f_{HT} and f_{LT} are the highest and lowest tunable frequency, respectively. In comparison with the previous method, a lower insertion loss and ultra-compactness feature is obtained with the presented reconfigurable on-chip filter.

IV. CONCLUSION

In this paper, a miniaturized semi-lumped reconfigurable on-chip bandpass filter with GaAs pHEMT technology is presented. The filter is achieved by serial lumped capacitors, parallel resonators, and reconfigurable components. The semi-lumped topology is employed to reduce the size of the circuit. The equivalent circuit model is built to interpret the mechanism of the design. From the measurement result, the proposed reconfigurable on-chip bandpass filter takes the advantages of low insertion loss and ultra-compactness, which can be more attractive in the high-integration circuit system.

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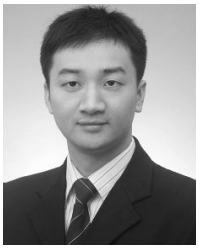

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