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A Modular Multilevel Dual Buck Inverter With Adjustable Discontinuous Modulation

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ABSTRACT Conventional single-cell dual buck inverters present high reliability, however they cannot be directly used in high voltage applications, because of the limited voltage rating of commercial switching devices. Therefore, a novel modular multilevel dual buck inverter (MMDBI), capable of processing voltage and power at higher levels, requiring a single dc input voltage, is proposed in this paper. Non-interleaved phase-shifted discontinuous modulation (NIPSDM) and interleaved phase-shifted discontinuous modulation (IPSDM) schemes are applied to the proposed inverter to reduce the current stress in the switching devices. Despite beneficial to the converter efficiency, the use of these discontinuous modulation approaches results in current zero-crossing distortion, which needs to be appropriately managed. In this work, theoretical values for the common-mode and differential-mode current ripples under NIPSDM and IPSDM modulation strategies are derived, and each switching operating mode is fully analyzed. From that, an adjustable current threshold value, which depends on the theoretical current ripple magnitude, is incorporated into the modulation strategy, producing a minimum switching overlap period between the two buck cells that eliminates the current zero-crossing distortion and produces a high-quality output current. Extensive simulation and experimental investigations are presented to demonstrate the feasibility and effectiveness of proposed topology and adjustable discontinuous modulation strategy.

INDEX TERMS Modular multilevel converter, dual buck inverter, discontinuous modulation, interleaved, non-interleaved, current ripple.

I. INTRODUCTION

Inverters play a crucial role in renewable power generation systems, uninterruptable power supplies, motor drives, airplane power systems, active filters, among others. While many topological arrangements have been proposed over the years, the search for novel inverter topologies with higher efficiency and reliability [1], [2] still is a driving force in power electronics, both in industry and academia.

Most of the proposed topologies are based on complementary switch arrangements, which inherently require the use of switch turn on dead-time to prevent converter shoot-through [3]. This inevitably results in output voltage distortion and limits the upper boundary of the switching frequencies that the converter can operate. It is also a major reliability hazard, especially when the switching frequency reaches several kHz.

In order to handle the existing shortcomings of traditional bridge-type converters, the dual buck inverter (DBI), an inherently shoot-through free topology, was firstly proposed in [4]. The arrangement eliminates the need for dead-time and associated output distortion and has high reliability. Nevertheless, the conventional single-cell dual buck half-bridge presents several drawbacks. Firstly, its reduced (50%) dc voltage usage leads to high voltage stress in the switching devices. Secondly, commercially available switching devices have limited

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voltage blocking capability, restricting the conventional DBI to low voltage, low power applications.

One approach to address these limitations is to improve the dual buck converter structure. In-depth analysis of the operation principles and characteristics of modified dual buck topologies were discussed in [5]–[16]. Typical structure variations include the dual buck full-bridge topology [9], [10] and the three-bridge dual buck topology [11], [12], which has higher dc voltage usage and lower voltage stress. Besides that, the single inductor dual buck topology [13] and the T-type dual buck topology [14] were proposed with the particular aim of reducing the system volume with fewer inductors and higher magnetic usage. However, because of the complex structure typically containing large number of switches, the influence of switching losses cannot be ignored in high power conversion applications. A family of dual buck structure with improved efficiency and reliability was proposed in [15], [16], where the general principles of the dual buck topology were summarized in detail, however without specific discussion on the modulation requirements for this topological arrangement.

There are two mainstream modulation strategies for dual buck inverters, which can be classified as full-cycle and half-cycle schemes. Full-cycle modulation requires all switches operating simultaneously within a fundamental period. This approach incorporates a bias into the inductor currents that produces an additional output voltage level [17], at the expense of higher device current stress and reduced converter efficiency. Conversely, only half the active switches conduct within each half period under half-cycle modulation. This eliminates the need for a bias current and improves the conversion efficiency, however introduces current zero-crossing distortion, originated from the presence of current ripples of opposite direction during the zero-crossing transitioning. References [10], [18] have proposed a hysteresis current control scheme to suppress the distortion, with the drawback of operating with variable switching frequency. A hybrid PWM method is adopted in [2], [18], where the duty ratio is set to 0 within the zero-crossing region to suppress the distortion, however this leads to distortion in the overall output current. A repetitive controller under this nonlinear modulation is introduced to eliminate the distortion, however tuning of the controller parameter is non-trivial. In [1], left and right switches of the dual buck are commanded to conduct simultaneously at a critical point of the inductor current, creating a smooth ripple current transition with suppression of the current distortion during zero crossings.

Multilevel topologies have evolved as a viable option to achieve lower voltage and current stresses with reduced switching losses while operating at higher dc link voltage conditions, when compared to the conventional DBI. The cascaded H-bridge multilevel inverter has the merits of modularity and controllability, however it presents shoot-through hazard because of its bridge-type cell unit. The cascaded dual buck half-bridge topology [20], [21] and the cascaded dual buck full-bridge topology [22]–[24] were proposed as alternatives to increase the converter reliability. Within this context, the use of carrier phase-shifted unipolar or bipolar PWM strategies allows increasing the effective converter switching frequency and this potentially eliminates the ripple current at zero crossings, reducing the distortion [20]. However, the use of multiple individual dc voltage sources results in larger volume and higher overall cost.

Another popular multilevel topology is the modular multilevel converter (MMC), which presents inherent modularity and scalability, flexible control, compact design, excellent harmonic performance and high efficiency. MMC allows high power conversion using low-voltage rated active switching devices, and this makes it a very suitable topology for high voltage and high power applications [25]–[30]. MMC converters formed by dual buck submodules (SMs) retain the same bidirectional four quadrant operation capability of traditional MMCs formed by full-bridge (or half-bridge) submodule arrangements.

This paper proposes a novel modular multilevel dual buck inverter (MMDBI) with adjustable discontinuous modulation. Operation principles and current path for the various converter switching modes are analyzed in detail for both non-interleaved phase-shifted discontinuous modulation (NIPSDM) and interleaved phase-shifted discontinuous modulation (IPSDM) schemes. In addition, common-mode and differential-mode current characteristics are compared between the two proposed discontinuous modulation approaches, since they present completely opposite patterns with the implementation of different interleaved angles. An adjustable current threshold, based on the theoretical current ripple values, is incorporated into the discontinuous modulation command to manage the current zero-crossing distortion and enhance the converter power quality. Simulation and experimental results illustrate the distinct converter behavior when operating under IPSDM or NIPSDM schemes and validate the proposed approach to mitigate the zero-crossing current distortion of this topology.

II. PROPOSED MMDBI TOPOLOGY

A. STRUCTURE OF PROPOSED MMDBI

Fig. 1 illustrates the circuit configuration of the proposed MMDBI. The dc system of MMDBI, often referred as dc-bus or dc-link, connects across the positive and negative nodes of the converter phase-leg. The single-phase ac system is divided into upper and lower arms, each formed by a series connection of N identical sub-modules and a center-tap coupled buffer inductor connected to an RL load. The converter losses are modeled by the parasitic resistance of the arm inductor. The midpoint of the independent dc sources acts as ground node of the overall MMDBI system.

As shown in Fig. 1(b), the sub-module is a dual buck topology, consisting of a dc capacitor and two legs, each formed by an IGBT and an anti-series diode, whose midpoint connects to the buffer coupled-inductor.

B. MATHEMATICAL MODEL OF PROPOSED MMDBI

Applying Kirchhoff's voltage law to the circuit in Fig. 1 yields the following equations:

$$U_{dc} - u_u - u_o = R_s i_u + L_s \frac{di_u}{dt} + L_m \frac{di_l}{dt} \quad (1)$$

$$U_{dc} - u_l + u_o = R_s i_l + L_s \frac{di_l}{dt} + L_m \frac{di_u}{dt} \quad (2)$$

where U_{dc} is the overall dc-link voltage, u_u, u_l, u_o are the sum of the N submodule voltages in the upper and lower arms and the ac-side output voltage, respectively; i_u, i_l are the upper and lower arm currents, respectively; L_s, L_m are the self-inductance and mutual inductance of the coupled arm inductor; and R_s is the parasitic arm resistor. Subtracting (1) from (2) yields

$$u_o = \frac{1}{2}(u_l - u_u) + \frac{1}{2}R_s(i_l - i_u) + (L_s - L_m)\frac{d(i_l - i_u)}{dt} \quad (3)$$

In addition, using Kirchhoff's current law, the output current of MMDBI system can be written as

$$i_o = i_u - i_l \quad (4)$$

The upper and lower arm currents and voltages can be split into common-mode and differential-mode quantities and expressed as

$$i_u = i_{cm} + i_{dm} \quad i_l = i_{cm} - i_{dm} \quad (5)$$

$$u_u = u_{cm} - u_{dm} \quad u_l = u_{cm} + u_{dm} \quad (6)$$

where i_{cm}, i_{dm}, u_{cm}, u_{dm} represent common-mode and differential-mode currents and voltages, respectively.

Additionally, substituting (4)-(6) into (1) and (2) yields

$$u_{cm} = U_{dc} - R_s i_{cm} - (L_k + 2L_m)\frac{di_{cm}}{dt} \quad (7)$$

$$u_{dm} = (R_s + 2R_g)i_{dm} + (L_k + 2L_g)\frac{di_{dm}}{dt} \quad (8)$$

where $L_k = L_s - L_m$ represents the leakage inductance of the coupled arm inductor. Since L_k and R_s are negligible in practice, Equation (3) is approximated as

$$u_o \approx \frac{1}{2}(u_l - u_u) \quad (9)$$

III. DISCONTINUOUS MODULATION SCHEMES

A. FUNDAMENTALS OF DISCONTINUOUS MODULATION

Figure 2 provides key waveforms of a dual buck MMC SM operating with discontinuous (Fig. 2(a)) and continuous (Fig. 2(b)) modulation schemes. From Fig. 2(a), continuous modulation requires that all switches operate simultaneously within the entire fundamental period. Continuous current mode (CCM) with synthesis of three-level SM voltage is achieved by incorporating a bias offset into the phase-leg coupled-inductor currents, which increases the devices current stress and associated switching and conduction losses. Conversely, under discontinuous modulation the active switches conduct complementarily within each half period (see fig. 2(b)), and this effectively reduces the device current stress and improves the conversion efficiency.

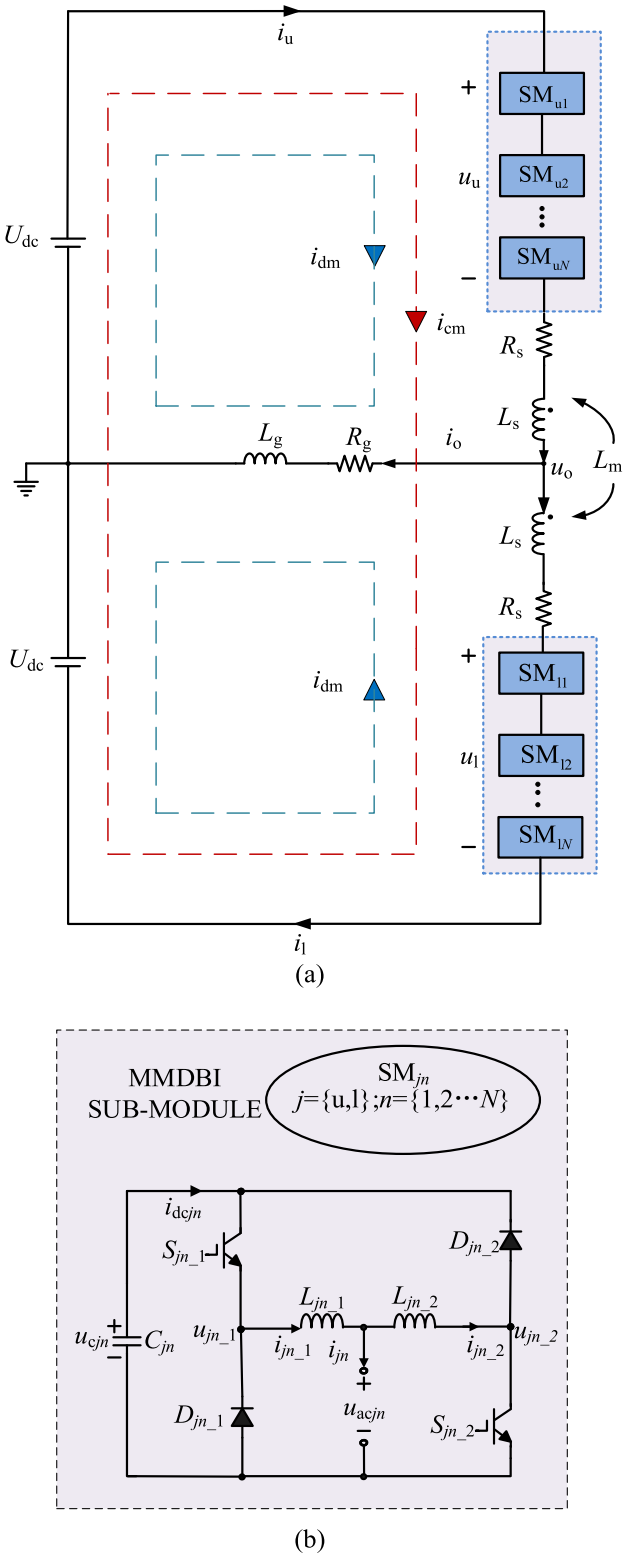

FIGURE 1. Circuit configuration of the proposed MMDBI. (a) System layout and (b) Dual buck submodule.

When the converter submodule is commanded with discontinuous modulation, the left buck cell (formed by switch S_{jn_1}, freewheeling diode D_{jn_1}, inductor L_{jn_1} and capacitor C_{jn} shown in Fig. 1.(b)) and the right buck cell (formed by

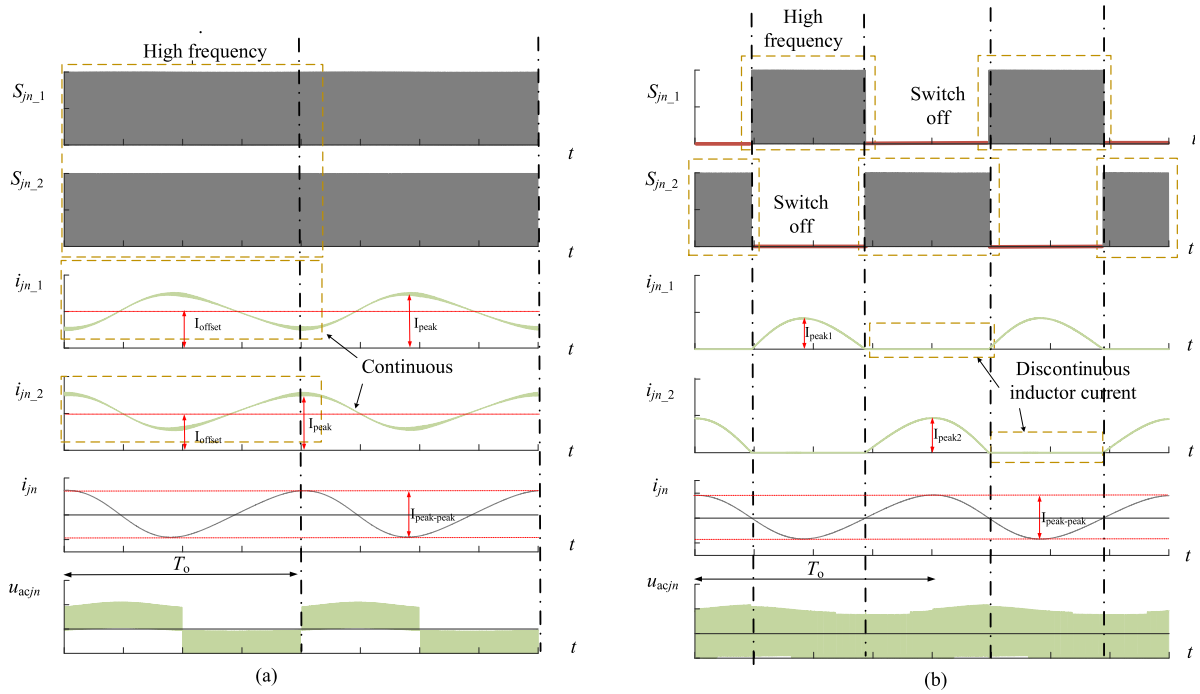

FIGURE 2. Illustration of two typical modulation schemes for dual buck cell. (a) Continuous modulation and (b) Discontinuous modulation.

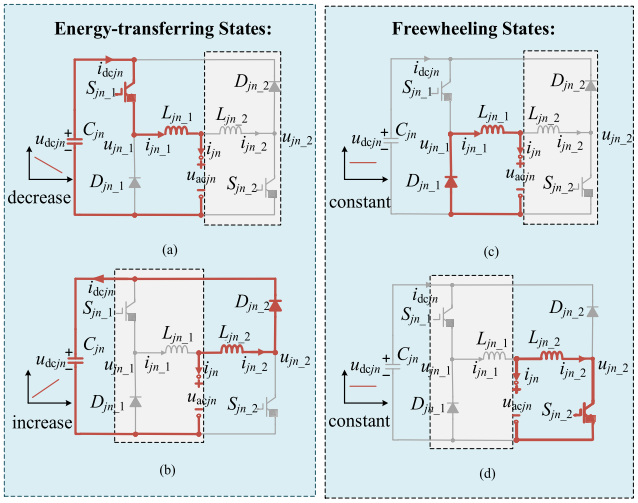

FIGURE 3. Operating states of the dual buck submodule. (a) Left buck operates, S_{jn_1} is on; (b) Right buck operates, S_{jn_2} is off; (c) Left buck operates, S_{jn_1} is off; (d) Right buck operates, S_{jn_2} is on.

switch S_{jn_2}, freewheeling diode D_{jn_2}, inductor L_{jn_2} and capacitor C_{jn} shown in Fig. 1.(b)) operate complementarily within a fundamental cycle. This results in four distinct operating states, illustrated in Fig. 3, where for two of these states there is an energy transfer from/to the submodule capacitor, while for the other two states the submodule capacitor is bypassed and its charge (and consequently, voltage) remains constant. When the left buck cell is operating, S_{jn_1} and D_{jn_1} alternately conduct to guarantee a continuous current flow through inductor L_{jn_1}. The submodule capacitor is bypassed when the freewheeling diode D_{jn_1} is conducting and it discharges when the switch S_{jn_1} is on, therefore the submodule capacitor energy keeps decreasing-constant-decreasing in cycles. Similarly, the capacitor energy keeps increasing-constant-increasing when the right buck cell is operating.

Consider that each submodule of the proposed MMDBI has identical characteristics (in particular, $L_{jn\_1} = L_{jn\_2} = L_{\rm sm}$) and assume two submodules per arm ($N = 2$) for simplicity. Consider that the phase-shifted carrier discontinuous PWM scheme achieves natural voltage balance and all submodule capacitor voltages are equal, i.e. $u_{\rm cu1} = u_{\rm cu2} = u_{\rm cl1} = u_{\rm cl2} = U_{\rm dc}$. The converter submodule switching behavior under NIPSDM and IPSDM schemes can be divided into four stages according to the individual switch conditions, as shown in Table 1. More specifically, stage I is characterized by having $i_{\rm l} > i_{\rm u} > 0$ and $i_{\rm o} < 0$, with switch pairs $S_{\rm u1\_2}$, $S_{\rm u2\_2}$ and $S_{\rm l1\_2}$, $S_{\rm l2\_2}$ both switching at high-frequency. Stage II has $i_{\rm l} > 0 > i_{\rm u}$ and $i_{\rm o} < 0$, with switch pairs $S_{\rm u1\_1}$, $S_{\rm u2\_1}$ and $S_{\rm l1\_2}$, $S_{\rm l2\_2}$ both switching at high-frequency, whereas stage III has $i_{\rm u} > i_{\rm l} > 0$ and $i_{\rm o} > 0$, with switch pairs $S_{\rm u1\_2}$, $S_{\rm u2\_2}$ and $S_{\rm l1\_2}$, $S_{\rm l2\_2}$ both operating at high-frequency. Finally, stage IV has $i_{\rm u} > 0 > i_{\rm l}$ and $i_{\rm o} > 0$, with switch pairs $S_{\rm u1\_2}$, $S_{\rm u2\_2}$ and $S_{\rm l1\_1}$, $S_{\rm l2\_1}$ both switching at high-frequency.

Next section provides a detailed analysis of the specific submodule switching patterns, taking into account the symmetrical operation and circuit layout of MMDBI.

B. NON-INTERLEAVED PHASE-SHIFTED DISCONTINUOUS MODULATION SCHEME (NIPSDM)

The phase-shifted modulation approach evenly allocates the N carriers in both upper and lower arms with incremental

TABLE 1. Submodule switching stages under discontinuous modulation scheme.

Switching Stage	Individual Switch Condition							
	S_{u1_1}	S_{u1_2}	S_{u2_1}	S_{u2_2}	S_{l1_1}	S_{l1_2}	S_{l2_1}	S_{l2_2}
Stage I $i_l > i_u > 0$ and $i_o < 0$	×	○	×	○	×	○	×	○
Stage II $i_l > 0 > i_u$ and $i_o < 0$	○	×	○	×	×	○	×	○
Stage III $i_u > i_l > 0$ and $i_o > 0$	×	○	×	○	×	○	×	○
Stage IV $i_u > 0 > i_l$ and $i_o > 0$	×	○	×	○	○	×	○	×

Legend: × = switch is off, ○ = switch is switching at high-frequency

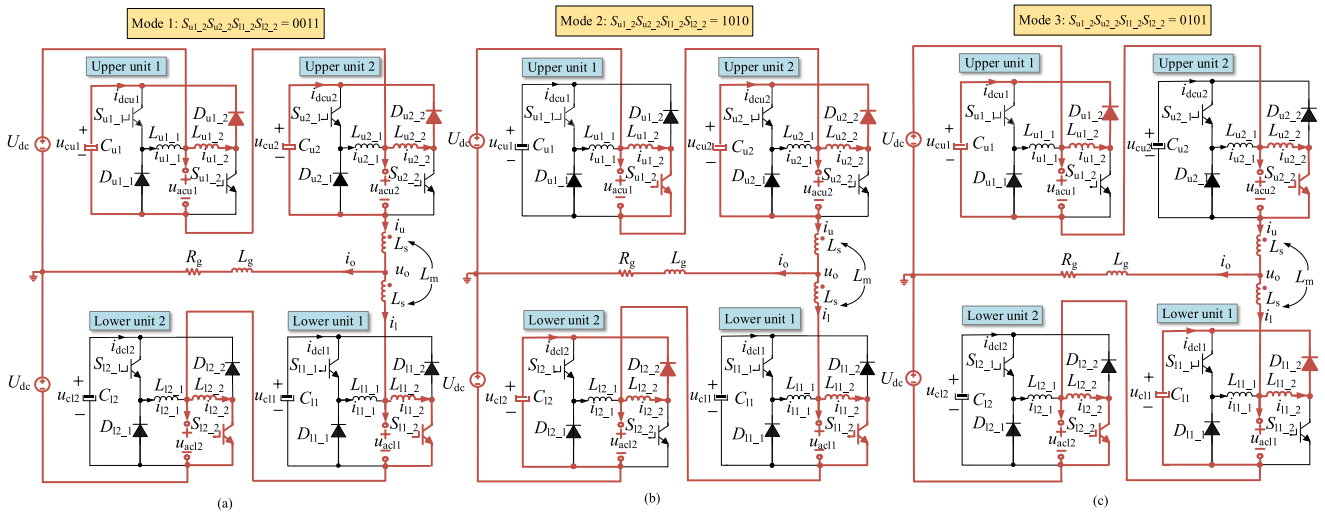

FIGURE 4. Current paths for switching stage I with NIPSDM scheme. (a) Mode 1, (b) Mode 2, (c) Mode 3 (same as Mode 1 and Mode 5 for IPSDM scheme).

$2\pi/N$ angle shifts, respectively, providing high effective switching frequency and even switching stresses and losses distribution across the submodules. Conversely, the nipsdm scheme adopts a zero phase-shift angle to the two groups of carriers in the upper and lower arms. As a result, during switching stage I, both upper and lower arm mmdbi submodules operate with their right buck cell conducting, with the arm current being equal to the current flowing through L_{jn_2} within each submodule, viz. $i_{jn\_2} = i_{jn}$ (j = u, l), whereas the current flowing through L_{jn_1} within each submodule is zero since diode D_{jn_1} is reverse biased, and as a consequence, the submodule circulating current is zero. Fig. 4 illustrates the various current paths for the NIPSDM scheme, for switching stage I, according to the operating modes defined as follows.

Mode 1: S_{l1_2} and S_{l2_2} are both on, D_{u1_2} and D_{u2_2} are both forward-biased and carry the freewheeling current. Capacitors C_{u1} and C_{u2} charge up while the other two capacitors retain their charge. Also, $u_u = 2U_{dc}$, $u_l = 0$, $u_o = U_{dc}$ and $u_{cm} = U_{dc}$. The rate of change of the arm currents and common-mode and differential-mode quantities are

$$\frac{di_{cm}}{dt} = \frac{1}{2}\left(\frac{di_u}{dt} + \frac{di_l}{dt}\right) \quad \frac{di_{dm}}{dt} = \frac{1}{2}\left(\frac{di_u}{dt} - \frac{di_l}{dt}\right) \tag{10}$$

From the current paths indicated in red in Fig. 4, the rate of change of upper, lower, common-mode, and differential-mode currents can be defined as

$$\frac{di_u}{dt} = \frac{U_{dc} + u_o}{B} \quad \frac{di_l}{dt} = \frac{-U_{dc} - u_o}{B} \tag{11}$$

$$\frac{di_{cm}}{dt} = 0 \quad \frac{di_{dm}}{dt} = \frac{U_{dc} + u_o}{B} \tag{12}$$

where $A = L_m + 2L_{sm} + L_s$ and $B = L_m - (2L_{sm} + L_s)$.

Mode 2: S_{u1_2} and S_{l1_2} are both on, D_{u2_2} and D_{l2_2} are both forward-biased and carry the freewheeling current. Capacitors C_{u2} and C_{l2} charge up while capacitors C_{u1} and C_{l1} retain their charge. Also, $u_u = U_{dc}$, $u_l = U_{dc}$, $u_o = 0$ and $u_{cm} = U_{dc}$. Current slopes in this mode can be expressed as

$$\frac{di_u}{dt} = \frac{u_o}{B} \quad \frac{di_l}{dt} = \frac{-u_o}{B} \tag{13}$$

$$\frac{di_{cm}}{dt} = 0 \quad \frac{di_{dm}}{dt} = \frac{u_o}{B} \tag{14}$$

Mode 3: S_{u2_2} and S_{l2_2} are both on, D_{u1_2} and D_{l1_2} are both forward-biased and carry the freewheeling current. Capacitors C_{u1} and C_{l1} charge up while C_{u2} and C_{l2} retain their charge. Also, $u_u = U_{dc}$, $u_l = U_{dc}$, $u_o = 0$ and $u_{cm} = U_{dc}$ and the current slopes are the same as for Mode 2.

C. INTERLEAVED PHASE-SHIFTED DISCONTINUOUS MODULATION SCHEME (IPSDM)

The use of an interleaved phase-shifted angle π/N between upper and lower arm carriers doubles the operating modes and increases the effective switching frequency of the phase-leg inductors in each submodule by $2N$ times without increasing the switching frequency of semiconductor devices. This allows reducing the volume of the passive filtering components. Fig. 5 illustrates the various current paths for the IPSDM scheme, for switching stage I, according to the operating modes defined as follows.

Mode 1: This mode is the same as Mode 3 for NIPSDM at switching stage I.

Mode 2: S_{l2_2} is on, D_{u1_2}, D_{u2_2}, and D_{l1_2} are all forward-biased and carry the freewheeling current. Capacitors C_{u1}, C_{u2}, and C_{l1} charge up while C_{l2} retains its charge. Also, $u_u = 2U_{dc}$, $u_l = U_{dc}$, $u_o = -U_{dc}/2$ and $u_{cm} = 3U_{dc}/2$. From the current paths indicated in red in Fig. 5, the rate of change of upper, lower, common-mode, and differential-mode currents can be expressed as

$$\frac{di_u}{dt} = \frac{\frac{A-B}{2}U_{dc} + Au_o}{AB} \quad \frac{di_l}{dt} = \frac{-\frac{A+B}{2}U_{dc} - Au_o}{AB} \tag{15}$$

$$\frac{di_{cm}}{dt} = \frac{-U_{dc}}{2A} \quad \frac{di_{dm}}{dt} = \frac{\frac{1}{2}U_{dc} + u_o}{B} \tag{16}$$

Mode 3: S_{u1_2} and S_{l2_2} are both on, D_{u2_2} and D_{l1_2} are both forward-biased and carry the freewheeling current. Capacitors C_{u2} and C_{l1} charge up while C_{u1} and C_{l2} retain their charge. Also, $u_u = U_{dc}$, $u_l = U_{dc}$, $u_o = 0$ and $u_{cm} = U_{dc}$. Current slopes are the same as for Mode 1.

Mode 4: S_{u1_2}, S_{l1_2}, and S_{l2_2} are all on, D_{u2_2} is forward-biased and carries the freewheeling current. Capacitor C_{u2} charge up while C_{u1}, C_{l1} and C_{l2} retain their charge. Also, $u_u = U_{dc}$, $u_l = 0$, $u_o = -U_{dc}/2$ and $u_{cm} = U_{dc}/2$. Current slopes can be defined as

$$\frac{di_u}{dt} = \frac{\frac{A+B}{2}U_{dc} + Au_o}{AB} \quad \frac{di_l}{dt} = \frac{-\frac{A-B}{2}U_{dc} - Au_o}{AB} \tag{17}$$

$$\frac{di_{cm}}{dt} = \frac{U_{dc}}{2A} \quad \frac{di_{dm}}{dt} = \frac{\frac{1}{2}U_{dc} + u_o}{B} \tag{18}$$

Mode 5: This mode is the same as Mode 3 for NIPSDM at switching stage I.

Mode 6: S_{l1_2} is on, D_{u1_2}, D_{u2_2}, and D_{l2_2} are all forward-biased and carry the freewheeling current. Capacitors C_{u1}, C_{u2}, and C_{l2} charge up while C_{l1} retains its charge. Also, $u_u = 2U_{dc}$, $u_l = U_{dc}$, $u_o = -U_{dc}/2$ and $u_{cm} = 3U_{dc}/2$. Current slopes in this mode are the same as for Mode 2.

Mode 7: S_{u2_2} and S_{l1_2} are both on, D_{u1_2} and D_{l2_2} are both forward-biased and carry the freewheeling current. Capacitors C_{u1} and C_{l2} charge up while C_{u1} and C_{l1} retain their charge. Also, $u_u = U_{dc}$, $u_l = U_{dc}$, $u_o = 0$ and $u_{cm} = U_{dc}$. Current slopes in this mode are the same as for Mode 3.

Mode 8: S_{u2_2}, S_{l1_2}, and S_{l2_2} are all on, D_{u1_2} is forward-biased and carries the freewheeling current. Capacitors C_{u1} charge up while C_{u2}, C_{l1}, and C_{l2} retain their charge. Also, $u_u = U_{dc}$, $u_l = 0$, $u_o = -U_{dc}/2$ and $u_{cm} = U_{dc}/2$. Current slopes in this mode are the same as for Mode 4.

Note that during switching stage I, only one controllable semiconductor device switches on or off within each operating mode, while all other switching devices retain their previous individual states. In addition, the switches within the lower arm submodules only conduct after all switches in the upper arm submodules have operated (i.e. have turned on or off). The number of on-state switches varies as $N, N-1, N+1$, and back to n, while the switched output voltage changes back and forth between 0 and $-0.5U_{dc}$.

The analysis of the operating modes for switching stages II, III, and IV has been performed using similar reasoning, with the results being here omitted for brevity.

IV. ADJUSTABLE DISCONTINUOUS MODULATION

Same as for the conventional dual buck converter, when the MMDBI topology operates with discontinuous modulation (NIPSDM OR IPSDM), upper and lower arm current ripples at zero-crossings are nonzero, and this causes undesirable current zero-crossing distortion, which needs to be managed. This section introduces an adjustable discontinuous modulation scheme that effectively mitigates the current zero-crossing distortion in the MMDBI topology and considerably enhances the converter power quality.

The modulation commands in the proposed discontinuous modulation strategy incorporate specific current thresholds, defined based on theoretical values of the arm ripple current, to enforce a minimum switching overlap period between the two buck cells that eliminates the zero-crossing current distortion.

A. CURRENT RIPPLE ANALYSIS

Current ripple needs to be appropriately managed for the synthesis of quality waveforms in power conversion systems. Section III has presented a detailed analysis of the current flow under various converter operating modes and has provided analytical expressions for the di_u/dt, di_l/dt, di_{cm}/dt and di_{dm}/dt slopes for each of these modes. For a given slope, the magnitude of the ripple current relates to the duration of each switching state, defined by the switching frequency and duty ratio. Since the modulation commands for upper and lower arms are 180° phase-shifted, duty ratios S_{un_2} and S_{ln_2} are complementary to each other, viz. $\delta_{un\_2} + \delta_{ln\_2} = 1$ with $n = \{1, 2\}$. For simplicity, consider that $\delta_{u1\_2} = \delta_{u2\_2} = \delta_{u\_2}$ and $\delta_{l1\_2} = \delta_{l2\_2} = \delta_{l\_2}$. Assuming the IPSDM scheme as an example, the time interval Δt for each operating mode within switching stage I is defined as $\Delta t_1 = (3/4 - \delta_{l\_2})T_s$

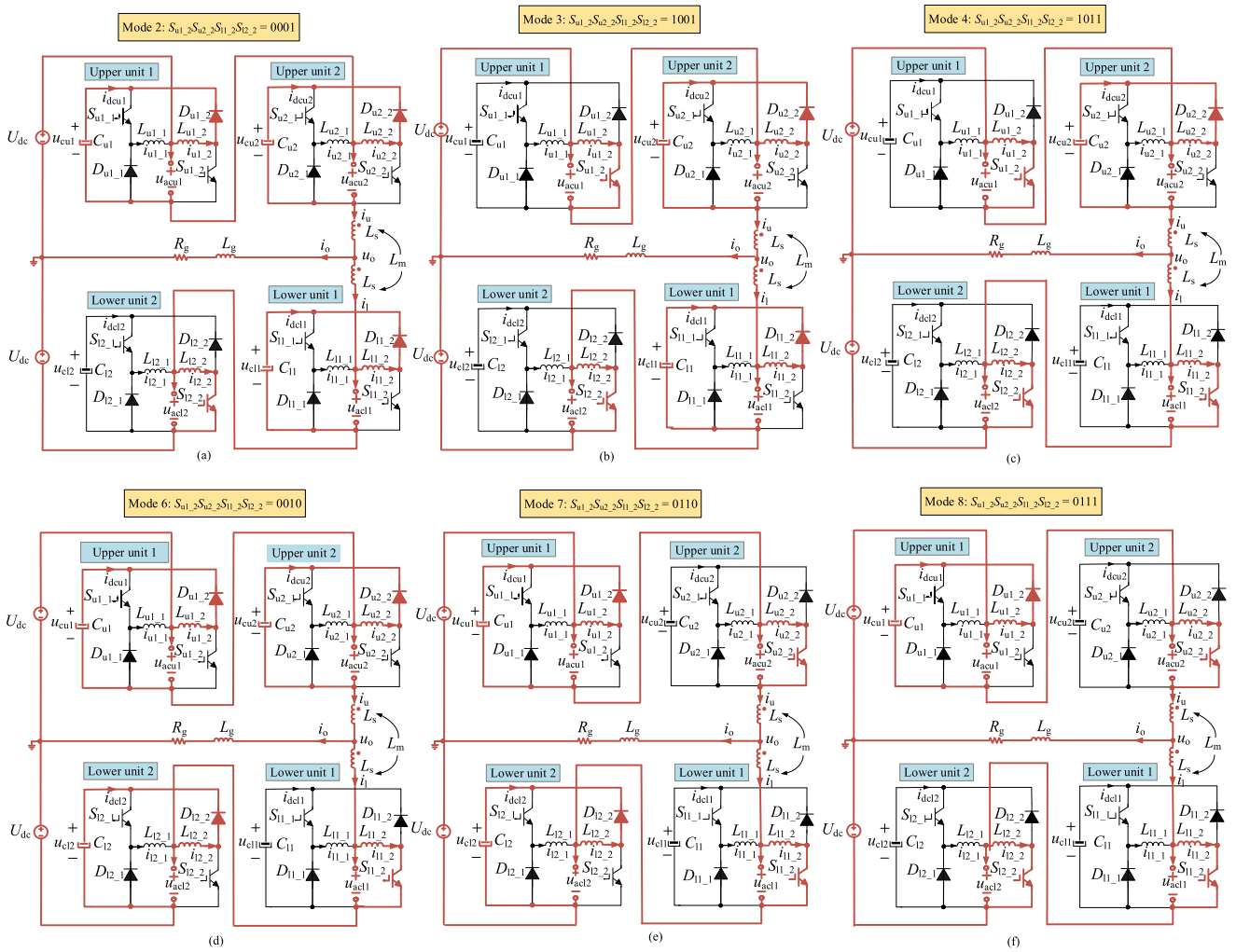

FIGURE 5. Current paths for switching stage I with IPSDM scheme. (a) Mode 2, (b) Mode 3, (c) Mode 4, (d) Mode 6, (e) Mode 7 and (f) Mode 8.

for the rise-time of i_{dm} (e.g. modes 1, 3, 5, and 7) and $\Delta t_2 = (\delta_{l\_2} - 1/2)T_s$ for the fall-time of i_{dm} (e.g. modes 2, 4, 6, and 8), where $\delta_{l\_2} \in [1/2, 3/4]$ and T_s denotes the switching period. As shown in Fig. 6, when i_o is negative (switching stages I and II), S_{ln_2} operates at high-frequency and the duty ratio δ_{l_2} changes continuously during this period and vice-versa.

1) COMMON-MODE CURRENT RIPPLE ANALYSIS

According to Eqn. (7), the common-mode current i_{cm} that flows through the phase-leg of MMDBI is controlled by the coupled arm inductance, upper half dc-link voltage and common-mode dc-side voltage, with the analytical expression for i_{cm} obtained by rewriting (7) as

$$i_{cm} \approx \frac{1}{L_k + 2L_m} \int (U_{dc} - u_{cm}) dt \tag{19}$$

From this expression, the common-mode current i_{cm} depends on the integral of the voltage difference between U_{dc} and u_{cm}. More specifically, if U_{dc} is larger than u_{cm} then i_{cm} has a positive slope, whereas if U_{dc} is smaller than u_{cm} then i_{cm} has a negative slope, and finally, if U_{dc} is equal to u_{cm} then i_{cm} remains constant. This means that for the switching combinations of each switching stage, as long as the sum of $S_{jn\_1} = 1$ and $S_{jn\_2} = 0$ with $n = \{1, 2, \ldots, N\}$ is equal to N, the submodule capacitor voltages match the overall dc-link voltage and the common-mode current remains constant within a switching cycle. However, if the sum of $S_{jn\_1} = 1$ and $S_{jn\_2} = 0$ with $n = \{1, 2, \ldots, N\}$ is larger than N, the energy-transferring submodules will transfer energy from their capacitors to the overall half dc-link capacitors and i_{cm} will reduce linearly and vice-versa.

Applying these principles to the NIPSDM and IPSDM schemes, a distinction is identified concerning the slope of i_{cm} within a switching period. More specifically, the common-mode current i_{cm} under NIPSDM is constant within each switching cycle, while the additional operating modes of the IPSDM scheme cause the rising-constant-decreasing pattern in the circulating current. Therefore, from the switch commands shown in Fig. 7, the common-mode ripple current

TABLE 2. Current ripples under IPSDM and NIPSDM schemes.

Switching Stage	NIPSDM		IPSDM	
	Δi_{cm_NI}	Δi_{dm_NI}	Δi_{cm_I}	Δi_{dm_I}
Stage I $\delta_{l\_2}\in[1/2,3/4]$	0	$K\frac{U_{dc}+u_o}{B}\left(\delta_{l\_2}-\frac{1}{2}\right)T_s$	$K\frac{\pm U_{dc}}{2A}\left(\delta_{l\_2}-\frac{1}{2}\right)T_s$	$K\frac{\frac{1}{2}U_{dc}+u_o}{B}\left(\delta_{l\_2}-\frac{1}{2}\right)T$
Stage II $\delta_{l\_2}\in[3/4,(1+M)/2]$			$K\frac{\pm U_{dc}}{2A}(1-\delta_{l\_2})T_s$	$K\frac{\frac{1}{2}U_{dc}+u_o}{B}(1-\delta_{l\_2})T_s$
Stage III $\delta_{u\_2}\in[1/2,3/4]$	0	$K\frac{U_{dc}+u_o}{B}\left(\delta_{u\_2}-\frac{1}{2}\right)T_s$	$K\frac{\pm U_{dc}}{2A}\left(\delta_{u\_2}-\frac{1}{2}\right)T_s$	$K\frac{\frac{1}{2}U_{dc}+u_o}{B}\left(\delta_{u\_2}-\frac{1}{2}\right)T_s$
Stage IV $\delta_{u\_2}\in[3/4,(1+M)/2]$			$K\frac{\pm U_{dc}}{2A}(1-\delta_{u\_2})T_s$	$K\frac{\frac{1}{2}U_{dc}+u_o}{B}(1-\delta_{u\_2})T_s$

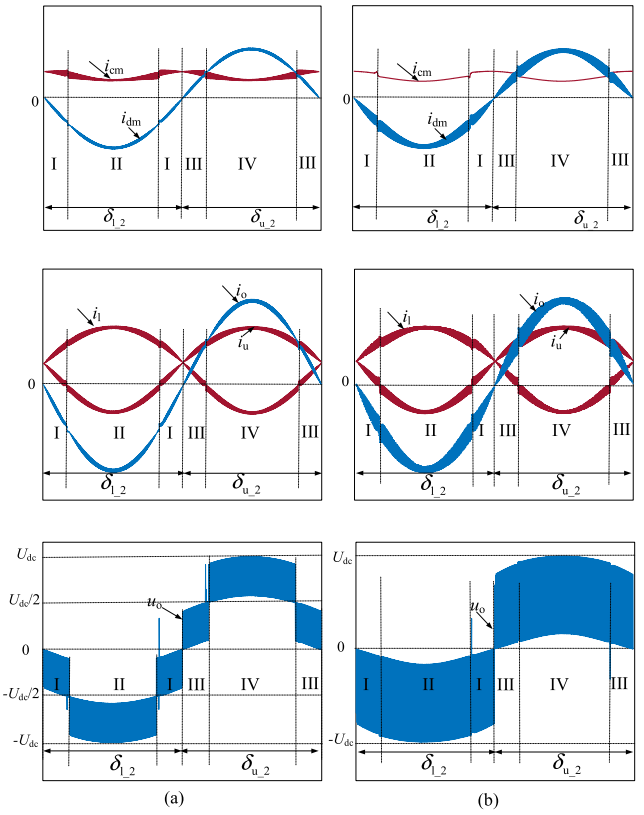

FIGURE 6. Simulation waveforms of arm currents i_u, i_l, common-mode and differential-mode currents i_{cm}, i_{dm}, and output voltage and current u_o, i_o of the proposed MMDBI ($N = 2$). (a) IPSDM, (b) NIPSDM.

within switching stage I of NIPSDM scheme is defined as

$$\Delta i_{cm\_NI} = 0 \tag{20}$$

Similarly, as illustrated in Fig. 8, i_{cm} falls or rises during the falling intervals of i_{dm}, whereas i_{cm} remains constant during the rising intervals of i_{dm}. Therefore, the common-mode ripple current within switching stage I of IPSDM scheme can be derived as

$$\Delta i_{cm\_I} = K\frac{\pm U_{dc}}{2A}\left(\delta_{l\_2}-\frac{1}{2}\right)T_s \tag{21}$$

where K provides an appropriate safety margin for the correct operation, with K usually set as 1.1 to 1.5.

2) DIFFERENTIAL-MODE CURRENT RIPPLE ANALYSIS

The differential-mode current ripple during switching stage I of NIPSDM scheme can be expressed as:

$$\Delta i_{dm\_NI} = K\frac{U_{dc}+u_o}{B}\left(\delta_{l\_2}-\frac{1}{2}\right)T_s \tag{22}$$

When compared to the NIPSDM scheme, the IPSDM approach has twice the number of switching states. Consequently, the differential-mode current ripple during switching stage I of IPSDM scheme is readily found as

$$\Delta i_{dm\_I} = K\frac{\frac{1}{2}U_{dc}+u_o}{B}\left(\delta_{l\_2}-\frac{1}{2}\right)T_s \tag{23}$$

A summary of the common-mode and differential-mode current ripples for the NIPSDM and IPSDM schemes is provided in Table 2. Considering the double effective switching frequency achieved by the IPSDM approach, the differential-mode ripple current is greatly reduced under this modulation strategy. In addition, for the IPSDM scheme there are two differential-mode (output current) ripples within the positive half-cycle, and the ripple approaches to zero when $\delta_{l\_2} = 3/4$ (i.e. zero-crossing of i_u) and $\delta_{l\_2} = 1/2$ (i.e. zero-crossing of i_o), respectively. This means that the differential-mode ripple current reduction takes place at the boundaries of the four switching stages. However, when it comes to the NIPSDM scheme, only one differential-mode current ripple exists throughout the positive half-cycle, and the ripple is zero when $\delta_{l\_2} = 1/2$ (i.e. zero-crossing of i_o).

Based on this analysis, there is a compromise between reducing the differential-mode ripple current at the expense of increasing the common-mode ripple current.

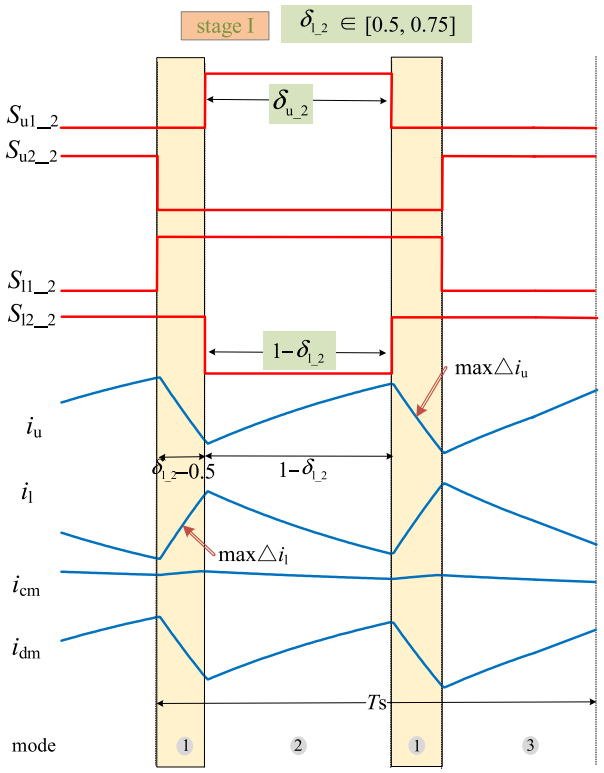

FIGURE 7. Switch commands for the NIPSDM scheme when S_{u_2} and S_{l_2} operate at high-frequency and resulting converter currents.

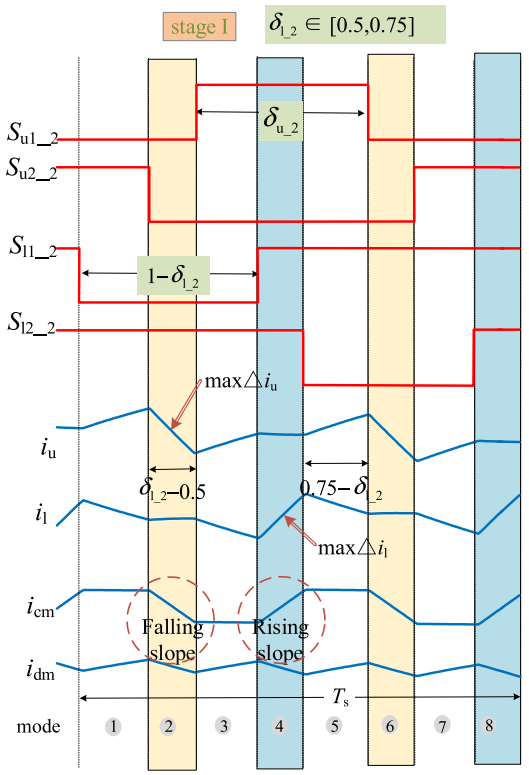

FIGURE 8. Gate signals for IPSDM scheme when S_{u_2} and S_{l_2} operate at high-frequency and resulting converter currents.

B. CURRENT ZERO-CROSSING DISTORTION ANALYSIS

When operating with a discontinuous modulation scheme (NIPSDM or IPSDM) with zero threshold (under the assumption that the current zero-crossing point is known as illustrated in Fig. 9(a)), the MMDBI topology presents current zero-crossing distortion during changes of the arm current polarity, and this effect is more severe for lower converter switching frequencies. Since the current ripple has opposite polarities around the zero-crossing point, this inevitably produces an unpredictable jump in the arm current and a large voltage overshoot (as shown in Fig. 6). This reduces the converter power quality and decreases the converter efficiency, particularly when the load power factor is relatively low and the ripple current is large because of capacitor voltage fluctuation during power exchange.

A possible strategy to manage the zero-crossing current distortion is to deliberately command both buck cell switches on for a short period of overlap time during arm current zero-crossing events. Consider for example the upper arm current i_u depicted in Fig. 9(b), where gray dashed boxes indicate overlap switching periods, achieved by turning S_{un_1} on when the positive average current Δi (e.g. half the maximum upper arm current ripple) is larger than the sampled value i_{u_avg} and turning S_{un_2} on when the negative average current $-\Delta i$ is smaller than the sampled value i_{u_avg}. In other words, S_{un_1} and S_{un_2} conduct simultaneously near the upper arm current zero-crossing zone, viz. $-\Delta i < i_{u\_avg} < \Delta i$, hence an adjustable overlap in their operating range in $m = \mathrm{M}\sin(\omega t)$ (where M is the amplitude of the modulation command m) is enforced (see green and blue shaded area in Fig. 9). However, as shown in Fig. 9(a), the use of a zero-threshold value is ineffective to deal with current zero-crossing distortions as the current ripple near zero-crossings is ignored without the appropriate current threshold comparison. Furthermore, since for a MMDBI the current zero-crossing point varies depending on the circulating current, a suitable current detection method is required, as it will be discussed in the following sub-section.

C. DESIGN OF ADJUSTABLE CURRENT THRESHOLD FOR DISCONTINUOUS MODULATION SCHEMES

Fig. 10 schematically illustrates the proposed adjustable zero-crossing current threshold circuit, where the sampled value of arm current is compared to the calculated average current ripple to generate the enabling signals E_{j_1} and E_{j_2}. Recall that for the IPSDM scheme the $\Delta i_{\mathrm{umax\_I}}$ occurs at the falling intervals of common-mode and differential-mode currents (as illustrated in Fig. 8). In addition, Δi_u during both falling and rising periods are identical for the NIPSDM scheme, therefore the falling interval can be assumed as $\Delta i_{\mathrm{umax\_NI}}$ (refer to Fig. 9 for details). Therefore, the maximum arm current ripples for the IPSDM and NIPSDM schemes can be calculated as

$$\Delta i_{\mathrm{umax\_I}} = K\frac{\frac{\mathrm{A-B}}{2}U_{\mathrm{dc}} + \mathrm{A}u_{\mathrm{o}}}{\mathrm{AB}}\left(\delta_{l\_2} - \frac{1}{2}\right)T_{\mathrm{s}} \quad (24)$$

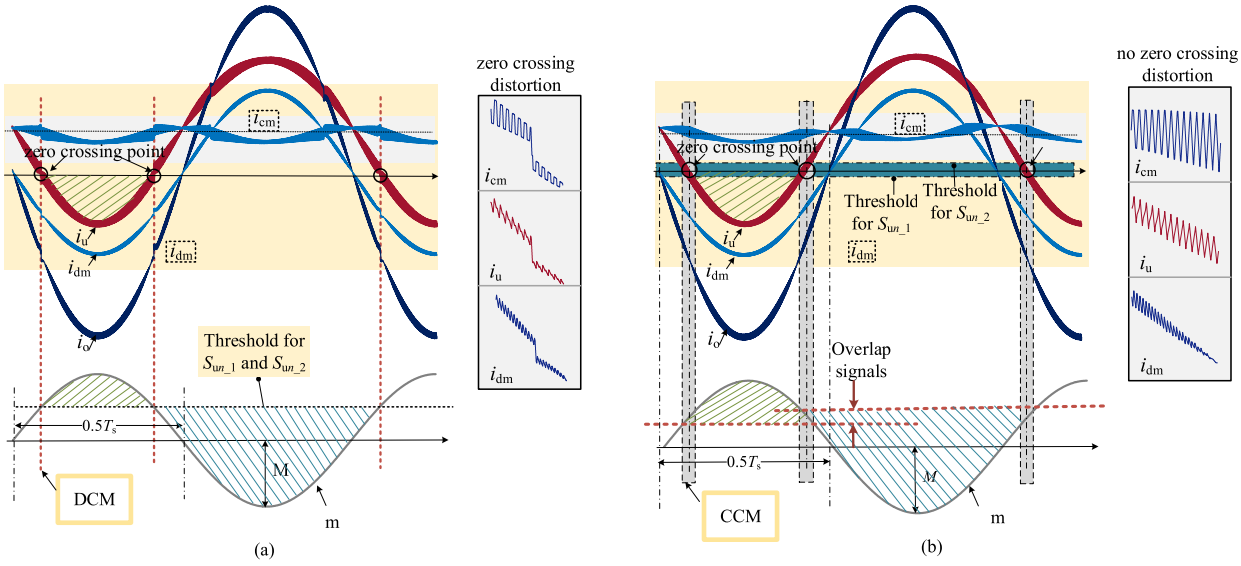

FIGURE 9. Arm current threshold detection principle at zero crossing points. (a) zero threshold, and (b) adjustable threshold.

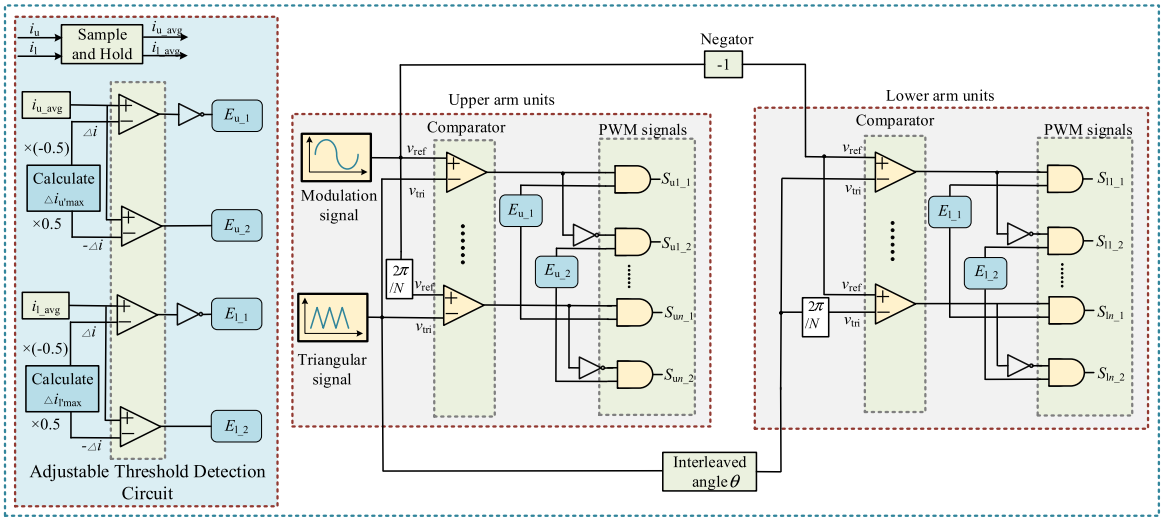

FIGURE 10. Schematic diagram of the adjustable discontinuous modulation strategies applied to the MMDBI system.

$$\Delta i_{\mathrm{umax\_NI}} = K\frac{U_{\mathrm{dc}} + u_{\mathrm{o}}}{\mathrm{B}}\left(\delta_{\mathrm{l\_2}} - \frac{1}{2}\right)T_{\mathrm{s}} \tag{25}$$

Same analysis can be applied to ΔI_{lmax}. Gate driver commands to the power switches are then produced by the AND logic operation between the threshold detection signals and the bipolar PWM signals (which originate from comparison between modulation commands and phase-shifted carrier signals). Note that the adjustable discontinuous modulation creates additional switching stages that occur during the short overlap period of the switching commands. However, as the strategy produces a minimal overlap period, the duration of these additional stages is quite short and as such they can be safely neglected.

V. SIMULATION INVESTIGATION

The concepts presented in this paper have been extensively investigated using detailed PSIM switching models, for a two cells per arm ($N = 2$) MMDBI with parameters listed in Table 3.

Two current threshold values, for both IPSDM and NIPSDM discontinuous modulation schemes, are considered in the analysis (namely, zero and theoretical), as discussed in the following sub-sections.

A. RESULTS FOR IPSDM AND NIPSDM SCHEMES WITH ZERO CURRENT THRESHOLD

simulation waveforms of the proposed MMDBI topology operating under IPSDM and NIPSDM discontinuous

TABLE 3. System parameters of the proposed MMDBI under discontinuous modulation.

Symbol	Quantity	Value
U_{dc}	dc side power supply	150 V
f_o	fundamental frequency	50 Hz
f_c	carrier frequency	10 kHz
M	modulation depth	0.8
C	dc-link capacitor on each module	940 μF
L_g	load inductance	5 mH
R_g	load resistance	8 Ω, 50 Ω
N	number of cells per arm	2
L_m, L_k	mutual and leakage inductance of arm coupled inductor	1.9 mH, 0.1 mH
R_s	resistance of arm inductor	200 mΩ
L_1, L_2	phase-leg inductor of each module	0.3 mH

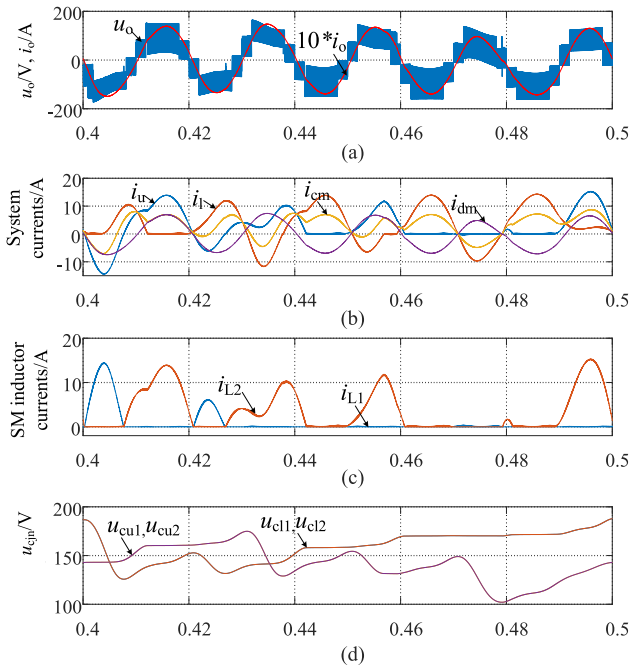

FIGURE 11. Simulation waveforms of MMDBI with zero current threshold under IPSDM ($N = 2$, $f_c = 10kHz$, $R_g = 8\Omega$). (a) Output voltage u_o and output current i_o. (b) Upper arm current i_u, lower arm current i_l, common-mode current i_{cm} and differential mode current i_{dm}. (c) Dual buck cell phase-leg currents i_{jn_1} and i_{jn_2}. (d) SM capacitor voltages u_{cu1}, u_{cu2}, u_{cl1} and u_{cl2}.

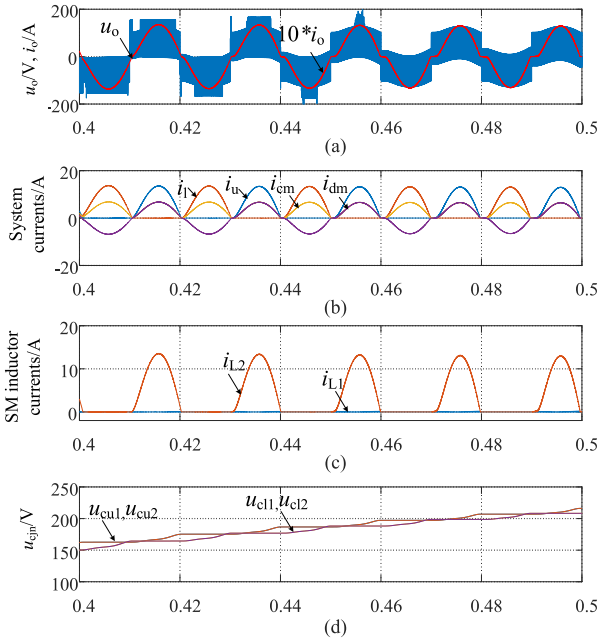

FIGURE 12. Simulation waveforms of MMDBI with zero current threshold under NIPSDM ($N = 2$, $f_c = 10kHz$), $R_g = 8\Omega$. (a) Output voltage u_o and output current i_o. (b) Upper arm current i_u, lower arm current i_l, common-mode current i_{cm} and differential mode current i_{dm}. (c) Dual buck cell phase-leg currents i_{jn_1} and i_{jn_2}. (d) SM capacitor voltages u_{cu1}, u_{cu2}, u_{cl1} and u_{cl2}.

modulation schemes with a zero current threshold value are shown in Fig. 11 and Fig. 12, respectively. from these figures, arm currents i_u and i_l and their common-mode i_{cm} and differential-mode i_{dm} representations contain undesirable irregularity, with the dual buck submodule phase-leg inductor currents i_{jn_1} and i_{jn_2} losing their complementarity within a fundamental cycle. This irregular behavior is likely caused by the presence of ripple in the arm currents, which causes multiple zero-crossing events and several comparisons with the zero-threshold boundary. This leads to submodules capacitor voltage unbalance as shown in Figs. 11(d) and 12(d) and should be avoided for safe operation.

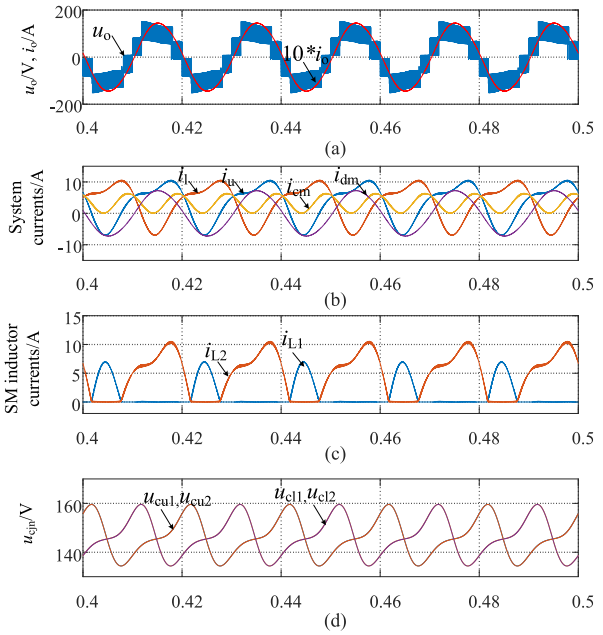

FIGURE 13. Simulation waveforms of MMDBI with theoretical current threshold to be 0.17A under IPSDM ($N = 2$, f_c =10kHz, R_g=8Ω). (a) Output voltage u_o and output current i_o. (b) Upper arm current i_u, lower arm current i_l, common-mode current i_{cm} and differential mode current i_{dm}. (c) Dual buck cell phase-leg currents i_{jn_1} and i_{jn_2}. (d) SM capacitor voltages u_{cu1}, u_{cu2}, u_{cl1} and u_{cl2}.

B. RESULTS FOR IPSDM AND NIPSDM SCHEMES WITH THEORETICAL CURRENT THRESHOLD

Fig. 13 and Fig. 14 Present waveforms for operation under IPSDM and NIPSDM schemes with theoretical current

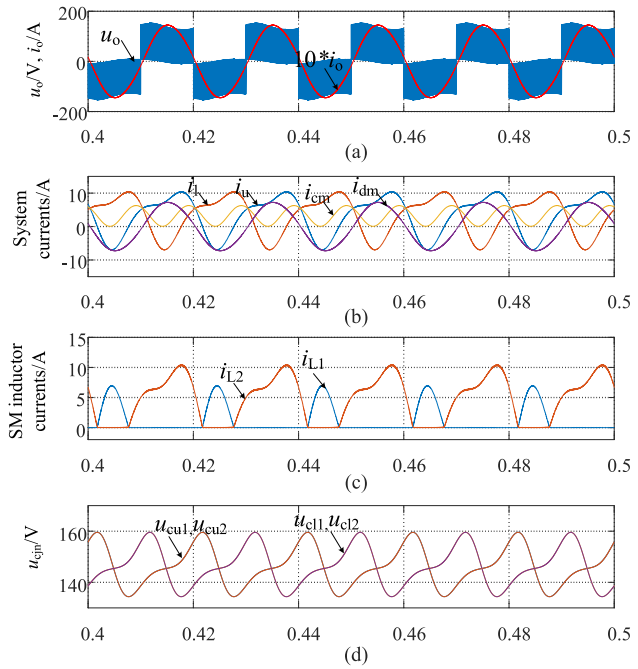

FIGURE 14. Simulation waveforms of MMDBI with current threshold to be 0.28A under NIPSDM ($N = 2$, $f_c = 10$kHz, R_g= 8 Ω). (a) Output voltage u_o and output current i_o. (b) Upper arm current i_u, lower arm current i_l, common-mode current i_{cm} and differential mode current i_{dm}. (c) Dual buck cell phase-leg currents i_{jn_1} and i_{jn_2}. (d) SM capacitor voltages u_{cu1}, u_{cu2}, u_{cl1} and u_{cl2}.

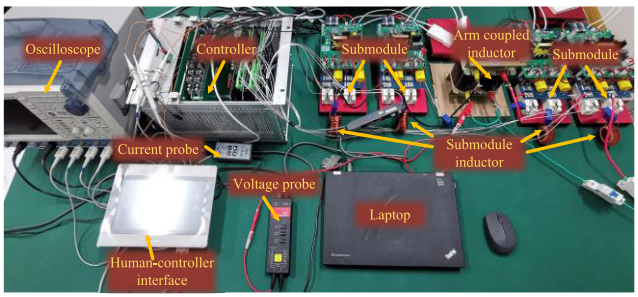

FIGURE 15. Experimental setup.

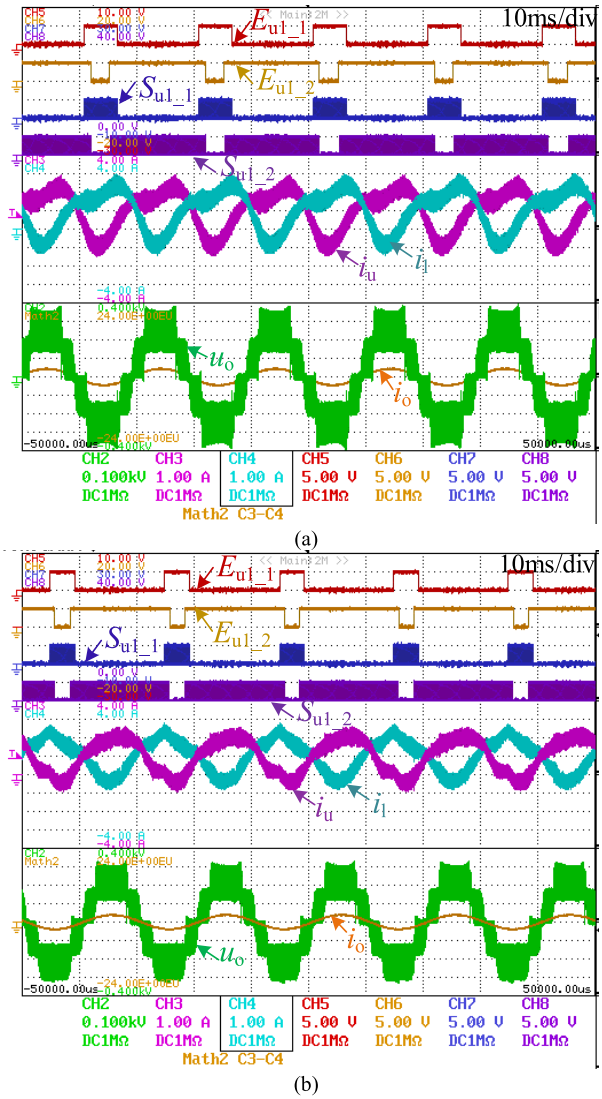

FIGURE 16. Steady-state waveforms of system variables for $R_g = 50$ Ω. (a) operation with ideal current threshold to be 0.44A, (b) operation with non-ideal current threshold.

thresholds, calculated from EQNS. (24) and(25), AS 0.17 A and 0.28 A, respectively. From these plots, The switched output voltage u_o presents five ($2N + 1$) distinct levels ($-U_{dc}$, $-U_{dc}/2$, 0, $U_{dc}/2$ and U_{dc}) for the IPSDM scheme, and only three voltage levels ($-U_{dc}$, 0, and U_{dc}) for the NIPSDM scheme, as expected (see Fig. 13(a) and Fig. 14(a) for details). Furthermore, the ac-side differential (output) current i_{dm} has a symmetrical sinusoidal shape, free of any dc offset. From Fig. 13(b) and Fig. 14(b), the ac-side current ripples are relatively larger for the NIPSDM scheme compared to the IPSDM scheme, and this is in agreement with the theoretical ripple analysis presented in Section IV. In addition, the common-mode ripple current for the IPSDM scheme is larger and contains high-frequency components due to the variable common-mode voltage. Note that the arm currents i_u and i_l have a dc bias, caused by the inherent circulating current present in MMDBI, which also produces an asymmetry in the dual buck cell phase-leg currents i_{jn_1} and i_{jn_2}, as shown in Fig. 13(c) and Fig. 14(c).

Careful inspection of the waveforms presented in Fig. 13 and Fig. 14 indicates that the proposed modulation strategy with adjustable current threshold eliminates the zero-crossing current distortion by enforcing the combined operation of both buck cells for an appropriately short time period via calculation of the maximum arm current ripples in the vicinity of the current zero-crossing events. Furthermore, when the theoretical threshold is adopted, the submodule capacitor voltages under both IPSDM and NIPSDM schemes are well balanced around 150 V, as can be seen from Figs. 13(d) and 14(d).

VI. EXPERIMENTAL VALIDATION

The adjustable discontinuous modulation scheme proposed in this work has been validated using the MMDBI laboratory prototype depicted in Fig. 15, with experimental parameters

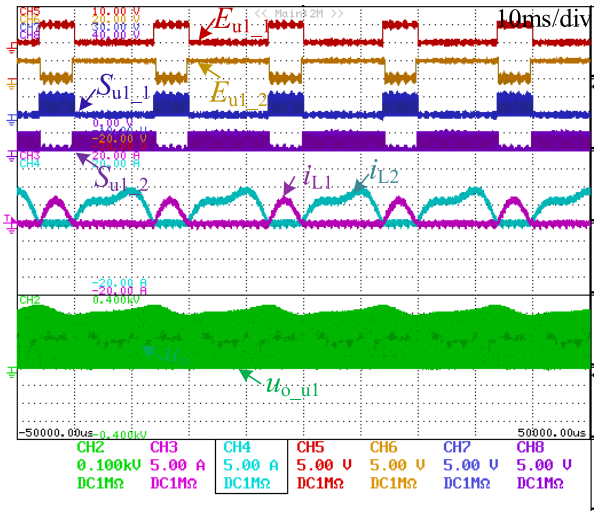

FIGURE 17. Steady-state threshold comparison enabling signals E_{u1_1}, E_{u1_2}, gate signals S_{u1_1}, S_{u1_2}, phase-leg inductor currents i_{jn_1}, i_{jn_2} and terminal output voltage u_{o_u1} of the upper arm submodule u1 when $R_g = 8\ \Omega$.

matching the simulated ones, except for the ac-side load resistance $R_g = \{50\ \Omega, 8\ \Omega\}$, which has been chosen to verify the system performance under different load conditions. For brevity, only the waveforms for the IPSDM scheme are provided as an example, with the interleaved angle set as $\theta = \pi/2$. Note that as the zero threshold causes irregular arm currents and unbalanced capacitor voltages (as can be seen from Fig. 11 and 12), this operating condition could not be demonstrated experimentally, as it consistently triggered overvoltage hardware protection. Instead, a non-ideal threshold (between zero and ideal) was adopted to illustrate the converter performance while achieving stable operation.

A. RESULTS FOR STEADY-STATE OPERATION WITH LOAD RESISTOR $R_g = 50\Omega$

The adjustable threshold detection scheme uses two threshold detection enabling signals E_{jn_1} and E_{jn_2}. These signals are incorporated into the PWM gate signals S_{u1_1} and S_{u1_2} that drive the dual buck phase-leg switches in the upper arm of MMDBI, to achieve a short target overlap period that effectively mitigates the current zero-crossing distortion. As depicted in Fig. 16(a), the MMDBI arm currents i_u and i_l transit smoothly during zero-crossings when adopting the threshold value calculated as 0.44 A from Eqn. (24), whereas as shown in Fig. 16(b), a deficient threshold value causes undesirable threshold comparison away from the zero-crossing region.

B. RESULTS FOR STEADY-STATE OPERATION WITH LOAD RESISTOR $R_g = 8\Omega$

This section provides a set of steady-state experimental waveforms (see Figs. 17-19) for inverter operation with load resistance R_g of 8 Ω. The presence of the double line frequency circulating harmonic components produces a small pulsation in the arm currents i_u and i_l, which can be minimized by

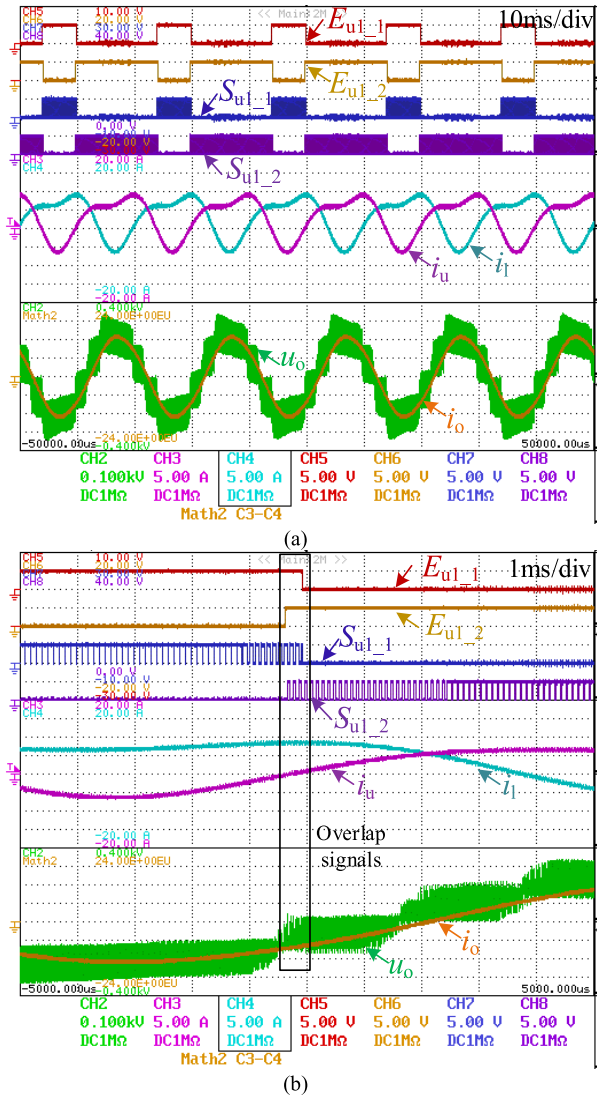

FIGURE 18. Steady-state waveforms of system variables for $R_g = 8\ \Omega$. (a) operation with ideal current threshold (0.36 A), (b) zoom of (a).

incorporating circulating current suppression strategies or using larger capacitors. Fig. 17 shows the asymmetry of the submodule u_1 phase-leg currents i_{L1} and i_{L2} caused by the dc bias in the MMDBI arm currents i_u and i_l. This figure also shows the submodule output voltage u_{o_u1}, with two levels, as expected for operation under IPSDM discontinuous modulation. Fig. 18 shows that when the current threshold (calculated as 0.36 A) is used, the zero-crossing distortion is adequately suppressed. In contrast, as shown in Fig. 19(b), a non-ideal current threshold results in irregularities for both upper and lower arm currents. However, further investigations with the use of smaller power factor (and further suppression of the current ripple) allows the use of a same threshold width with effective current zero-crossing suppression on both arms.

C. RESULTS FOR DYNAMIC OPERATION

Fig. 20 provides experimental waveforms that illustrate the dynamic response of MMDBI system for a load change (from

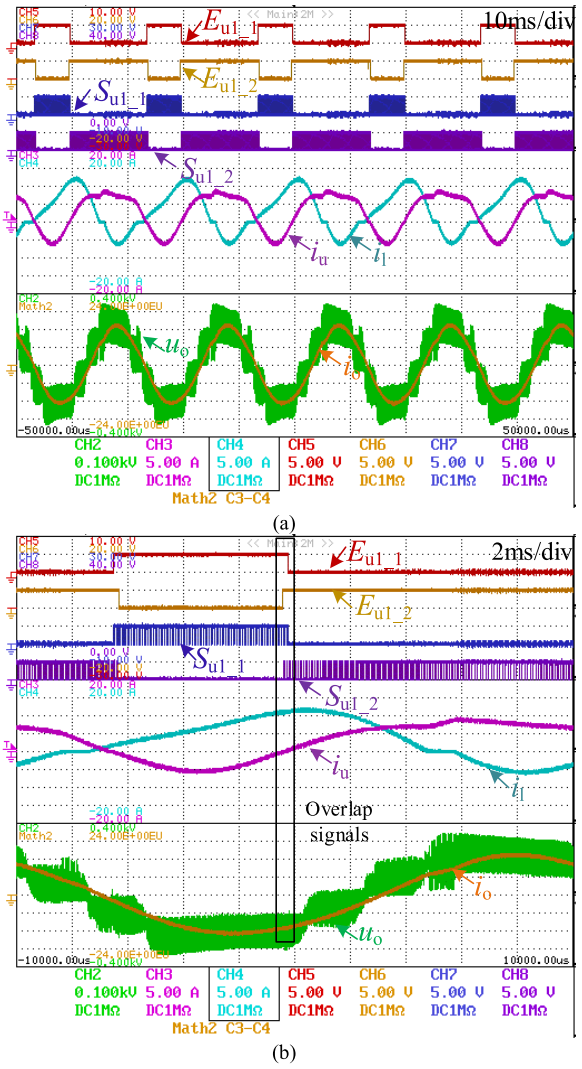

FIGURE 19. Steady-state waveforms of system variables for $R_g = 8\ \Omega$. (a) operation with non-ideal current threshold, (b) zoom of (a).

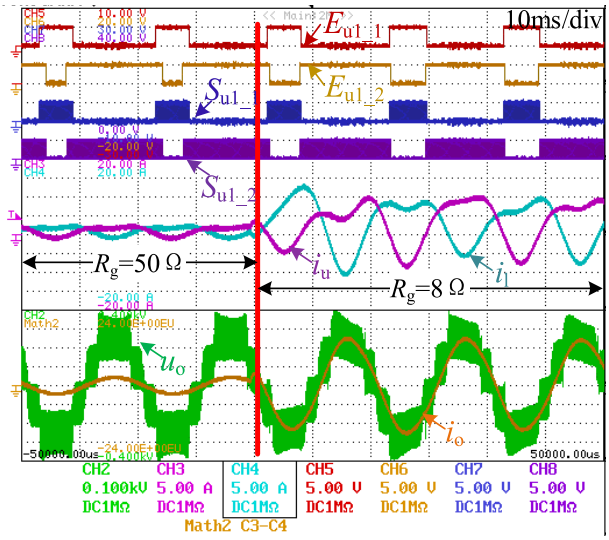

FIGURE 20. Dynamic performance when the load resistance changes from $R_g = 50\ \Omega$ to $R_g = 8\ \Omega$.

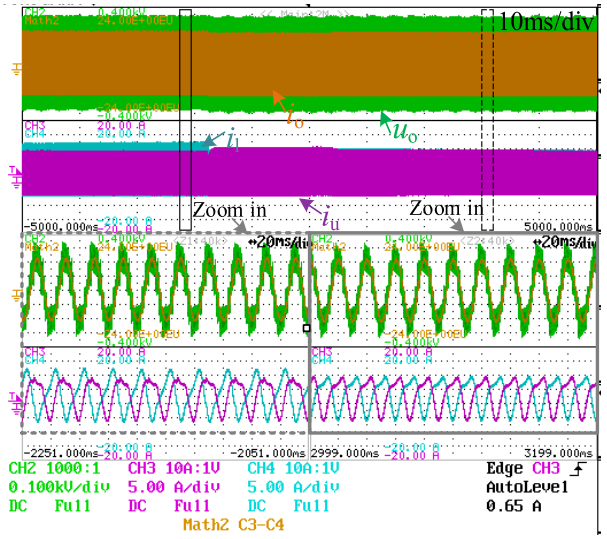

FIGURE 21. Dynamic performance when the current threshold value changes from non-ideal to ideal.

light to heavy load), with the modulation strategy implemented according to the scheme depicted in Fig. 10. Note that the arm currents i_u and i_l and the ac-side output current i_o and voltage u_o return to a new steady-state condition after a short transient period.

In addition, Fig. 21 shows the dynamic converter performance for a threshold width change from non-ideal to ideal width. The zoomed view at the bottom of Fig. 21 illustrates the beneficial effect that an appropriate threshold width has on the system performance. all in all, these results demonstrate the fast-dynamic response achieved by the proposed methodology. The small mismatches between simulation and experimental waveforms are caused by second-order practical effects such as IGBT device voltage drops and electromagnetic disturbance.

D. FURTHER COMPARISON BETWEEN SIMULATION AND EXPERIMENTAL RESULTS

Harmonic spectra of the output current and voltage, for converter operation with IPSDM modulation strategy, for both simulation and experiment, are provided in Fig. 22. Careful inspection of this figure indicates that the overall results predicted by simulation are in good agreement with experimental measurements, except for the baseband harmonics, which are a little larger for the experimental results, and produce a slightly larger output voltage weighted thd for experiment (1.11%), compared to simulation (0.75%). This small mismatch is likely caused by the limited storage capacity of laboratory oscilloscope, which allows data acquisition of two fundamental cycles only. Also, note the presence of a small portion of the 20 kHz harmonic components in the spectra. These harmonics arise from the slight asymmetry in the PWM signals produced by enabling signals e_{jn_1} and e_{jn_2}, which results in partial cancelling of the second carrier group harmonics [31].

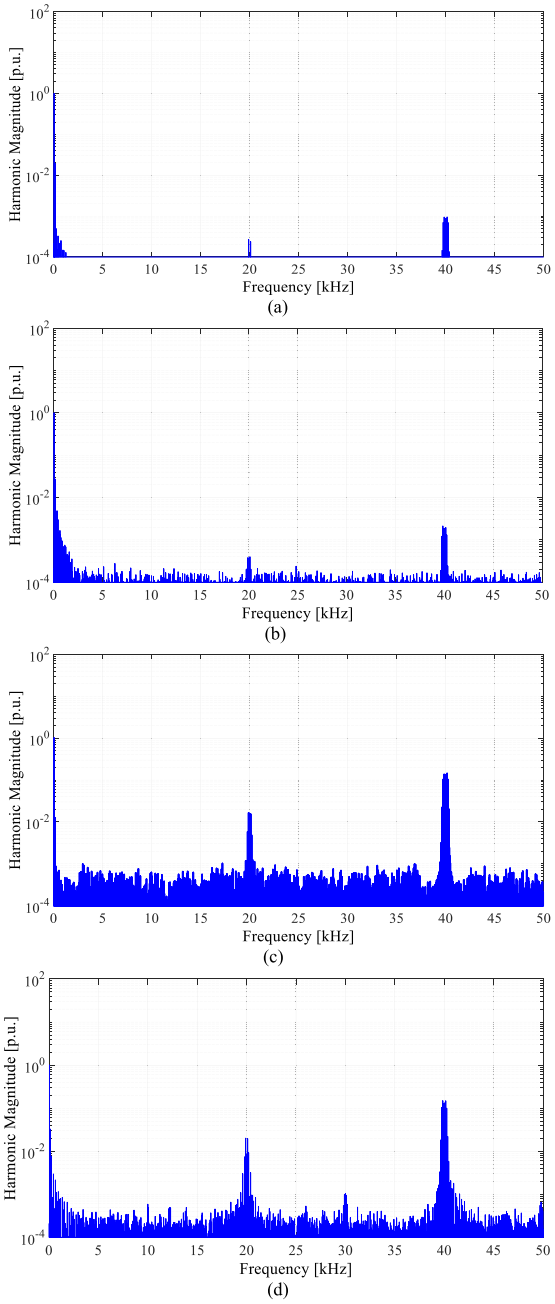

FIGURE 22. Harmonic spectrums of system output variables under IPSDM. (a) Simulated output current, (b) experimental output current, (c) Simulated output voltage, (d) experimental output voltage.

E. EFFICIENCY GAIN OF ADJUSTABLE DISCONTINUOUS MODULATION

Comparative efficiency curves between continuous modulation and proposed adjustable discontinuous modulation are depicted in Fig. 23. From these curves, the adjustable discontinuous modulation substantially improves the system efficiency when compared to the continuous modulation approach. Note the efficiencies for both modulation approaches are relatively low, particularly at lower power conditions, where the transferred power is a small fraction of the rated converter capability. Efficiency measurements

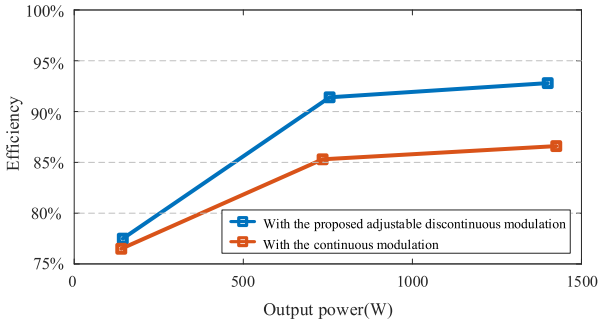

FIGURE 23. Comparative efficiency curve of the MMDBI between adjustable discontinuous modulation and continuous modulation schemes.

at higher operating power conditions, which would further demonstrate the benefit of using the proposed discontinuous modulation approach, cannot be performed at this stage because of limitations of our laboratory facilities. However, the efficiency improvement achieved by the adjustable discontinuous modulation is quite evident from the curves provided in Fig. 23.

VII. CONCLUSION

This paper has proposed a novel modular multilevel converter based on dual buck submodules. Adjustable phase-shifted IPSDM AND NIPSDM discontinuous modulation schemes have been introduced, which are characterized by having only half the switches operating in high-frequency at any given time, leading to reduced device current stresses on semiconductor switch devices and thus improved overall converter efficiency.

Fundamental principles and comprehensive analysis of the converter operating modes and corresponding arm current ripples have been provided. From these, an adjustable current threshold comparison circuit, embedded into the modulation scheme, has been proposed to mitigate the MMDBI arm current zero crossing distortion, for both interleaved phase-shifted discontinuous modulation (IPSDM) and non-interleaved phase-shifted discontinuous modulation (NIPSDM) schemes.

Simulation and experimental results have demonstrated that the adjustable threshold detection strategy proposed in this work, based on the theoretical manipulation of the maximum ripple current, is effective in eliminating the current zero-crossing distortion that is observed when traditional IPSDM and NIPSDM schemes are adopted for modulating the MMDBI topology.

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