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The Research on Additional Errors of Voltage Transformer Connected in Series

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ABSTRACT The series summation method is an important method in the calibration of the voltage coefficient (VC) of the standard voltage transformers (VTs), in which the key step is connecting a fully-insulated VT and a semi-insulated VT in series, and comparing them with the third VT under test. Caused by the imperfect electrical shielding of the serially-wound VTs, additional errors are introduced in the calibration. By analyzing the cause of the additional errors in the serial connection of the VTs, two methods were designed in this paper to measure the additional errors. The proposed methods were harnessed to measure the additional errors for a serial connection of a 35 kV fully-insulated two-stage voltage transformer (TSVT) and a 35 kV semi-insulated TSVT. The results show that the two methods give a consistency of better than 1.0×10^{-6} in ratio error and $2.0 \mu\text{rad}$ in phase displacement, respectively. The accurate measurement of the series additional errors and the correction of them significantly improve the accuracy of the VC measurement of a $110/\sqrt{3}$ kV TSVT based on the series summation method. Furthermore, the VC measurement result is verified by the consistency of the series summation method with the series additional errors corrected and the high-voltage standard capacitor method.

INDEX TERMS Error analysis, high-voltage techniques, series summation method, standard voltage transformer, the serial connection of the transformers, voltage coefficient.

I. INTRODUCTION

Electric energy trade and the loss measurement traceability of electric power transformers, reactors, etc. require a 10^{-6} -level accuracy and the traceability of power frequency high voltage ratio standards. For example, a loss measurement of an accuracy of 1% for the 0.001 power factor means an overall accuracy of 0.001% [1]. The voltage coefficient (VC) of the voltage transformer (VT) refers to the voltage dependence of the transformer error, that is, the variation in ratio error and phase displacement of the transformer with the voltage, which is the most important technical index to ensure the accuracy of transformer ratio. The usual way to measure the VC is by comparing VT with a compressed gas high-voltage standard capacitor (HVSC) and a gas-filled parallel-plates capacitor through a current-comparator-based bridge

(C -tan δ bridge) [2] (called the HVSC method). However, limited by the sensitivity of the C -tan δ bridge, the VC calibration uncertainties of these two-stage voltage transformers (TSVTs) were not as good as they were expected, and were mainly beneath 30% of the rated voltage.

The summation method is another important method for calibrating VTs, which was proposed by scholars from PTB [3]–[6]. This method was proposed for VT ratio traceability, which is the absolute determination of the errors of voltage transformers with parallel-series step-up method or with a summation method via intermediate transformers or capacitive divider. The summation method was improved in 1990s for easier operation [7]. Reference [7] presented a voltage series summation circuit by connecting two single-stage voltage transformers (SSVTs) in series to determine the VC of a third VT, the method is used to calibrate the VC of the transformer (called the series summation method). Instead of the primary in series and the secondary grounding in the

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Zinn’s circuit, the series summation method does not need to accurately adjust the voltage balance between the upper and lower of the boosting transformers, which greatly reduces the difficulty of manufacturing and measurement.

However, limited by the severe nonlinearity and repeatability of the single-stage transformers, the calibration accuracy are not sufficient. Moreover, the changes of the ratio winding potential of the full insulation transformer introduced an unquantifiable error because of its imperfect electrical shielding. Furthermore, in the VC measurement of VT with higher accuracy and higher voltage level, the influence of these two problems is more obvious and cannot be ignored [8], [9].

The key step of the series summation method is to connect the fully-insulated VT and the semi-insulated VT in series, and then compared them with the third VT under test [7]–[9]. Caused by the imperfect electrical shielding of the series-wound VTs, the additional errors are inevitably introduced when the leakage current of the VTs are changed in the calibration. Obviously, in the measurement of VT with higher accuracy and higher voltage level, the influence of the additional errors would be more significant and cannot be ignored. In order to reduce the influence of the additional errors on measurement, a straightforward method is to measure these errors and correct them in the data processing of the series summation method.

In this work, we evaluated the additional errors in the serial connection of the voltage transformers. By analyzing the cause of the additional errors in the serial connection of the VTs, two new measurement methods were proposed and designed to measure the additional errors in the paper. We implemented the proposed methods in the additional errors measurement in the serial connection of a 35 kV fully-insulated two-stage voltage transformer (TSVT) and a 35 kV semi-insulated TSVT. Furthermore, the effectiveness of the two additional errors measurement methods is verified by an indirect comparison: the VC of the $110/\sqrt{3}$ kV two-stage voltage transformers with low-voltage excitation (LVE-TSVT) was measured with the series summation method presented in [7] with a replacement of SSVTs with TSVTs, including the additional errors in the serial connection are ignored or corrected. And then the results were compared with the HVSC method [2].

II. THE ADDITIONAL ERRORS CAUSED BY THE VTS CONNECTED IN SERIES

In the principle of the series summation method [7], the key step is the fully-insulated SSVT and the semi-insulated SSVT connected in series, as shown in Fig. 1(a), where T_1 is a semi-insulated SSVT, and T_{23} is a combined SSVT, which is composed of a fully-insulated VT T_2 , and a high voltage isolation transformer (HVIT) with 1:1 ratio. The function of T_3 is to convert the output voltage of T_2 from the high floating voltage \dot{u}_2 into a low floating voltage \dot{u}_{23} .

However, it should be noticed that the potential of the low terminals X_0 and x_0 of T_{23} in Fig.1 (a) were different from

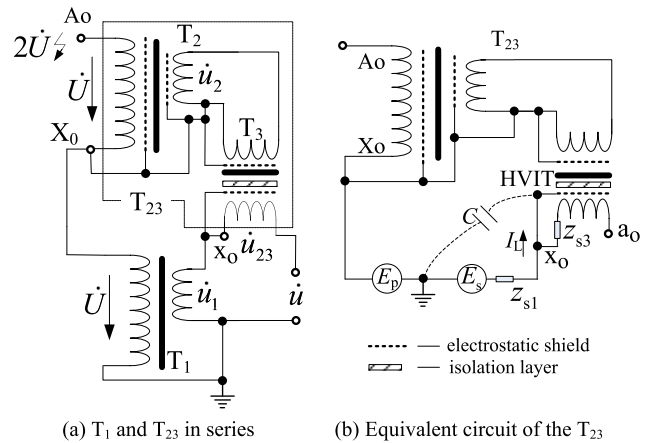


FIGURE 1. The equivalent circuit of T_{23} in serial connection.

those in solely used. Any imperfect electrical shields between the primary and secondary windings may introduce an error shift, and the leakage current changes between grounding and floating situations for the terminals of X_0 and x_0 may also introduce an incalculable error [10].

In order to more concisely analyze the source of additional error in series, the T_{23} was re-drawn in Fig.1(b), where, E_p and E_s are potentials to ground of terminals X_0 and x_0 , respectively. I_L is current entering terminal x_0 . C is the stray capacitance of the electrical shields of T_3 to ground. z_{s1} and z_{s3} are the internal impedance of the secondary winding of the T_1 and T_3 respectively. A change in the operating potentials of the windings will cause a variation in the distribution of capacitance currents within the transformer. This, in turn, may affect the magnetization of the core causing a shift in the transformer error.

Furthermore, the effect of leakage current I_L is not only on T_{23} but also on T_1 . Fig.2 shows the variation of leakage current I_L in the measurement loop of the semi-insulated transformer T_1 in series. TTS is a commercial available transformer test set, $I_{L(T1)}$ is the leakage current from T_1 , and $I_{L(T23)}$ is the leakage current from T_{23} . For the semi-insulated transformer T_1 , leakage currents $I_{L(T23)}$ and $I_{L(T1)}$ both flow through the ratio winding of T_1 , and then a voltage drop is generated across the winding impedance z_{s1} . When the leakage current I_L changes, it will cause the ratio output voltage to change, resulting in the ratio error change. Among them, $I_{L(T23)}$ is greatly affected by E_s , and the $I_{L(T23)}$ not only forms a voltage drop on the winding impedance z_{s3} of the fully-insulated transformer T_{23} but also as the load of T_1 and T_{23} , resulting in load error. The leakage current, $I_{L(T1)} + I_{L(T23)}$, changed about 1 mA in the experiment of T_{23} and T_1 in the serial connection in the Section B of Chapter IV.

The effect of E_p , E_s and I_L on T_{23} and T_1 were the main reasons for the additional errors introduced in the serial connection of the transformer. Furthermore, as the voltage level increases or the VC of the measured voltage transformer is evaluated at 10^{-6} -level, the errors with E_p , E_s and I_L must be considered in the series summation method.

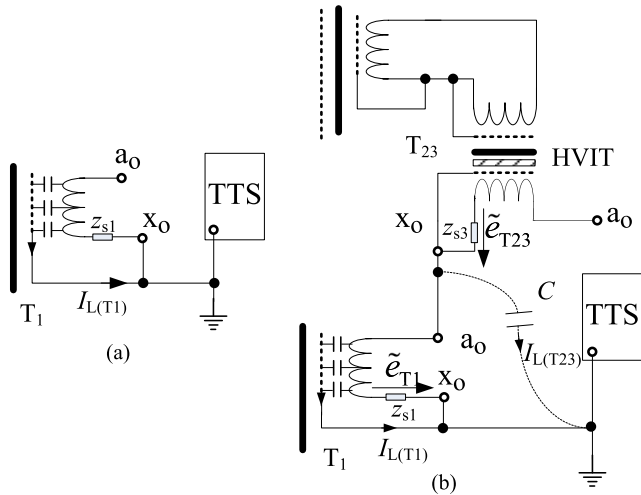


FIGURE 2. The effect of leakage current I_L on T_{23} and T_1 in the serial connection of the voltage transformer, figure (a) shows the T_1 used in normal, and figure (b) shows the variation of leakage current when T_1 used in series. More importantly, the change is directly in the error measurement loop.

Let the errors of T_1 and T_{23} under a voltage \dot{U} be $\dot{\beta}(\dot{U}) = f_2(\dot{U}) + j \cdot \delta_2(\dot{U})$ and $\dot{\gamma}(\dot{U}) = f_3(\dot{U}) + j \cdot \delta_3(\dot{U})$, in which $f_2(\dot{U})$, $f_3(\dot{U})$ and $\delta_2(\dot{U})$, $\delta_3(\dot{U})$ are the ratio errors and phase displacement, respectively.

Assuming that, $\tilde{e}_{T1} = f_{eT1}(\dot{U}) + j \cdot \delta_{eT1}(\dot{U})$, $\tilde{e}_{T23} = f_{eT23}(\dot{U}) + j \cdot \delta_{eT23}(\dot{U})$ represent the additional errors respectively caused by the T_1 and T_{23} connected in series (from its low voltage terminals being grounded to floating by connecting with T_1 in series), where errors may accordingly change for imperfect electrical shields, and leakage current changes etc. Then according to Fig.1 (a), it has

$$\dot{u}_1(\dot{U}) = \frac{\dot{U}}{K} [1 + \dot{\beta}(\dot{U}) + \tilde{e}_{T23}] \quad (1)$$

$$\dot{u}_{23}(\dot{U}) = \frac{\dot{U}}{K} [1 + \dot{\gamma}(\dot{U}) + \tilde{e}_{T1}] \quad (2)$$

$$\begin{aligned} \dot{u}(2\dot{U}) &= \dot{u}_1(\dot{U}) + \dot{u}_{23}(\dot{U}) \\ &= \frac{\dot{U}}{0.5K} \left[1 + \frac{\dot{\beta}(\dot{U}) + \tilde{e}_{T23} + \dot{\gamma}(\dot{U}) + \tilde{e}_{T1}}{2} \right] \end{aligned} \quad (3)$$

Therefore, the additional errors respectively caused by the T_1 and T_{23} connected in series (the \tilde{e}_{T1} and \tilde{e}_{T23}) cannot be ignored when the VC of the measured voltage transformer is evaluated at 10^{-6} -level, especially for high voltage. However, the \tilde{e}_{T1} and \tilde{e}_{T23} could be measured and corrected.

III. THE MEASUREMENT METHOD OF THE ADDITIONAL ERRORS OF \tilde{e}_{T1} AND \tilde{e}_{T23}

To demonstrate the presence and the influence of \tilde{e}_{T1} and \tilde{e}_{T23} , two additional error measurement methods were designed. One is to carry out measurements directly by the transformer test set (TTS), that is, the errors are directly read from the TTS (called direct measurement method). The other is based on the third standard VT. The SSVTs,

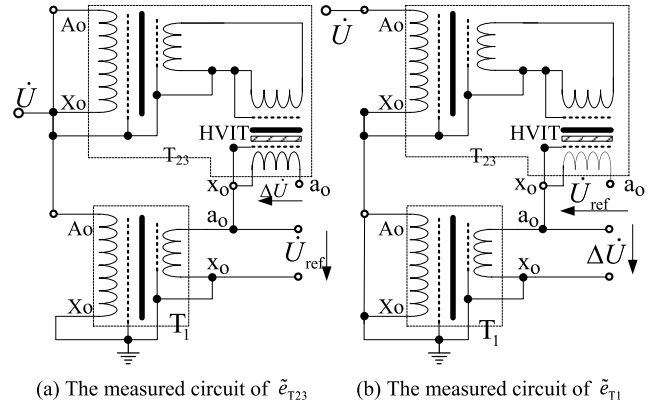


FIGURE 3. directly measured circuits of \tilde{e}_{T23} and \tilde{e}_{T1} with the TTS. Both in figure (a) and (b), keep the primary and the secondary windings of T_1 and T_{23} connected in series respectively. Through controlling the primary winding of T_{23} and T_1 , the corresponding T_1 and T_{23} are in series, respectively. For example, in figure (a), when the high and the low ends of primary windings of T_{23} were connected to the high voltage \dot{U} , the existence of $I_{L(T23)}$ may form a voltage drop on the leakage impedance of the fully-insulated transformer T_{23} and result the load error at the same time, that is, the effect of E_p , E_s and I_L on T_{23} .

in series or solely used, are compared with the third standard VT, and the errors introduced in serial connection are calculated (called comparative measurement method).

The direct measurement circuit was designed as shown in Fig.3. In Fig.3 (a), T_1 and T_{23} are connected in series and a voltage of \dot{U} and 0 V were applied respectively, that is, the high and the low ends of primary windings of T_{23} were connected to the high-voltage \dot{U} . Then, TTS measures the $\Delta\dot{U}$ or \tilde{e}_{T23} , of the secondary voltage of T_{23} against to the \dot{U}_{ref} of the secondary voltage of T_1 . The \tilde{e}_{T1} could be determined in the similar method as \tilde{e}_{T23} , as shown in Fig.3 (b).

The second measurement method of the additional errors \tilde{e}_{T1} and \tilde{e}_{T23} is comparative measurement. Taking the measurement of \tilde{e}_{T23} as an example, the comparative measurement circuits were designed as shown in Fig.4, and the comparative measurement circuit of \tilde{e}_{T1} is the same with the \tilde{e}_{T23} and is omitted. In Fig.4, the semi-insulated SSVT T_1 is compared with the third standard voltage transformer T_0 in series and solely used respectively. And then calculated the errors introduced in serial connection, that is, the change of the error of the measured SSVT T_1 between two comparison experiments.

Take the additional errors measurement in the serial connection of a 35 kV fully-insulated TSVT and a 35 kV semi-insulated TSVT as an example, in the experiment, the two measured methods on the additional errors of \tilde{e}_{T1} and \tilde{e}_{T23} gave a well agreement of ratio error and phase displacement, respectively (detailed in Table 1 of Chapter IV).

IV. THE MEASUREMENT AND VERIFICATION OF THE ADDITIONAL ERRORS OF \tilde{e}_{T1} AND \tilde{e}_{T23}

In the process of the series summation method based on SSVTs, the nonlinearity and repeatability of the SSVTs also contribute some uncertainties. To achieve better uncertainty, the LVE-TSVTs were used instead of SSVTs. In order to

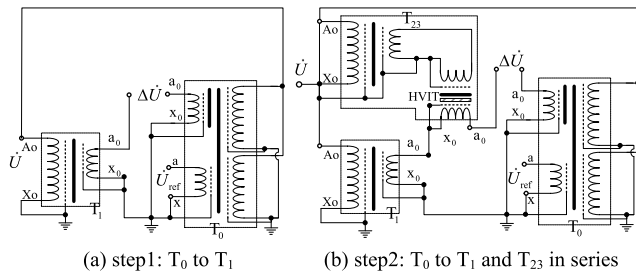


FIGURE 4. Comparative measurement of the $\tilde{e}_{T_{23}}$ with the third standard VT T_0 .

TABLE 1. The data of \tilde{e}_{T_1} and $\tilde{e}_{T_{23}}$ in the serial connection of a new 35 kV fully-insulated LVE-TSVT and a 35 kV semi-insulated LVE-TSVT.

Percentage of \dot{U}_n /%	15	30	60	Method of measurement	
Applied voltage /kV	9.5	19.1	38.1		
$\tilde{e}_{T_{23}}$	$f / 10^{-6}$	13.5	13.6	13.7	Direct measurement (Fig.3)
	$\delta / \mu\text{rad}$	-8.8	-8.6	-8.5	
	$f / 10^{-6}$	13.9	13.4	13.2	
$\delta / \mu\text{rad}$	-8.5	-10.2	-9.9		
\tilde{e}_{T_1}	$f / 10^{-6}$	0.9	0.8	1.0	Direct measurement (Fig.3)
	$\delta / \mu\text{rad}$	-1.8	-1.8	-1.7	
	$f / 10^{-6}$	1.1	1.0	0.9	
$\delta / \mu\text{rad}$	-1.4	-1.6	-1.7		

Compared the data of the two measurement methods at corresponding voltages, the maximal difference of ratio error was 0.5×10^{-6} at the 60% of the rated voltage for the $\tilde{e}_{T_{23}}$, and the maximal difference of phase displacement was $1.6 \mu\text{rad}$ at the 30% of the rated voltage for the $\tilde{e}_{T_{23}}$.

measure the VC of the $110/\sqrt{3}$ kV LVE-TSVT T_0 , a new 35 kV fully-insulated LVE-TSVT T_{23} was developed for the series summation method, by connecting in series with the 35 kV semi-insulated LVE-TSVT T_1 . It should be declared that this paper, in sections IV.A, reuses some content from thesis [11] with permission.

A. THE 35 kV FULLY-INSULATED LVE-TSVT

Similar to the semi-insulated LVE-TSVT in [12], the structure of the HVIT T_3 and the fully-insulated LVE-TSVT T_2 are both made of two overlapped toroidal cores, S1 and S2. A low-voltage excitation TSVT $T_{20}(T_{30})$ and an auxiliary transformer $T_{2C}(T_{3C})$ are also involved.

Fig. 5(a) presents the structure of the HVIT (T_3) with 1:1 ratio, including the layout of the cores, the windings, as well as the shields. The difference between the HVIT and the semi-insulated LVE-TSVT in [12] was that an insulation layer I_{S1} (I_{SP}) and an electrostatic shield E.S.0 were added

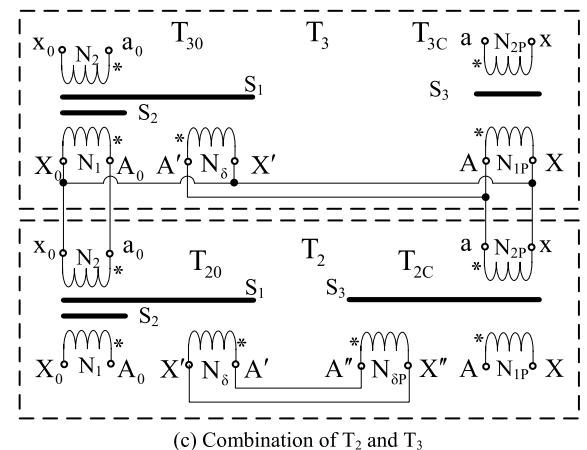
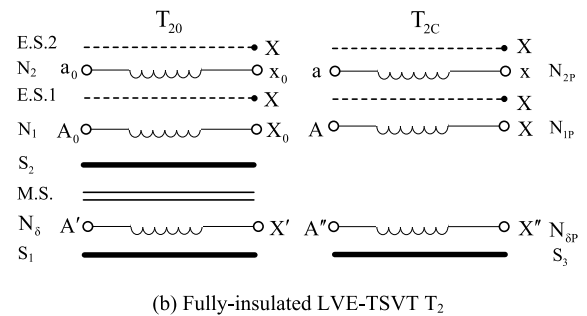
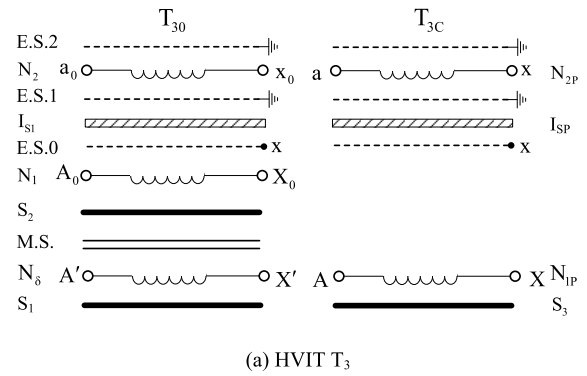


FIGURE 5. Structure of a fully-insulated LVE-TSVT.

between the primary ratio winding N_1 (N_{1P}) and the secondary ratio windings N_2 (N_{2P}) of the transformer T_{30} (T_{3C}) in T_3 . E.S.0 was electric connected with the terminal X_0 (X) of N_1 .

Fig. 5 (b) shows the structure of the fully-insulated LVE-TSVT T_2 . The difference between T_2 and the semi-insulated LVE-TSVT in [3] is that the electrostatic shields E.S.1 and E.S.2 of T_2 are generally connected to the terminal X_0 (X) of N_1 (N_{1P}) and x_0 (x) of N_2 (N_{2P}) respectively, rather than directly grounded.

Fig. 5 (c) presents the circuits of T_{23} , the combination of T_2 and T_3 , with electrostatic shields and insulation layers omitted for convenience. The upper dashed box presents the HVIT T_3 , and the lower dashed box presents the fully-insulated LVE-TSVT T_2 . The terminals (A_0 , A) and (X_0 , X) of T_{20} and T_{2C} in T_2 were led out within two bushings for high voltage connection.

B. THE ERROR MEASUREMENTS OF \tilde{e}_{T1} AND \tilde{e}_{T23} IN THE SERIAL CONNECTION OF A NEW 35 kV FULLY-INSULATED LVE-TSVT AND A 35 kV SEMI-INSULATED LVE-TSVT

Measuring the additional errors of \tilde{e}_{T23} and \tilde{e}_{T1} caused by the new 35 kV fully-insulated LVE-TSVT and the 35 kV semi-insulated LVE-TSVT connected in series, schematic diagram of measuring circuits as shown in Fig.3 and Fig.4, where SSVTs are replaced with LVE-TSVTs in the measurement. Table 1 lists the \tilde{e}_{T23} and \tilde{e}_{T1} in condition of corresponding voltages. In Fig.4, the standard VT is a $110/\sqrt{3}$ kV semi-insulated LVE-TSVT (T_0) [13]. A 8-dial two-stage inductive voltage divider (IVD) was cascaded with the series secondary windings of T_1 and T_{23} in order to match the ratios between the $110/\sqrt{3}$ kV LVE-TSVT and the series of 35 kV LVE-TSVTs, and the IVD is omitted in Fig.4.

From Table 1, the two measurements on the errors of \tilde{e}_{T1} and \tilde{e}_{T23} give a consistency of better than 1.0×10^{-6} in ratio error and $2.0 \mu\text{rad}$ in phase displacement, respectively.

C. THE APPLICATION OF THE ADDITIONAL ERRORS

The 35 kV fully-insulated LVE-TSVT (T_{23}) and the 35 kV semi-insulated LVE-TSVT (T_1) were connected in series to calibrate the VC of the $110/\sqrt{3}$ kV semi-insulated LVE-TSVT (T_0) based on the series summation method [7]. A 8-dial two-stage IVD was cascaded with the series secondary windings of T_1 and T_{23} in order to match the ratios between the $110/\sqrt{3}$ kV LVE-TSVT and the series of 35 kV LVE-TSVTs. The photo of experimental site is shown in Fig. 6.

Let the errors of T_0 under a voltage \dot{U} as $\dot{\alpha}(\dot{U}) = f_1(\dot{U}) + j \cdot \delta_1(\dot{U})$, in which $f_1(\dot{U})$ and $\delta_1(\dot{U})$ are the ratio errors and phase displacement, respectively. Based on the three steps of the series summation method mentioned in [7], and considering the error introduced in series, the VC of the measured $110/\sqrt{3}$ kV LVE-TSVT (T_0) can be expressed as equation (4) and (5).

$$\begin{aligned} \Delta\dot{\alpha}_{\dot{U} \sim 2\dot{U}} &= \dot{\alpha}(2\dot{U}) - \dot{\alpha}(\dot{U}) \\ &= \tilde{\varepsilon}_1(2\dot{U}) - \left(\frac{\tilde{\varepsilon}_2(\dot{U}) + \tilde{\varepsilon}_3(\dot{U})}{2} - \frac{\tilde{e}_{T1} + \tilde{e}_{T23}}{2} \right) \end{aligned} \quad (4)$$

$$\begin{cases} f_1(2\dot{U}) - f_1(\dot{U}) \\ = f_{\varepsilon 1}(2\dot{U}) - \frac{f_{\varepsilon 2}(\dot{U}) + f_{\varepsilon 3}(\dot{U})}{2} + \frac{f_{\varepsilon T1}(\dot{U}) + f_{\varepsilon T23}(\dot{U})}{2} \\ \delta_1(2\dot{U}) - \delta_1(\dot{U}) \\ = \delta_{\varepsilon 1}(2\dot{U}) - \frac{\delta_{\varepsilon 2}(\dot{U}) + \delta_{\varepsilon 3}(\dot{U})}{2} + \frac{\delta_{\varepsilon T1}(\dot{U}) + \delta_{\varepsilon T23}(\dot{U})}{2} \end{cases} \quad (5)$$

where, $\tilde{\varepsilon}_1(2\dot{U})$ is the error of T_0 at the voltage of $2\dot{U}$ by taking T_1 and T_{23} in series as the reference. $\tilde{\varepsilon}_2(\dot{U})$ and $\tilde{\varepsilon}_3(\dot{U})$ are the errors of T_0 at the voltage of \dot{U} by taking T_1 and T_{23} as the reference respectively. Let the errors obtained from the three comparative measurement experiments as $\tilde{\varepsilon}_1(2\dot{U}) = f_{\varepsilon 1}(2\dot{U}) + j \cdot \delta_{\varepsilon 1}(2\dot{U})$, $\tilde{\varepsilon}_2(\dot{U}) = f_{\varepsilon 2}(\dot{U}) + j \cdot \delta_{\varepsilon 2}(\dot{U})$,

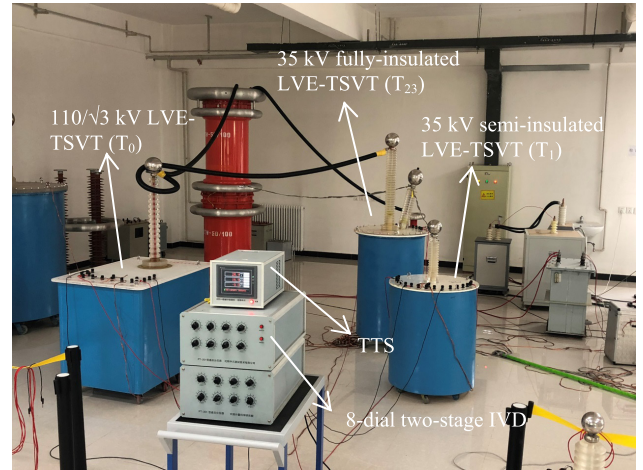


FIGURE 6. Photos of $110/\sqrt{3}$ kV LVE-TSVT measurement with the series summation method, and replace the SSVTs with LVE-TSVTs. The series summation method contents three comparison experiments. Step 1: T_1 and T_{23} were connected in series, and then were compared with T_0 at the voltage of $2\dot{U}$. Step 2 and Step 3: T_1 and T_{23} were compared with T_0 one by one at voltage of \dot{U} .

TABLE 2. Three steps of the series summation method and the additional error in series.

Applied voltage /kV	19.1	38.1	76.2	
Percentage of \dot{U}_n /%	30	60	120	
$\tilde{\varepsilon}_1(2\dot{U})$	$f_{\varepsilon 1}/10^{-6}$	16.7	16.4	15.6
	$\delta_{\varepsilon 1}/\mu\text{rad}$	-9.6	-9.9	-10.2
Percentage of \dot{U}_n /%	15	30	60	
$\tilde{\varepsilon}_2(\dot{U})$	$f_{\varepsilon 2}/10^{-6}$	16.5	15.8	15.7
	$\delta_{\varepsilon 2}/\mu\text{rad}$	-8.3	-7.7	-8.4
$\tilde{\varepsilon}_3(\dot{U})$	$f_{\varepsilon 3}/10^{-6}$	3.9	3.8	3.5
	$\delta_{\varepsilon 3}/\mu\text{rad}$	-2.6	-2.0	-2.0
Percentage of \dot{U}_n /%	15	30	60	
\tilde{e}_{T23}	$f/10^{-6}$	13.5	13.6	13.7
	$\delta/\mu\text{rad}$	-8.8	-8.6	-8.5
\tilde{e}_{T1}	$f/10^{-6}$	0.9	0.8	1.0
	$\delta/\mu\text{rad}$	-1.8	-1.8	-1.7

In the Table II, the \tilde{e}_{T23} and \tilde{e}_{T1} are measured with direct measurement method, that is, the data of row 3, 4, and row 7, 8 of Table I.

$\tilde{\varepsilon}_3(\dot{U}) = f_{\varepsilon 3}(\dot{U}) + j \cdot \delta_{\varepsilon 3}(\dot{U})$, where $f_{\varepsilon 1}(2\dot{U})$, $f_{\varepsilon 2}(\dot{U})$, $f_{\varepsilon 3}(\dot{U})$, and $\delta_{\varepsilon 1}(2\dot{U})$, $\delta_{\varepsilon 2}(\dot{U})$, $\delta_{\varepsilon 3}(\dot{U})$ are the TTS readings in ratio errors and phase displacement, respectively.

Table 2 lists the measured data in condition of corresponding voltages of the three comparative measurement experiments.

$\Delta\dot{\alpha}_{\dot{U} \sim 2\dot{U}}$ is calculated according to equation (4) and (5) with the $\tilde{\varepsilon}_1(2\dot{U})$, $\tilde{\varepsilon}_2(\dot{U})$ and $\tilde{\varepsilon}_3(\dot{U})$ got in the three comparative measurement experiments. The data is listed in Table 3.

TABLE 3. Ratio errors and phase displacement got by the series summation method.

Percentage of \dot{U}_n /%	$2^{N-1} \% \dot{U}_n$ $\sim 2^N \% \dot{U}_n$	15	30	60	Error Processing
$\Delta\dot{\alpha}_{2^{N-1}\dot{U}_n \sim 2^N \dot{U}_n}$	$f / 10^{-6}$	6.5	6.6	6.0	\tilde{e}_{T1} and \tilde{e}_{T23} is ignored
	$\delta / \mu\text{rad}$	-4.2	-5.1	-5.0	
$\Delta\dot{\alpha}_{2^{N-1}\dot{U}_n \sim 2^N \dot{U}_n}$	$f / 10^{-6}$	-0.7	-0.6	-1.4	\tilde{e}_{T1} and \tilde{e}_{T23} is corrected
	$\delta / \mu\text{rad}$	1.2	0.1	0.1	

TABLE 4. The VC of T_0 with the series summation method.

Percentage of \dot{U}_n /%	15	30	60	120	Error Processing	
Applied voltage /kV	9.5	19.1	38.1	76.2	\tilde{e}_{T1} and \tilde{e}_{T23} is ignored	
$\Delta\dot{\alpha}_{15\% \dot{U}_n \sim \dot{U}_n}$	$f / 10^{-6}$	0.0	6.5	13.1		19.1
	$\delta / \mu\text{rad}$	0.0	-4.2	-9.3	-14.3	
$\Delta\dot{\alpha}_{15\% \dot{U}_n \sim \dot{U}_n}$	$f / 10^{-6}$	0.0	-0.7	-1.3	-2.7	\tilde{e}_{T1} and \tilde{e}_{T23} is corrected
	$\delta / \mu\text{rad}$	0.0	1.2	1.3	1.4	

In the series summation method, the variation in ratio error and phase displacement of the measured transformer from voltage \dot{U} to $2\dot{U}$ can be calculated through three comparison experiments. So the test points of 15%, 30%, 60% and 120% instead of regular test points such as rated voltage of 80% and 100%. And it also can choose test points such as rated voltage of 20%, 40% and 80%.

Summing all the $\Delta\dot{\alpha}$ to get the total error with equation (6).

$$\begin{aligned} \Delta\dot{\alpha}_{(15\% \sim 120\%) \dot{U}_n} &= \Delta\dot{\alpha}_{(15\% \sim 30\%) \dot{U}_n} + \Delta\dot{\alpha}_{(30\% \sim 60\%) \dot{U}_n} + \Delta\dot{\alpha}_{(60\% \sim 120\%) \dot{U}_n} \end{aligned} \quad (6)$$

The table 4 lists the VC of the $110/\sqrt{3}$ kV LVE-TS VT obtained when the additional errors are corrected according to Table 2 or ignored. In order to further verify the additional errors measurement method, we measured the VC of the $110/\sqrt{3}$ kV LVE-TS VT in the next section by another commonly methods.

V. DISCUSSION AND VERIFICATION

A few attentions are given for the above measurements.

A. TTS AND SECONDARY LOOP GROUNDING

In the error measured circuits, $\Delta\dot{U}/\dot{U}_{ref}$ was measured by a commercial available TTS. Basically, it was a specially designed Phase-Lock-Amplifier (PLA) with higher input voltage up to 120 V in its reference channel, and high floating and differential input voltage for $\Delta\dot{U}$. In order to prevent any leakage current load or introduce any error voltage in the secondary voltage loop, all the low terminals x_0 of the semi-SSVTs should be connected to a single grounding point on the PLA-based TTS.

B. THE DISCUSS ON ADDITIONAL ERRORS MEASUREMENT WITH THE DIRECT MEASUREMENT METHOD

As analyzed in Section II, the effect of leakage current I_L is not only on T_{23} but also on T_1 , that is, as the load of T_1 , T_{23} and resulting in load error. Based on third standard VT T_0 , the load errors of T_1 when used in serial connection with T_{23} can be measured, as shown in Figure 7. The T_1 , in series or solely used, is compared with the standard VT T_0 , and the load errors introduced in serial connection are calculated.

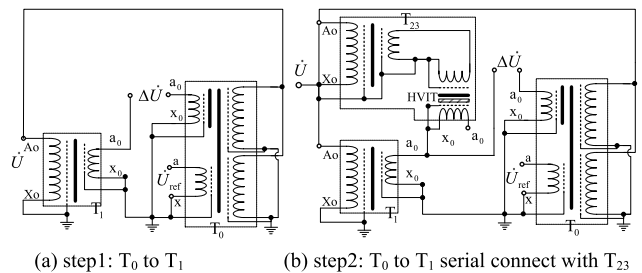


FIGURE 7. Comparative measurement of the load errors of T_1 with a standard VT T_0 , the difference from Figure 4 is that the output of T_1 when used in series is measured here (a_0 of T_1), instead of the output of T_1 serial connection with T_{23} (a_0 of T_{23}) in Figure 4. The T_1 and T_{23} are represented with single stage for convenience.

The load errors of the 35 kV semi-insulated TS VT when used in serial connection with the 35 kV fully-insulated TS VT were measured. And the comparison of experimental data indicated that the load errors of the 35 kV semi-insulated TS VT is less than 0.5×10^{-6} in ratio error and $0.6 \mu\text{rad}$ in phase displacement respectively. It is due to the better load-carrying capacity of the TS VT of this semi-insulated structure. Therefore, when the additional errors are measured with the direct measurement method, the load errors of T_1 can be ignored.

There is the same load effect on T_{23} from T_1 . However, the x_0 of T_{23} is nearly the ground potential, as shown in Fig.3 (a). So the load errors of T_{23} can be ignored too.

C. THE VERIFICATION BY MEASURING THE VC OF THE $110/\sqrt{3}$ kV LVE-TS VT WITH HVSC METHOD

Another commonly method for measuring the VC of the $110/\sqrt{3}$ kV LVE-TS VT is by comparing it with a gas-compressed HVSC through an AC current comparator from 30% to 120% of the rated voltage [2]. The principle diagram of calibration system between standard capacitor and LVE-TS VT is shown in Fig.8, which mentioned in [2].

The C -tan δ bridge was a modified commercial available one based on AC current comparator principle. In the bridge, seven dials for capacitive ratio and dissipation were designed, and an external phase-lock-amplifier was attached as a null indicator to obtain a 1×10^{-7} adjustment. The current dependence of the fixed ratio of this C -tan δ bridge was checked better than 3×10^{-7} by comparing two capacitors with negligible voltage coefficient [13].

[10] N. L. Kusters, W. J. M. Moore, and O. Petersons, "The effect of winding potentials on voltage transformer errors," *IEEE Trans. Power Appar. Syst.*, vol. 83, no. 2, pp. 115–121, Feb. 1964.

[11] H. Shao, F. Lin, B. Liang, H. Zhang, W. Zhao, J. Wang, and C. Li, "Voltage dependence measurement of a 110 kV LVE-TSVT," in *Proc. Conf. Precis. Electromagn. Meas. (CPEM)*, Jul. 2016, pp. 1–2.

[12] S. X. Peng, Y. H. Song, and Y. X. Ma, "R&D on two-stage potential transformers of 35 kV with accuracy class of 0.001 and (110/v 3) kV with accuracy class of 0.002," *Elect. Equip.*, vol. 6, no. 7, pp. 10–16, Jul. 2005.

[13] H. M. Shao, F. P. Lin, B. Liang, W. Zhao, D. X. Dai, S. X. Peng, T. Y. Sun, J. Y. Liu, and H. H. Zhang, "The development of 110/√3kV two-stage voltage transformer with accuracy class 0.001," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 6, pp. 1383–1389, Jun. 2015.

[14] N. L. Kusters and O. Petersons, "The voltage coefficients of precision capacitors," *Trans. Amer. Inst. Elect. Eng., I, Commun. Electron.*, vol. 82, no. 5, pp. 612–621, Nov. 1963.

[15] H. H. Zhang, Z. H. Zhang, H. M. Shao, and W. Zhao, "Voltage coefficients measurement method of the high voltage compressed-gas capacitor," *Chin. J. Sci. Instrum.*, vol. 36, no. 3, pp. 530–536, Mar. 2015.

[16] H. Shao, W. Li, D. Dai, B. Liang, and F. Lin, "The development of 5 nF parallel-plate capacitors with low voltage coefficient," in *Proc. 29th Conf. Precis. Electromagn. Meas. (CPEM)*, Aug. 2014, pp. 286–287.



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