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A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 μm CMOS

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ABSTRACT A new solution for an ultra-low-voltage, ultra-low-power operational transconductance amplifier (OTA) is presented in the paper. The design exploits a three-stage structure with a Reversed Miller Compensation Scheme, where the input stage is based on a non-tailed bulk-driven differential pair. Optimization of the structure for very low supply voltage is discussed. The resulting amplifier outperforms other ultra-low-voltage OTAs in terms of a DC voltage gain and power efficiency, expressed by standard figures of merit. Experimental verification using a 0.18 μm CMOS technology, with supply voltage of 0.3-V, showed a dissipation power of 13 nW, a DC voltage gain of 98 dB, a gain-bandwidth product of 3.1 kHz and an average slew-rate of 9.1 V/ms at 30 pF load capacitance. The experimental results agree well with simulations.

INDEX TERMS Bulk-driven, operational transconductance amplifier, operational amplifier, low voltage, low power.

I. INTRODUCTION

The increasing demand for ultra-low-power electronic systems, entails an increasing interest in the design of analog and mixed signal circuits, powered with very low supply voltages, often much lower than 0.5 V. These new designs include operational amplifiers [1]–[8], linear transconductors [9], [10], differential-difference amplifiers [11] hysteretic comparators [12], and many other building blocks. In order to ensure sufficient voltage swing at such extreme supply conditions, a bulk-driven (BD) technique [13], [14] is often considered. Even though the BD transistors suffer from a reduced transconductance, that entails larger input noise and offset, this technique seems to be still attractive in such cases when the supply voltage (V_{DD}) is comparable with the threshold voltage (V_{TH}) of the used MOS transistors and a large input common-mode range (ICMR) is required at the same time.

One of the most important analog building blocks in integrated systems is the operational transconductance amplifier (OTA). In recent years a number of deep sub 0.5-V OTAs have been shown in the literature [2], [4], [6]–[8]. It is worth mentioning, that the presented OTAs usually show moderate value of the DC open-loop voltage gain. In most cases it is associated with the use of low-V_{TH} CMOS processes, that entails reduced intrinsic voltage gains of MOS transistors, as well as smaller g_{mb}/g_m ratios [2]. In order to overcome this issue, specific layout design techniques combined with a partial positive feedback [2], three-stage structures [4], [8] or other gain-boosting techniques can be used [6]. Nevertheless, despite special design approaches, the achieved voltage gains in most cases are rather moderate, ranging from 43 dB [4] to 70 dB [8]. Only in some cases a slightly larger voltage gain, exceeding 70 dB, can be achieved, using partial positive feedback or auxiliary current-mode amplifiers [6], but at the cost of a reduced gain-bandwidth product (GBW) and slew-rate (SR).

In this work a new solution for a high-gain (ca. 100 dB) deep sub 0.5-V OTA is presented. The design is based on a three-stage structure, where the input differential pair is realized using the idea of non-tailed differential stage [15], that can operate from very low relative supply voltages (V_{DD}/V_{TH}), while offering improved DC voltage gain and SR. Consequently, an ultra-low-voltage (ULV) three-stage amplifier was designed using standard 0.18 μm CMOS process with relatively large intrinsic voltage gains of MOS transistors. The achieved voltage gain of the considered structure approaches 100 dB, while operating from V_{DD} as low as 0.3 V. Moreover, the achieved GBW and SR to supply current ratios are competitive to the ones achieved for other OTAs presented in literature with similar V_{DD}. The three-stage amplifier was frequency compensated using similar approach as presented in [16] for a 1-V gate-driven amplifier.

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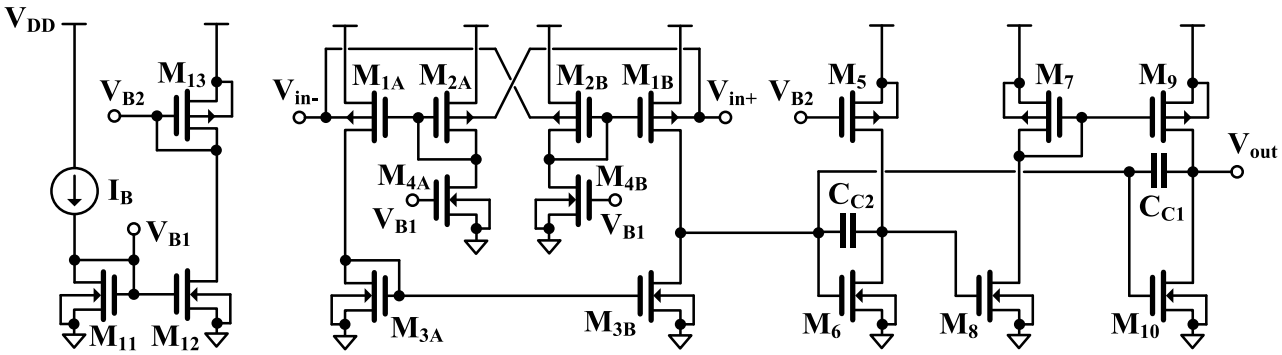


FIGURE 1. CMOS schematic of the proposed three-stage OTA.

Nevertheless, the ULV design requires larger transistor sizes, that leads to larger parasitic capacitances affecting the circuit performance. Hence, the design constraints associated with an ULV environment as well as the optimization of such a structure under sub-V_{TH} supply are discussed in the paper.

The proposed circuit can serve as a general-purpose OTA in ULV amplifiers, active filters, analog to digital converters and other applications requiring high-gain OTAs.

The rest of the article is organized as follows. In section II a general description of the OTA is presented. In section III, the design constraints in an ULV environment are discussed. Experimental and simulation results are shown in section IV. Finally, the paper is concluded in section V.

II. CIRCUIT DESCRIPTION

The structure of the presented OTA is shown in Fig.1. The circuit consists of three stages. Its simplified block diagram is depicted in Fig. 2, where g_{mi}, R_{oi} and C_{oi} are the i-th stage transconductance, resistance and equivalent output capacitance respectively, while g_{mFF} stands for the transconductance of the feedforward path implemented by M_{10}. The overall structure can be considered as a Reversed Nested Miller Compensation (RNMC) topology [17]–[19]. The RNMC structures are often implemented with the use of a special nulling resistor, however, in this design the nulling resistor was removed, since its value would be un-practically large, in the range of tens of mega ohms. The resistorless version of a 3-stage RNMC OTA, devoted to driving large capacitive loads was previously discussed in [16].

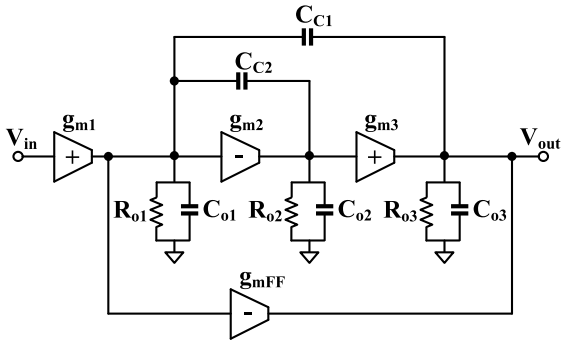


FIGURE 2. Block diagram of OTA.

The first stage of the presented structure (M_1-M_4) is based on a non-tailed bulk-driven differential amplifier [15]. Despite the non-tailed architecture, the circuit behaves as a truly differential amplifier, with good common-mode rejection (CMRR) and power supply rejection (PSRR) ratios. Compared to the BD differential pair biased with the same total current and the same sum of transistor channel areas, the circuit offers improved voltage gain (+ 6 dB), slew-rate and lower minimum V_{DD}, while showing the same input referred noise and offset [7], [15]. The use of such a circuit allows realizing amplifiers with very low V_{DD} ($\ll$0.5 V) and rail-to-rail ICMR, while using CMOS processes with standard V_{TH} voltages of around 0.4-0.5V, low leakage currents and relatively high intrinsic voltage gains of MOS transistors. All these features allow increasing the overall voltage gain of an ULV OTA.

The second stage of the amplifier is formed by the transistor M_6, loaded with the current source based on the transistor M_5. The output stage (M_7-M_{10}) [16], [20] operates in class AB, that increases its current driving capability and SR. The capacitances C_{C1} and C_{C2} are used for frequency compensation. Transistors M_{11}-M_{13} form the biasing circuit.

A. SMALL-SIGNAL PERFORMANCE

The small-signal analysis of the structure in Fig.2. has been performed in [16]. For simplicity it was assumed that $C_{C1,2}$, $C_L \gg C_{oi}$ and $g_{mi}R_{oi} \gg 1$, i=1...3 (C_L being the load capacitance of OTA). With the above assumptions the circuit is described by a third order transfer function with two zeros, one located in the left half-plane (LHP) and the other one in the right half-plane (RHP) [16]. The DC voltage gain of the circuit can be approximated as:

$$A_{vo} \approx -g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3} \tag{1}$$

while the dominant pole p_1 and the gain-bandwidth product (ω_{GBW}) are respectively given by:

$$p_1 \approx -\frac{1}{R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}C_{C1}} \tag{2}$$

$$\omega_{GBW} = \frac{g_{m1}}{C_{C1}} \tag{3}$$

As it was shown in [16], assuming $g_{mFF} = g_{m3}$, $C_{C2} < g_{m2}g_{m3}C_{C1}/g_{m1}^2$ and $C_L \gg C_{C1}$, the phase margin Φ can be approximated as:

$$\tan\phi = \frac{g_{m2}g_{m3}C_{C1}^2 - g_{m1}^2 C_{C2}C_L}{g_{m1}g_{m2}C_{C1}C_L} \tag{4}$$

From (4), the compensation capacitor C_{C1} can be calculated using the following formula [16]:

$$C_{C1} = \sqrt{\frac{g_{m1}C_{C2}C_L}{g_{m3}}\left(\frac{g_{m1}}{g_{m2}} + \tan\phi\right)} \tag{5}$$

Assuming operation in a weak inversion region and neglecting the second-order effects, the transconductance g_{m1} in Fig. 2 can be expressed as:

$$g_{m1} \cong 2g_{mb1} = 2\eta\frac{I_{D1}}{n_p V_T} \tag{6}$$

where $\eta = g_{mb}/g_m$ is the bulk to gate transconductance ratio at a given operating point for transistors $M_{1A,B}$, I_{D1} is the quiescent drain current of these transistors, n_p is the subthreshold slope factor for a p-channel MOS and V_T is the thermal potential.

The transconductances g_{m2} and g_{m3} in Fig. 2 are given by:

$$g_{m2} = \frac{I_{D5,6}}{n_n V_T} \tag{7}$$

$$g_{m3} = \frac{I_{D8}}{n_n V_T}\cdot\frac{(W/L)_9}{(W/L)_7} = \frac{I_{D10}}{n_n V_T} \tag{8}$$

Note, that the feedforward transconductance g_{mFF} is equal to g_{m3}.

B. IMPACT OF STRAY CAPACITANCES

Ultra-low-voltage (sub V_{TH}) design entails large transistor sizes to maintain both, low $|V_{GS}|$ voltage drops at the operating point, as well as sufficiently high output resistances of transistors at reduced V_{DS} voltages. The large transistor sizes entail larger parasitic capacitances C_{oi}. Therefore, using the formulas developed in ideal case could lead to large errors. The most critical is the impact of the parasitic capacitance C_{o2}, since outputs of the first and the third stages are shunted with large capacitances C_{C1}, C_{C2} and C_L (in addition, in case of the first stage the capacitances C_{C1} and C_{C2} are multiplied by the Miller effect). Non-ideal analysis with a non-zero value of C_{o2} give the same formulas for tan Φ and C_{C1} as developed for ideal case, however, in (4) and (5) the capacitance C_{C2} should be replaced with $C'_{C2} = C_{C2} + C_{o2}$. Note, that C_{o2} limits the minimum value of C'_{C2}, which next limits the minimum value of C_{C1} and consequently lowers the GBW product of OTA.

C. SLEW-RATE PERFORMANCE

Slew-rate in multi-stage amplifiers is limited by the slowest stage. For the considered structure its value can be expressed by:

$$SR = min\left(\frac{I_{o1max}}{C_{o1}+C_{C1}+C_{C2}}; \frac{I_{02max}}{C_{o2}+C_{C1}}; \frac{I_{03max}}{C_{o3}+C_L}\right) \tag{9}$$

where I_{oimax} (i=1...3) is the maximum output current of the i-th stage of the OTA. Assuming that the SR is not constrained by the $|V_{GS}|$ voltage drops across the diode-connected transistors, in the considered design the negative slew-rate (SR-) is limited rather by the first stage and can be estimated as:

$$SR_- \approx \frac{I_{o1max}}{C_{o1}+C_{C1}+C_{C2}} \tag{10}$$

where I_{o1max} is given by:

$$2I_{D1}\sinh\left(\frac{\eta V_{inm}}{n_p U_T}\right) \tag{11}$$

where V_{inm} is the amplitude of the input step and its maximum value is equal to V_{DD}. It is worth noting, that the maximum value of I_{o1max} is achieved only in the first phase of falling of the output signal. As the output voltage (in a voltage follower configuration) decrease, the output current of the first stage decrease as well, which slows down the falling process. Thus, the real SR- can be lower than calculated from (10).

The positive slew-rate (SR+) is limited rather by the intermediate stage and can be estimated as:

$$SR_+ \approx \frac{I_{D5}}{C_{o2}+C_{C2}} \tag{12}$$

As it can be concluded from (10) and (12) in general case one can expect an unsymmetrical large-signal behavior of the amplifier.

D. INPUT NOISE AND DYNAMIC RANGE

The input noise of the OTA is determined by its input stage. Given that M_1 is identical with M_2 ($I_{D1} = I_{D2}$), which guarantees optimum noise performance [15], the input-referred thermal and flicker noise densities ($\bar{v}_t^2$ and $\bar{v}_{1/f}^2$ respectively) in a weak inversion region can be expressed as:

$$\bar{v}_t^2 = \frac{8kT}{3g_{mb1,2}}\left(\frac{g_{m1,2}}{g_{mb1,2}} + \frac{g_{m3,4}}{g_{mb1,2}}\right) \tag{13}$$

$$\bar{v}_{1/f}^2 = \frac{1}{fC_{OX}g_{mb1}^2}\left(\frac{K_{fp}g_{m1,2}^2}{W_{1,2}L_{1,2}} + \frac{K_{fn}g_{m3}^2}{2W_3L_3} + \frac{K_{fn}g_{m4}^2}{2W_4L_4}\right) \tag{14}$$

where K_{fn}, K_{fp} are the flicker noise constants for n- and p-channel transistors respectively and the other symbols have their usual meaning.

Considering only the thermal noise (which is dominant in most cases due to the low biasing currents) and assuming the maximum amplitude of the input signal equal to $V_{DD}/2$, the biasing currents of the input stage ($I_{D1} = I_{D2}$) for the assumed dynamic range (DR) in a voltage follower configuration can be calculated using the following equation [6]:

$$I_{D1,2} = \frac{1}{4}DR^2\frac{8kT(\frac{\pi}{2})f_{GBW}2n_pV_T2\sqrt{2}}{3\eta^2\left(V_{DD}/2\sqrt{2}\right)^2} \tag{15}$$

Thus, the required biasing current $I_{D1,2}$ is proportional to the GBW product of the amplifier and to the square of the DR. On the other hand, the current $I_{D1,2}$ is inversely proportional to the square of the parameter η, so maintaining the same DR and GBW using the BD approach entails worse power effectiveness of the overall structure as compared with the gate-driven (GD) approach.

III. OTA DESIGN

Due to the ULV operation of the considered structure, where the input noise and DR are one of the main concerns, the design has been started with calculating the value of the required biasing currents of the input stage, using eqn. (15). This determined also the value of the input transconductance g_{m1} [see (6)]. Assuming DR = 60 dB (η = 0.36, $n_p = 1.35$,)), from (15) the current I_{D1} was found to be 2.5 nA for $V_{DD} = 0.3$V.

As it was shown in [16], to achieve power optimization, the transconductance g_{m3} should be equal to $2g_{m1} + g_{m2}$, while it is suggested to choose the g_{m2}/g_{m1} ratio between 4 and 7. Taking the above into account, from (6)-(8), we achieve:

$$I_{D5,6} = (4 \ldots 7) \cdot 2\eta I_{D1} \frac{n_p}{n_n} \tag{16}$$

$$I_{D9,10} = 4\eta \frac{n_n}{n_p} I_{D1} + I_{D5,6} \tag{17}$$

Thus, with $n_n/n_p \approx 1$, assuming $g_{m2}/g_{m1} = 5.56$ we set the value of $I_{D5,6}$ to 10 nA. Consequently, from (17) the value of $I_{D9,10}$ was calculated to be 13.6 nA, which was rounded up to 15 nA, to achieve the $I_{D9,10}/I_{D1}$ ratio to be an integer number.

For the given biasing currents of OTA the circuit was dimensioned during the simulation phase. The channel lengths of transistors (L) were chosen relatively large to increase their output resistances, and hence their intrinsic voltage gains. Only for M_7 and M_9 the channel lengths were lower, to decrease their C_{gs} capacitances, and consequently increase the frequency of the parasitic pole p_p, associated with the drain/gate node of M_7, which should be located well above the GBW product of OTA. The current $I_{D7,8}$ was chosen to be $I_{D9,10}/4$. This value was also a result of a compromise between the total dissipation power and the frequency of p_p. For the assumed L, the channel widths (W) of all transistors were adjusted to achieve $|V_{GS}| \approx V_{DD}/2$, which results in a maximum voltage headroom for possible changes of $|V_{GS}|$, caused by the process and temperature variations. It is also worth noting, that minimum channel areas for transistors in the input stage are constrained by the required offset of OTA and flicker noise.

Once the circuit was dimensioned, the parasitic capacitance C_{o2} was estimated to be 0.31 pF. The capacitance C_{C2} was then assumed to be 0.6 pF, i.e. the capacitance C_{o2} was around 1/3 of the sum $C_{C2} + C_{o2}$, and the nonlinear capacitors $C_{bd5} + C_{bd6}$ were around 10 % of this sum. Next, from (5), replacing C_{C2} with C_{C2}' and assuming C_L = 20pF, $\Phi = 68°$, the capacitance C_{C1} was calculated to be 2.4 pF. Thus, the anticipated GBW was 3.45 kHz.

IV. RESULTS AND COMPARISON

A. IMPLEMENTATION

The circuit has been implemented in a 0.18 μm CMOS process from TSMC, with threshold voltages of around $\pm$0.5V. The supply voltage was 0.3 V ($\pm$0.15 V during measurement) and the biasing current I_B was 2.5 nA (provided externally). The circuit performance was also tested for V_{DD} = 0.5V/I_B = 40nA. The transistor aspect ratios are shown in Table 1. The circuit was dimensioned as described in section III. The small-signal parameters of the design are summarized in Table 2, while Fig.3 shows the microphotograph of the fabricated OTA.

TABLE 1. Transistor aspect ratios.

Device	W/L [µm/µm]	Device	W/L [µm/µm]
M_{1A}, M_{1B},M_{2A}, M_{2B}	15/1	M_7	40/0.2
M_{3A}, M_{3B}	20.6/1	M_8	30/1
M_{4A},M_{4B}	15/0.5	M_9	4x40/0.2
M_5,M_{13}	25/0.5	M_{10}	6x20.6/1
M_6	4x20.6/1	M_{11}, M_{12}	15/0.5

TABLE 2. Small-Signal Parameters of OTA for V_{DD} = 0.3V, I_B = 2.5 nA.

Parameter	Value
g_{m1}	51.8 nA/V
g_{m2}	292 nA/V
g_{m3}	438 nA/V
g_{mFF}	437 nA/V
C_{C1}	0.6 pF
C_{C2}	2.4 pF

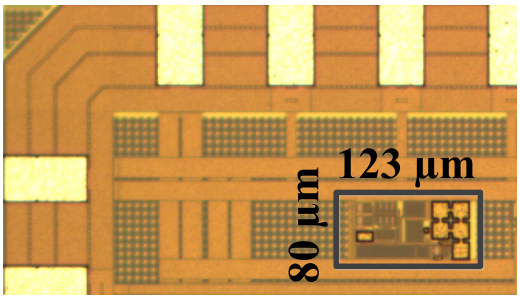


FIGURE 3. Microphotograph of the fabricated OTA.

B. EXPERIMENTAL RESULTS

Below, the measured performance of the test chip is presented. Since the parasitic load capacitance of our printed circuit board exceeded 20 pF, the test chip was measured for C_L = 30pF. This capacitance was fine-tuned and measured with a precise RLC meter E498A from Agilent.

Fig.4 shows the open-loop frequency responses of OTA, measured for two supply voltages (0.3 V and 0.5 V) and two

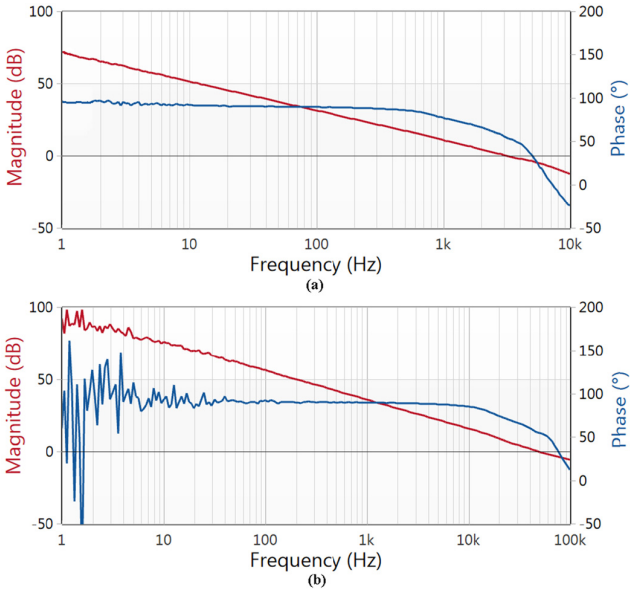


FIGURE 4. Open-loop frequency characteristics of OTA for (a) $V_{DD} = 0.3$ V, $I_B = 2.5$ nA, (b) $V_{DD} = 0.5$V, $I_B = 40$ nA.

corresponding biasing currents I_B (2.5nA and 40 nA). Due to the limitations of our vector network analyzer (Bode 100), the characteristics were measured for f > 1Hz. The voltage gains at 1 Hz were 71.4 and 93 dB for the 0.3 and 0.5-V version respectively.

The value of a DC voltage gain was found to be 98.1 dB and 103.6 dB for a 0.3-V and 0.5-V version respectively.

Figs. 5 and 6 show the selected small-signal parameters (GBW, Φ, A_{vo}) against the input common-mode voltage V_{icm} for $V_{DD} = 0.3$V. The quiescent output level of V_{out} was equal to V_{icm}. The measured A_{vo} remained larger than 85 dB for V_{icm} ranging from 50 mV to 250 mV, i.e. 50 mV for each supply rail. The measured variations of GBW and Φ remained relatively small ($\pm$4.5 % for GBW) with V_{icm} ranging from 50 mV to 250 mV, that proves small variation of the input transconductance of the OTA. Due to the limited voltage swing, and operation with $V_{BS} < 0$ in the whole input range,

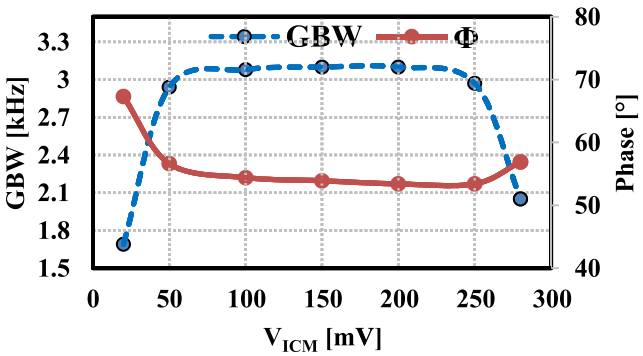


FIGURE 5. GBW and phase margin of OTA against the input common-mode voltage, $V_{DD} = 0.3$V, $I_B = 2.5$nA, $C_L = 30$pF.

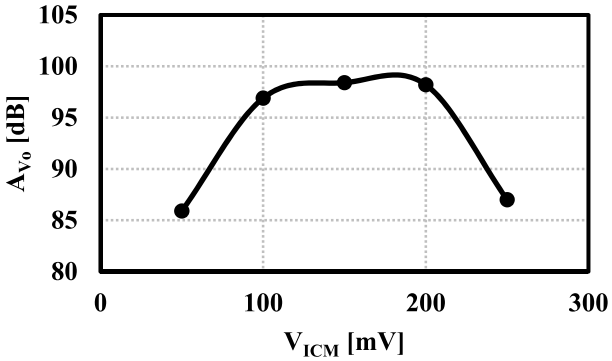


FIGURE 6. DC voltage gain of OTA against the input common-mode voltage, $V_{DD} = 0.3$V, $I_B = 2.5$nA.

the relative variations of the input transconductance were lower than observed for other BD input stages supplied with larger V_{DD} [21]. Fig. 7 shows the large-signal step responses of the OTA for an input step of V_{DD}-50 mV peak-to-peak. The overshoots and oscillations of the responses are on acceptable level. Both responses showed SR+ > SR−, that was in agreement with theoretical expectations (see (10) and (12)).

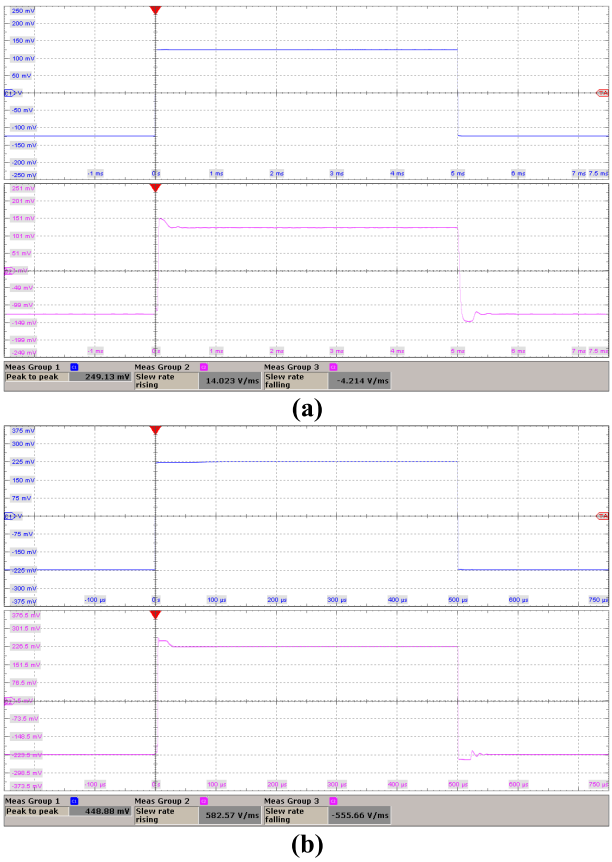


FIGURE 7. Step responses of OTA for (a) $V_{DD} = 0.3$ V, $I_B = 2.5$ nA f = 100 Hz, horiz: 1ms/div, vert: 50 mV/div, (b) $V_{DD} = 0.5$V, $I_B = 40$ nA, f = 1kHz, horiz: 100 μs/div, vert: 75 mV/div.

In Fig. 8 the sine-wave responses for rail-to-rail input are presented, showing, that the input and output

TABLE 3. Performance summary of the 3-stage OTA.

Parameter	meas.	sim.		meas.	sim.	
V_{DD}, [V]	0.3			0.5		
C_L, [pF]	30	30	20	30	30	20
I_B, [nA]	2.5	2.5	2.5	40	40	40
A_{vo}, @ DC [dB]	98.1	98.4	98.4	103.6	105	105
A_v @ 1 Hz [dB]	71.4	70.0	70.0	92.0	93.0	93.0
GBW, [kHz]	3.1	3.56	3.58	49.2	56.1	56.4
Phase margin, [°]	54.2	53.9	63.7	54.8	54	63.9
SR+, [V/ms]	14	13.7	18.3	583	697	840
SR-, [V/ms]	4.2	4.9	5.17	556	348	352
1% settling time, [µs]	252	244	201	26	18.2	16.4
Input referred offset, [mV]	3.1[a)]	3.19[b)]	3.19[b)]	3.0[a)]	3.18[b)]	3.18[b)]
CMRR @ DC, [dB]	60	77.2	77.2	65	82.8	82.8
PSRR @ DC, [dB]	61	87.8	87.8	65	86.8	86.8
Input noise [c)], [μV/Hz$^{1/2}$]	-	1.8	1.8	-	0.5	0.5
Dissipation power, [nW]	13	12.88	12.88	346	346	346
Input current (0-V_{DD}), [pA]	< 100	< 80	< 80	< 15e3	<14e3	<14e3
Silicon area, [mm^2]	0.00984 (123 µm x 80 µm)					

a) std. dev. for 5 measured samples
b) std. dev. (MC 200 runs)
c) thermal noise

common-mode ranges are both rail-to-rail. The Total Harmonic Distortion (THD) for a 0.3-V version was 0.49 % for $V_{in} = 250$ mV_{pp} and f=10 Hz.

Table 3 summarizes the simulated and measured performances of the OTA for two supply voltages. The circuit was simulated for $C_L = 20$ pF (value used in design) and $C_L = 30$ pF (used in measurements). The simulated value of Φ for $C_L = 20$ pF was 63.7°, and was quite close to the value predicted theoretically (68°). The small difference between the theoretical and simulated values may be attributed to the second order effects, mainly the impact of the parasitic pole p_p, associated with M_7. Note, that neglecting the C_{o2} in the design leads to a phase error exceeding 10°.

The values of the measured A_{vo}, GBW and other parameters were in good agreement with simulations. Larger differences were observed only for CMRR and PSRR, however, both parameters remain on acceptable levels. The simulated DC voltage gains for $V_{DD} = 0.5$V were larger than for $V_{DD} = 0.3$V due to the larger V_{DS} voltages of MOS transistors at the operating point, that entailed slightly larger output resistances of the devices.

The input referred noise was only simulated because of the lack of the proper noise meter. The corner frequency for flicker noise was relatively low (32 Hz) due to the low biasing currents (larger thermal noise) and large transistor channel areas. The total input noise integrated from 0.1 Hz to GBW was 109 μV and was dominated by thermal noise.

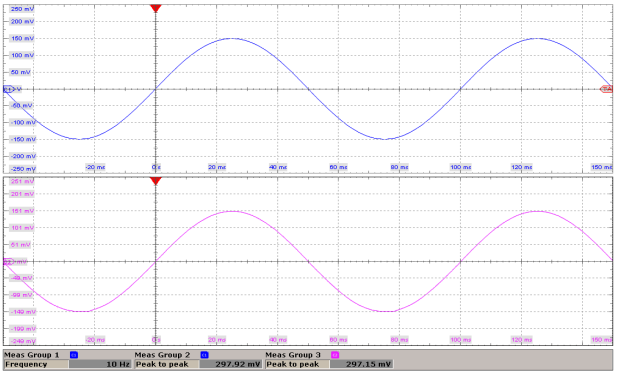
The measured input current of OTA was lower than 100 pA for $V_{DD} = 0.3$V and $V_{icm} = 0$ (i.e. -0.15 V during measurement, where ± 0.15 V supply was used). They are equal to the currents of the forward-biased bulk-source junctions of the input transistors M_1/M_2 and decrease exponentially with V_{icm}.

Table 4 shows the results of Monte Carlo (MC) analysis for $V_{DD} = 0.3$V. As it can be concluded from the results, the design is robust against transistor mismatch.

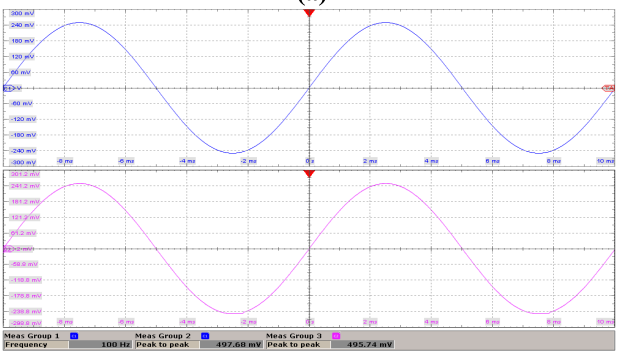
In order to show the circuit sensitivity against process and temperature (P/T), the simulated results of corner and temperature analysis for $V_{DD} = 0.3$ V are shown in Table 5. The results of the simulations prove, that the circuit is robust also against P/T variations. Larger changes were observed only for SR, which may be attributed mainly to the variations of $|V_{GS}|$ voltages of transistors, that affected the maximum output currents of the amplifier gain stages in an ULV environment.

C. PERFORMANCE COMPARISON

Table 6 presents a comparison of the proposed OTA with other fabricated ultra-low-voltage OTAs ($V_{DD} \leq 0.7$ V). As it can be concluded, the proposed design offers the best DC voltage gain, much higher than achieved in other designs



(a)



(b)

FIGURE 8. Sine wave responses of OTA for rail to rail input; (a) 0.3V/2.5 nA, (10 Hz), horiz: 20ms/div, vert: 50 mV/div, (b) 0.5V/40 nA (100 Hz), horiz: 2 ms/div, vert: 60 mV/div.

and one of the lowest relative supply voltages (V_{DD}/V_{TH}), the same as achieved in the best so far designs [6], [7]. The noise properties of the compared circuits differ significantly, since the input noise highly depends on the biasing currents (GBW product of OTA), and the type of the input stage (BD or GD). In general, the solutions based on the GD approach show lower input noise, at the cost of a lower ICMR. The design proposed here show similar noise as other deep sub 0.5-V amplifiers with similar bandwidth and rail-to-rail input.

In order to compare small-signal and large-signal power effectiveness of the OTAs in Table 6, the following standard figures of merit (FOMs) have been adopted:

$$IFOM_S = \frac{GBW \cdot C_L}{I_{DD}} \tag{18}$$

$$IFOM_L = \frac{SR_a \cdot C_L}{I_{DD}} \tag{19}$$

where $SR_a = (SR_+ + SR_-)/2$ is the average slew-rate and I_{DD} is the total supply current. In order to better compare the low voltage capabilities of the OTAs in Table 6, the next two FOMs have been used, which refer the small-signal bandwidth and SR to the total dissipation power P_{diss} rather than I_{DD}:

$$FOM_S = \frac{GBW \cdot C_L}{P_{diss}} \tag{20}$$

$$FOM_L = \frac{SR_a \cdot C_L}{P_{diss}} \tag{21}$$

TABLE 4. Results of Monte Carlo Analysis, for $V_{DD} = 0.3$ V, $I_B = 2.5$ nA, $C_L = 30$ pF, (200 runs).

Parameter	Mean	Std. dev.	min	max
A_{vo} @ DC, [dB]	98.73	0.053	98.54	98.84
GBW, [kHz]	3.526	0.164	3.062	3.995
Phase margin, [°]	55.5	2.42	48.19	61.37
t_{sett} (1%), [µs]	244.1	0.24	243.44	244.77
CMRR, [dB]	59.28	9.459	43.33	96.55
PSRR, [dB]	61.03	10.33	46.27	122.1
I_{DD}, [nA]	43.05	1.624	38.91	47.25

TABLE 5. Simulated Main Performance Parameters over Process and Temperature Variations for $V_{DD} = 0.3$ V, $I_B = 2.5$ nA, $C_L = 30$ pF.

Parameter (T=27 °C)	SS	SF	TT	FS	FF
P_{diss}, [nW]	12.3	12.83	12.88	12.9	13.3
A_{vo}, [dB]	99.9	96.5	98.4	98.9	95.2
GBW, [kHz]	3.52	3.47	3.56	3.65	3.58
Phase margin, [°]	52.59	54.7	53.9	52.75	54.79
SR+/SR-, [V/ms]	4.3/3.9	12/4.1	13.6/4.9	8.1/5.3	27.9/5.1
CMRR @ DC, [dB]	75.7	76.9	77.2	76	76.3
PSRR @ DC, [dB]	64.3	79.7	87.8	77.5	83.4

Parameter (TT corner)	0°	27°	70°
P_{diss}, [nW]	12.1	12.88	14.3
A_{vo}, [dB]	97.3	98.4	90.8
GBW, [kHz]	3.6	3.56	3.39
Phase margin, [°]	53.8	53.9	53.3
SR+/SR-, [V/ms]	5.1/4.0	13.6/4.9	24/4.5
CMRR @ DC, [dB]	75	77.2	70.5
PSRR @ DC, [dB]	61	87.8	69.2

Process corners: S-slow, F-fast, T-typical, first: n-channel MOS, second p-channel MOS.

As it is can be concluded from Table 6, the proposed circuit outperforms all other designs in terms of $IFOM_L$ and FOM_L, and offers one of the highest values of IFOMs and FOMs. Only the design in [3] offers better FOMs, since it was optimized for particular value of C_L. Nevertheless, the OTA in [3] does not provide a rail-to-rail input range.

As compared with other similar OTAs published recently, [6], [7], the proposed OTA offers larger DC voltage gain and large-signal FOMs (FOM_L and $IFOM_L$). The most important advantage of the structure in [7] is high CMRR and simple topology, while the circuit in [6] offers symmetrical SR.

TABLE 6. Performance comparison of sub 0.7-V Amplifiers.

Parameter	This work	[7] 2020	[8] 2019	[6] 2018	[20] 2016	[5] 2016	[4] 2015	[3] 2014	[2] 2014	[22] 2007	[1] 2005	[1] 2005
Technology, [µm]	0.18	0.18	0.065	0.18	0.18	0.18	0.065	0.18	0.13	0.35	0.18	0.18
V_{DD}, [V]	0.3	0.3	0.25	0.3	0.7	0.5	0.35	0.5	0.25	0.6	0.5	0.5
V_{DD}/V_{TH} [d]	0.6	0.6	0.68	0.6	1.75	1.18	1.16	1.29	1.16	1.02	1.14	1.14
C_L, [pF]	30	30	15	20	20	40	3	30	15	15	20	20
DC gain, [dB]	98.1	> 64.7	70	> 65.8	57.5	77	43	70	60	69.4	62	52
GBW, [kHz]	3.1	2.96	9.5	2.78	3e3	4.0	3.6e3	18	1.88	11.3	10e3	2.5e3
Phase margin, [°]	54	52	88	61	60	56	56	55	52.5	65	-	-
SR+, [V/ms]	14	1.9	2.0	6.44	1.8e3	2.0	5.6e3	3.0	0.64	14	2e3	2.89e3
SR-, [V/ms]	4.2	6.4	2.0	7.80	3.8e3	2.0	5.6e3	3.0	0.77	14	2e3	2.89e3
CMRR @ DC, [dB]	60	110	62.5	72	19	55	46	-	-	75	74.5	78
Thermal noise, [$\mu V/Hz^{1/2}$]	1.8 [e]	1.6[e]	-	1.85[e]	0.10	-	-	0.31	3.3	0.29	0.070	0.080
Power, [nW]	13	12.6	26	15.4	25.4e3	70	17e3	75	18	548	74e3	110e3
Operation mode	BD	BD	BD	BD	BD	GD	BD	GD	BD	BD	GD	BD
ICMR/V_{DD}, [%]	100	100	100	100	79	100	100	60	100	100	20	100
$IFOM_S$, [MHz · pF/mA]	2148	2114	1370	1083	1650	1143	222	3600	392	181	1351	227
$IFOM_L$, [V · pF/µs · mA]	6300	2964	288	2790	1540	571	346	680	146	230	270	263
FOM_S, [MHz · pF/mW]	7154	7047	5481	3610	2357	2286	634	7200	1568	302	2702	455
FOM_L, [V · pF/µs · mW]	21000	9880	1154	9300	2200	1142	989	1360	584	383	540	525
Silicon area, [mm^2]	0.0098	0.0085	0.002	0.0082	0.0198	0.036	0.0050	0.057	0.0830	0.06	0.017	0.026

d) average $|V_{TH}|$
e) simulated value

It is also worth noting, that the 1-V OTA in [16], where similar frequency compensation method was used, showed IFOMs of 20513 MHz · pF/mA at $C_L = 200$pF. However, this IFOMs was proportional to the square root of C_L. Therefore, for $C_L = 30$ pF one could expect the IFOMs of around 8000 MHz · pF/mA. Nevertheless, the above OTA was realized with larger V_{DD} and much lower transistor sizes, that allowed decreasing C_{C2} to 0.15 pF, thus improving the GBW product of OTA. In the design discussed here, the GBW product was constrained by the parasitic capacitances of transistors. The other factors affecting IFOMs in this design were: larger biasing current of the BD input stage for the same transconductance and additional power consumed by the biasing circuit, which was included in the total dissipation power. Nevertheless, the OTA described in this work showed the best performance among all sub 0.5-V OTAs in terms of the DC voltage gain and standard FOMs.

V. CONCLUSION

The paper presents a design of a 0.3-V ultra-low-power OTA. The circuit is based on a three-stage structure with an RNMC compensation scheme and an input stage based on a non-tailed BD differential pair. Design restrictions in an ULV supply conditions are discussed. Experimental verification showed superior performance in terms of standard FOMs and DC voltage gain, as compared with other similar OTAs with sub 0.5-V supply and rail-to-rail input common-mode range.

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