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Analysis and Protection Scheme of Station Internal AC Grounding Faults in a Bipolar MMC-HVDC System

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ABSTRACT The symmetrical bipolar configuration shows a great advantage in modular multilevel converter (MMC) based high-voltage dc-current (HVDC) transmission. In a bipolar MMC-HVDC system, station internal ac grounding faults cause sub-module (SM) capacitors to discharge violently. These faults do great harm to MMCs and require special protection schemes. In this paper, a single-phase-to-ground fault is taken as an example to investigate transient characteristics of station internal ac grounding faults in a bipolar MMC-HVDC system. A calculation theory of fault current based on the improving RLC model and second-order differential equation with variable coefficients is introduced. A novel transient zero-mode current based protection criterion with better reliability, quickness, and ability to endure fault resistances is proposed to detect internal ac grounding faults. The fault clearing strategy applicable to three types of grounding faults is also designed. The correctness of the proposed calculation theory and protection schemes is verified through simulations performed in PSCAD/EMTDC.

INDEX TERMS MMC-HVDC, station internal ac grounding fault, second-order differential equation with variable coefficients, transient zero-mode current, protection scheme.

I. INTRODUCTION

Modular multilevel converter (MMC) based high-voltage dc-current (HVDC) transmission has a good application prospect in fields of renewable energy integration, asynchronous interconnection of grids, and isolated power supply due to its advantages such as modularity, scalability, and high-quality output waveforms [1]–[3]. MMC-HVDC systems can be realized in a bipolar configuration to achieve flexible operation modes and a lower overvoltage level, which conforms to the development trend of dc grids with high voltage, large capacity, and multi terminals [4]–[6].

In recent years, studies for MMC-HVDC systems mainly talk about characteristics of dc faults [7]–[10] and improvement of protection or control strategies [11]–[14]. Existing literature associated with grid-side ac faults mainly focuses on the impact of the faults on control systems [15]–[18]. Without being isolated by the converter transformer, station internal ac grounding faults are more harmful to MMCs and characteristics are notably different from those of grid-side ac faults. Ma *et al.* [19] analyze characteristics of the station internal ac single-phase-to-ground fault and two-phase short circuit fault in the symmetrical monopole MMC-HVDC system. These faults will not cause severe overcurrent in the MMC and do little harm to power electronic devices. Therefore, monopole structure has a low requirement for the quickness of protection and the traditional ac differential protection can meet this requirement. In [20], analysis and calculation of station internal ac three-phase-to-ground faults in a bipolar MMC-HVDC system are carried out. A protection criterion based on the differential current of converter arms is also proposed but it is sensitive to fault resistances. The post-blocking characteristics of the station internal ac single-phase-to-ground fault in the HB-MMC based bipolar HVDC system and FB-MMC based bipolar HVDC system are respectively discussed in [21] and [22]. Some suitable protection schemes are also designed. The control strategies are improved in [23] to suppress overvoltage and overcurrent caused by grounding faults. Li *et al.* [24] put forward a double-thyristor based protection strategy to

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deal with internal single-phase-to-ground fault. A new hybrid arm MMC is introduced in [25] to overcome the overvoltage problem.

Every MMC is equipped with an overcurrent protection of arms, which will operate after grounding faults and block IGBTs. Therefore, all the existing researches neglect the pre-blocking transient characteristics. In fact, SM capacitors discharge sharply before the MMC is blocked. The overcurrent protection of arms is the last barrier to protect IGBTs. The threshold of the overcurrent protection is too high, approaching twice the rated current of IGBTs. If the overcurrent protection of arms fails to operate, IGBTs will be destroyed by discharging currents of SMs within a few milliseconds. If we design a faster protection to detect the grounding fault before IGBTs are blocked by overcurrent and then take some protection measures immediately, fault current can be limited to be smaller and cleared earlier. At the same time, the overcurrent protection of arms can be employed as the backup protection for station internal grounding faults. These two protections cooperate with each other to enhance the reliability of station internal protections and reduce the probability that the converter is destroyed because of single protection failing to operate. However, the common ac differential protection in actual engineering has poor quickness and cannot detect the fault before IGBTs are blocked. Thus, it is significant to analyze pre-blocking transient characteristics and design new protection schemes for station internal ac grounding faults.

In this paper, a symmetrical bipolar MMC-HVDC system is considered. First, the necessity of configuring a fast protection for station internal ac lines is explained. Second, since pre-blocking characteristics are important for developing protection schemes, we take the single-phase-to-ground fault as an example to analyze transient characteristics and calculation theory of station internal ac grounding faults. Third, According to fault characteristics, a novel transient zero-mode current based protection criterion with better quickness, reliability, and ability to endure fault resistances is proposed for internal ac grounding faults, which can operate within 1ms after the fault. A clearing strategy is also designed. Finally, fault analysis, calculation theory, and protection schemes are proved correct in PSCAD/EMTDC.

II. ANALYSIS OF PROTECTION CONFIGURATION FOR STATION INTERNAL AC-LINE PROTECTED ZONE

The typical protection partitioning principle in the MMC-HVDC system is shown in Fig. 1. It consists of seven parts: ac protected zone, converter transformer protected zone, station internal ac-line protected zone, converter protected zone, bipolar protected zone, dc-pole protected zone and dc-line protected zone. Adjacent protected zones overlap each other to protect all electrical equipment without dead zone.

For dc-line protected zone, traveling wave based protection is widely employed as the main protection in practical engineering. Differential under-voltage protection and low voltage protection are usually used as backup protections. Converter protected zone is generally equipped with the overcurrent protection of arms, which will operate and block IGBTs once arm overcurrent is detected.

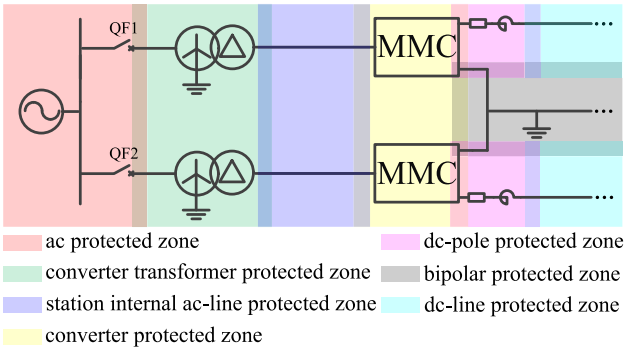

FIGURE 1. Protection partitioning in the MMC-HVDC system.

There are limited researches on the protection for station internal ac-line protected zone. The typical protection scheme in flexible dc systems generally employs ac bus differential protection as the main protection for station internal ac lines. Ac bus overcurrent protection and zero-sequence current protection are used as backup protections. However, it takes several cycles for the power-frequency-based ac bus differential protection to detect the fault, which delays the following protection strategies put into use. For example, the thyristor T_2 in [24] will not be triggered until the station internal ac grounding fault is detected. As a result, the tripping time of the ac breaker will be postponed, which is unexpected in actual engineering. Moreover, as is mentioned in the introduction, we expect the main protection of the station internal ac-line protected zone can operate before the overcurrent protection of arms. Obviously, the quickness of ac bus differential protection cannot meet this requirement. Therefore, it is necessary to investigate the pre-blocking transient characteristics and put forward a new protection with better quickness to detect station internal ac grounding faults.

III. ANALYSIS OF FAULT TRANSIENT CHARACTERISTICS

Grounding faults on station internal ac lines and those on valve-side leads of the transformer have same characteristics, so they are collectively called station internal ac grounding faults here and can be divided into three types: single-phase-to-ground faults, two-phase-to-ground faults and three-phase-to-ground faults. Transient characteristics of two asymmetric grounding faults are similar and the only difference is the number of faulted phases. A three-phase-to-ground fault can be considered as a special asymmetrical fault and it doesn't have non-faulted phases. In view of this, this paper takes the single-phase-to-ground fault as an example to illustrate the characteristics and calculation method of station internal ac grounding faults. In practical engineering, the IGBT's ability to withstand overcurrent and interrupting capacity of DCCBs must match fault current level. Therefore,

the fault current calculation provides an important reference for the selection of electrical equipment. In addition, the fault current calculation will theoretically verify correctness of the fault characteristic analysis and support the design of the main protection for station internal ac-line protected zone. The transient switching process of SMs and control strategies of MMCs are considered before the converter is blocked. In the improved RLC model, the equivalent capacitor is expressed as a variable related to control strategies. Before the MMC is blocked, the fault current can be obtained by solving a second-order differential equation with variable coefficients. The proposed calculation method can be used to accurately calculate the discharging current of a single bridge arm and the discharging current between several bridge arms. The specific analysis is as follows:

A. DISCHARGING CURRENT OF SM CAPACITORS ON THE LOWER ARM OF FAULTED PHASES

As shown in Fig. 2, when a single-phase-to-ground fault occurs in phase A, on-state SM capacitors on the lower arm of phase A discharge acutely from the grounding point on metallic return to the fault point (F), causing severe overcurrent in the fault path. The MMC needs to be blocked immediately. After that, the current freewheels through diodes and arm inductances and decays slowly. The fault current is shown as $i_{f\,\mathrm{sm1}}$.

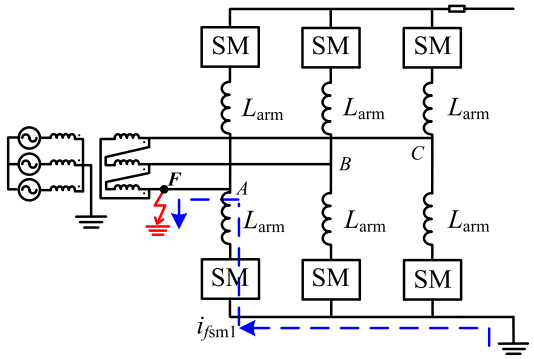

FIGURE 2. Discharging current of lower arm SM capacitors in phase. A.

In normal operation, the number of on-state SMs on the lower arm of phase A can be expressed as:

$$n_{A2}(t) = \frac{N}{2} + f\left(\frac{v_A^*(t)}{U_C}\right) \tag{1}$$

where N is the total number of SMs on a bridge arm, $v_A^*(t)$ is the modulation voltage of phase A, U_C is the average voltage of SM capacitors and f represents the rounding function.

Within a few milliseconds before the MMC is blocked, the modulation strategy is considered to have no obvious distortion. The number of on-state SMs on the lower arm of phase A can be estimated by (1).

Fig. 3 illustrates the improving RLC equivalent circuit of the discharging path in Fig. 2. L_1 represents the lower arm inductance in phase A with $L_1 = L_{\mathrm{arm}}$. R_1 is the equivalent

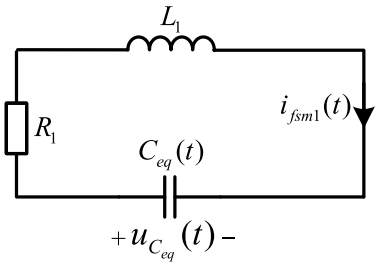

FIGURE 3. Improving RLC equivalent circuit.

resistance. According to real-time equivalent principle, the equivalent capacitor becomes $C_{\mathrm{eq}}(t) = C_0/n_{\mathrm{A2}}(t)$. $i_{f\,\mathrm{sm1}}(t)$ is the discharging current of SM capacitors and $u_{\mathrm{Ceq}}(t)$ is the equivalent voltage across $C_{\mathrm{eq}}(t)$.

According to Fig. 3, relationships in (2) can be obtained.

$$\begin{cases} u_{C_{eq}}(t) = L_1 \dfrac{di_{fsm1}(t)}{dt} + R_1 i_{fsm1}(t) \\ i_{fsm1}(t) = -C_{eq}(t) \dfrac{du_{C_{eq}}(t)}{dt} \end{cases} \tag{2}$$

There is the following constraint between $u_{\mathrm{Ceq}}(t)$ and $n_{\mathrm{A2}}(t)$:

$$u_{C_{eq}}(t) = n_{A2}(t) \times \overline{u}_{sm}(t) \tag{3}$$

where $\overline{u}_{sm}(t)$ is the average voltage of SM capacitors on a bridge arm.

According to (2) and (3), a second-order differential equation with variable coefficients for $\overline{u}_{sm}(t)$ can be derived as follows:

$$\frac{d^2\overline{u}_{sm}(t)}{dt^2} + f(t)\frac{d\overline{u}_{sm}(t)}{dt} + g(t)\overline{u}_{sm}(t) = 0 \tag{4}$$

where

$$g(t) = \frac{n''_{A2}(t)}{n_{A2}(t)} + \frac{R_1 n'_{A2}(t)}{L_1 n_{A2}(t)} + \frac{n_{A2}(t)}{L_1 C_0} - \left(\frac{n'_{A2}(t)}{n_{A2}(t)}\right)^2,$$
$$f(t) = \frac{n'_{A2}(t)}{n_{A2}(t)} + \frac{R_1}{L_1}.$$

$n'_{A2}(t)$ and $n''_{A2}(t)$ are the first derivative and the second derivative of $n_{\mathrm{A2}}(t)$, respectively. $n_{\mathrm{A2}}(t)$ is a step function whose all-order derivatives equal to zero except discontinuous points. Since there is no significance to consider a single point in practical engineering, the paper ignores these points and considers $n_{\mathrm{A2}}(t)$ as a piecewise constant whose all-order derivatives are equal to zero. In view of this, (4) can be simplified as follows:

$$\frac{d^2\overline{u}_{sm}(t)}{dt^2} + \frac{R_1}{L_1}\frac{d\overline{u}_{sm}(t)}{dt} + \frac{n_{A2}(t)}{L_1 C_0}\overline{u}_{sm}(t) = 0 \tag{5}$$

$\overline{u}_{sm}(t)$ can be obtained by solving this differential equation and then $i_{f\,\mathrm{sm1}}(t)$ can be derived as follows:

$$i_{f\,\mathrm{sm1}}(t) = -C_0 \frac{d\overline{u}_{sm}(t)}{dt} \tag{6}$$

After the MMC is blocked, the fault current freewheels through diodes and arm inductances. The post-blocking equivalent circuit is a first-order RL circuit and the lower arm current in phase A can be derived:

$$i'_{fsm1}(t) = I_0 e^{-\frac{R_1}{L_1}t} \tag{7}$$

where I_0 is the lower arm current at the moment of blocking the MMC.

B. DISCHARGING CURRENT OF SM CAPACITORS IN NON-FAULTED PHASES

As is shown in Fig. 4, when a grounding fault occurs at F in phase A, on-state SM capacitors in non-faulted phases (phase B and phase C) will discharge acutely, causing severe overcurrent on bridge arms. On-state SM capacitors on the upper arm of phase A will also be overcharged by the fault current. The MMC should be blocked immediately to cut off the discharging process of SM capacitors. After that, the current freewheels through diodes, arm inductances, and upper arm capacitors in phase A. The fault current is shown as $i_{f\,\mathrm{sm2}}$.

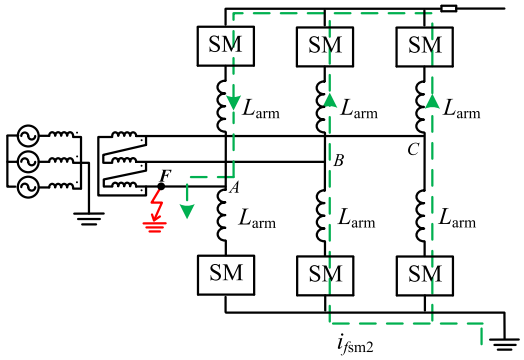

FIGURE 4. Discharging current of SM capacitors in non-faulted phases.

Before the MMC is blocked, only on-state SM capacitors on the upper arm of phase A are charged, as shown in Fig. 5. The discharging path of phase B and phase C are similar. Taking phase B as an example, we can achieve the equivalent circuit shown in Fig. 6.

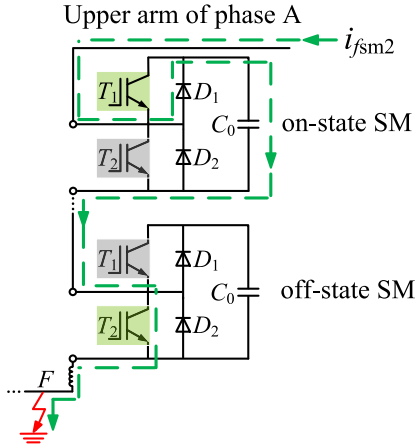

FIGURE 5. Charging current on the upper arm of phase A.

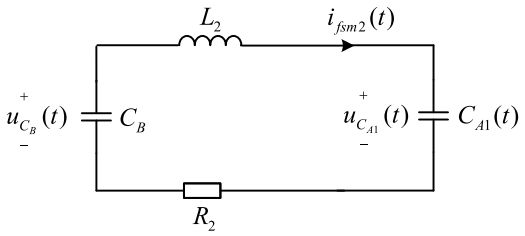

FIGURE 6. Equivalent circuit of the discharging path.

L_2 represents the equivalent inductance with $L_2 = 3L_{\mathrm{arm}}$. R_2 is the equivalent resistance. The equivalent capacitor of the upper arm in phase A becomes $C_{\mathrm{A1}}(t) = C_0/n_{\mathrm{A1}}(t)$, where $n_{\mathrm{A1}}(t)$ represents the number of on-state SMs on the upper arm of phase A, as is shown in (8).

$$n_{A1}(t) = \frac{N}{2} - f\left(\frac{v_A^*(t)}{U_c}\right) \tag{8}$$

The number of on-state SMs in phase B is always equal to N, so its total capacitance is C_0/N. The number of off-state SMs is also equal to N and its total capacitance is C_0/N too. These two parts of capacitors will be inserted and discharge in turns due to the capacitor voltage balance control. Because the switching process is very short, the discharging process can be viewed as two same capacitors discharging in parallel [26]. Thus, the equivalent capacitor of phase B becomes $C_{\mathrm{B}} = 2C_0/N$.

According to Fig. 6, the following relationships can be obtained:

$$\begin{cases} u_{C_B}(t) = u_{L_2}(t) + u_{R_2}(t) + u_{C_{A1}}(t) \\ i_{fsm2}(t) = -C_B \dfrac{du_{C_B}(t)}{dt} = C_{A1}(t) \dfrac{du_{C_{A1}}(t)}{dt} \\ u_{C_{A1}}(t) = n_{A1}(t) \times \overline{u}_{sm}(t) \end{cases} \tag{9}$$

A second-order differential equation with variable coefficients for $\overline{u}_{sm}(t)$ can be derived as follows from (9):

$$\frac{d^2\overline{u}_{sm}(t)}{dt^2} + \frac{R_2}{L_2}\frac{d\overline{u}_{sm}(t)}{dt} + \left(\frac{N + 2n_{A2}(t)}{2L_2C_0}\right)\overline{u}_{sm}(t) = \frac{A_1}{L_2C_0} \tag{10}$$

where $A_1 = u_{C_B}(0) + \frac{C_{A1}(0)}{C_B} u_{C_{A1}}(0)$.

$\overline{u}_{sm}(t)$ can be obtained by solving this differential equation and then $i_{f\,\mathrm{sm2}}(t)$ can be derived as follows:

$$i_{fsm2}(t) = C_0 \frac{d\overline{u}_{sm}(t)}{dt} \tag{11}$$

After the MMC is blocked, the discharging current of phase B freewheels through diodes and arm inductances, which will charge all upper arm SM capacitors in phase A, as shown in Fig. 7. The equivalent circuit is shown in Fig. 8, where R'_2 represents the equivalent resistance of the fault path, $C'_{A1}(t) = C_0/N$, and $L'_2 = 3L_{\mathrm{arm}}$.

According to Kirchhoff's Voltage Law (KVL), the following expression can be derived:

$$L'_2C'_{A1}\frac{d^2u_{C'_{A1}}(t)}{dt} + R'_2C'_{A1}\frac{du_{C'_{A1}}(t)}{dt} + u_{C'_{A1}}(t) = 0 \tag{12}$$

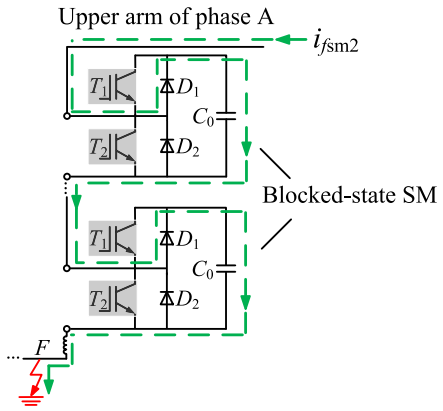

FIGURE 7. Charging current on the upper arm in phase A.

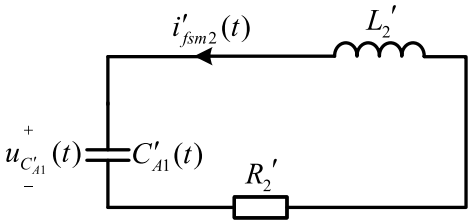

FIGURE 8. Equivalent circuit of the freewheeling path.

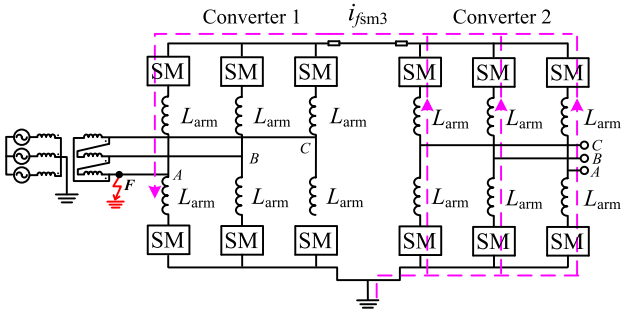

FIGURE 9. Pre-blocking discharging current of SM capacitors in the opposite positive MMC.

It is a second-order differential equation with constant coefficients in (12) and the expression of the freewheeling current can be obtained:

$$i'_{fsm2}(t) = -C'_{A1}U_0 e^{-\beta t}(\beta\cos\omega t + \omega\sin\omega t) + \frac{I_0 + C'_{A1}U_0\beta}{\omega} e^{-\beta t}(\omega\cos\omega t - \beta\sin\omega t) \quad (13)$$

where I_0 and U_0 are values of $i_{fsm2}(t)$ and $u_{C_{A1}}(t)$, respectively when the MMC is blocked. $\omega = \sqrt{\omega_0^2 - \beta^2}$, $\omega_0 = \sqrt{\frac{1}{L'_2 C'_{A1}}}$, $\beta = \frac{R'_2}{2L'_2}$.

C. DISCHARGING CURRENT OF SM CAPACITORS IN THE OPPOSITE POSITIVE MMC

As shown in Fig. 9, when a grounding fault occurs at F in phase A, on-state SM capacitors in the opposite positive MMC discharge through dc lines. On-state SM capacitors on the upper arm of phase A will be charged continually by the fault current shown as i_{fsm3}. The charging mechanism is the same as that in Fig. 5.

The fault causes severe overcurrent on dc lines and overvoltage on upper arm capacitors in phase A. i_{fsm2} flows through T_1 of on-state SMs in non-faulted phases, producing a forward voltage drop across T_1. As a result, D_1 will be reverse-biased and i_{fsm3} cannot feed into non-faulted phases, as shown in Fig. 10.

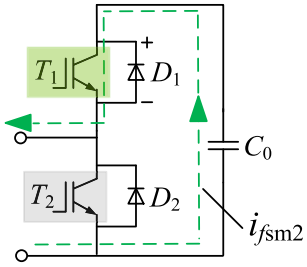

FIGURE 10. D_1 is reverse-biased.

After the faulted MMC is blocked, i_{fsm3} continues to freewheel into the upper arm of phase A until decaying to zero. In addition, the discharging current begins to feed into non-faulted phases when i_{fsm2} decays to zero and the following relationship is satisfied:

$$u_{dc} - u_f > u_C \quad (14)$$

where u_{dc} represents the dc voltage, u_f is the ac voltage of non-faulted phases and u_C is total capacitor voltages of upper arm in non-faulted phases. This fault current is illustrated in Fig. 11.

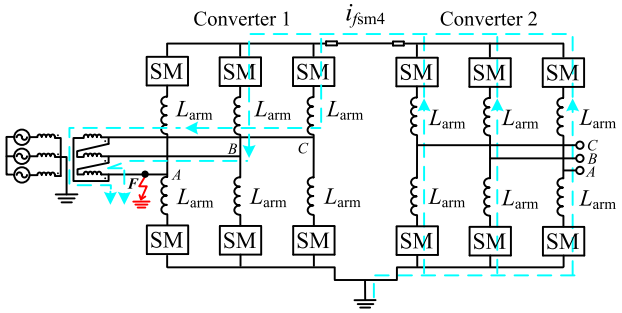

FIGURE 11. Discharging current feeding into non-faulted phases.

Fig. 12 describes the equivalent circuit of the pre-blocking discharging path. C_2 represents the equivalent capacitor of the opposite positive MMC with $C_2 = 6C_0/N$. $C_{A1}(t)$ is the equivalent capacitor of the upper arm in phase A with $C_{A1}(t) = C_0/n_{A1}(t)$. R_3 represents the equivalent resistance and the equivalent inductance becomes $L_3 = L_{S1} + L_l + L_{S2} + 2L_p$. L_{S1} is the upper arm inductance in phase A of Converter 1, L_l is the equivalent inductance of dc lines, L_{S2} is the equivalent inductance of Converter 2 and L_p is the inductance of the current limiting reactor.

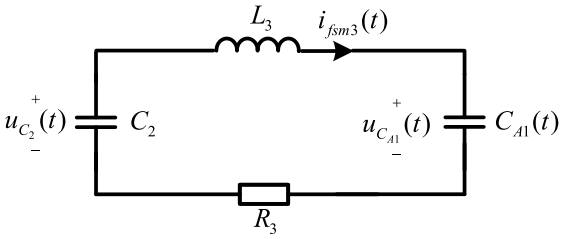

FIGURE 12. Equivalent circuit of the pre-blocking discharging path.

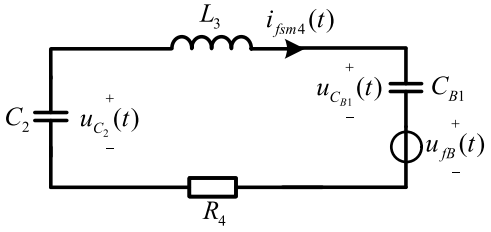

FIGURE 13. Equivalent circuit of the charging path in phase B.

The only difference between the equivalent circuit in Fig. 12 and that in Fig. 6 is the values of constants, so the solution is exactly the same. A second-order differential equation with variable coefficients for $\overline{u}_{sm}(t)$ can be obtained:

$$\frac{d^2\overline{u}_{sm}(t)}{dt^2}+\frac{R_3}{L_3}\frac{d\overline{u}_{sm}(t)}{dt}+\frac{N+6n_{A1}(t)}{6L_3C_0}\overline{u}_{sm}(t)=\frac{A_2}{L_3C_0} \tag{15}$$

where $A_2 = u_{C_2}(0) + \frac{C_{A1}(0)}{C_2}u_{CA1}(0)$.

$\overline{u}_{sm}(t)$ can be obtained by solving this differential equation and then $i_{f\,\mathrm{sm3}}(t)$ can be derived as follows:

$$i_{fsm3}(t) = C_0\frac{d\overline{u}_{sm}(t)}{dt} \tag{16}$$

After the faulted MMC is blocked, the fault current will feed into three-phase upper arms of the faulted MMC if (14) is satisfied. The calculation of freewheeling current in phase A is similar to that in Fig. 12 and the only distinction between them is that $C_{\mathrm{A1}}(t)$ becomes constant with $C_{\mathrm{A1}}(t) = C_0/N$. Thus, it won't be repeated here. The post-blocking charging paths in phase B and phase C are similar. The equivalent circuit is illustrated in Fig. 13 by taking phase B as an example.

C_2 and L_3 in Fig. 13 are identical to those in Fig. 12. C_{B1} represents the equivalent capacitor of the upper arm in phase B with $C_{\mathrm{B1}} = C_0/N$. R_4 is the equivalent resistance and $u_{f\mathrm{B}}(t)$ is the ac voltage of phase B after the MMC is blocked. Based on Fig. 13, the following relationships can be obtained:

$$\begin{cases} u_{C_2}(t) = R_4 i_{fsm4}(t) + L_3\dfrac{di_{fsm4}(t)}{dt} + u_{C_{B1}}(t) + u_{fB}(t) \\ u_{fB}(t) = U_m\sin(\omega t+\theta) \\ i_{fsm4}(t) = -C_2\dfrac{du_{C_2}(t)}{dt} = C_{B1}\dfrac{du_{C_{B1}}(t)}{dt} \end{cases} \tag{17}$$

where θ and U_m are the phase and amplitude of the ac voltage of phase B when the MMC is blocked, respectively.

According to (17), $i_{f\,\mathrm{sm4}}$ can be derived as follows:

$$\begin{aligned} i_{fsm4}(t) = {} & C_2e^{-\beta t}(\beta A_2+\omega' A_1)\sin\omega' t \\ & +C_2e^{-\beta t}(\beta A_1-\omega' A_2)\cos\omega' t \\ & +K_1C_2\omega\sin\omega t - K_2C_2\omega\cos\omega t \end{aligned} \tag{18}$$

where $\beta = R_4/2L_3$, $\omega_0 = \sqrt{7/L_3C_2}$, $\omega' = \sqrt{\omega_0^2-\beta^2}$, $A = u_{B1}(0) + C_2u_{C_2}(0)/C_{B1}$, $A_1 = u_{C_2}(0) - K_1 - A/7$, $A_2 = [C_2\beta A_1 - I_0 - C_2\omega K_2]/C_2\omega'$. $u_{B1}(0)$, $u_{C_2}(0)$, and I_0 are initial values. K_1 and K_2 are regulated by the following equations:

$$\begin{cases} \omega^2L_3K_1 - R_4\omega K_2 - 7K_1/C_2 + U_m\sin\theta/C_2 = 0 \\ \omega^2L_3K_2 + R_4\omega K_1 - 7K_2/C_2 + U_m\cos\theta/C_2 = 0 \end{cases} \tag{19}$$

D. ANALYSIS OF AC CURRENT

Within a few milliseconds before the MMC is blocked, the distortion of ac current is much less than values of discharging current of SM capacitors. The discharging current plays a dominant role in pre-blocking characteristics. Therefore, this paper neglects the change of ac current and only analyzes and calculates the discharging current of SM capacitors accurately to provide reference for practical engineering.

After the MMC is blocked, lower arms of non-faulted phases will produce large fault current with dc offsets, resulting in grid-side ac current exhibiting no zero-crossings. As a result, the grid-side ACCB cannot be tripped. These have been expounded in [21] and will not be repeated here.

IV. PROTECTION SCHEMES

At present, there is little research on the main protection for station internal ac-line protected zone in the bipolar MMC-HVDC system. The protection proposed in [20] is sensitive to fault resistance and the quickness of the existing ac differential protection cannot meet the requirement mentioned in the introduction. Therefore, this section will develop a fast protection for station internal ac grounding faults based on fault characteristics analyzed in Section III. The reach of protection covers valve-side leads of the transformer and station internal ac lines. The proposed protection can operate within 1ms after the fault occurs, which is much earlier than the blocking time of IGBTs (verified in Section V-E). Thus, the proposed protection can cooperate with the overcurrent protection of arms very well. Another advantage of the proposed protection is the better ability to endure fault resistances. The proposed fault clearing strategy can clear the fault completely within 3ms after the fault is detected.

A. TRANSIENT ZERO-MODE CURRENT-BASED PROTECTION CRITERION FOR STATION INTERNAL AC GROUNDING FAULTS

The transient zero-mode current can be expressed as follows:

$$3i_0 = (i_A + i_B + i_c) \tag{20}$$

where i_{A}, i_{B}, and i_{C} represent ac phase current.

In normal operation, the transient zero-mode current $3i_0$ at the ac-side of the MMC equals to zero since ac systems are symmetrical. When a station internal ac grounding

fault occurs, current at the ac-side of the MMC contain ac zero-sequence current and discharging current of SM capacitors. Thus, the transient zero-mode current $3i_0$ is unequal to zero. This paper determines whether an internal ac grounding fault has occurred by detecting $|3i_0|$ at the ac-side of the MMC. Since CTs are seldom installed on station internal ac lines, the sum of current on six bridge arms of the MMC are employed to represent $|3i_0|$ indirectly. The protection criterion is expressed as follows:

$$|3i_0| = \left| \sum_{j=A,B,C} (i_{j\_up} + i_{j\_down}) \right| > \Delta_1 \tag{21}$$

where i_{j_up} represents the upper arm current in phase j of the MMC and i_{j_down} is the lower arm current. The positive direction of them is from dc poles to ac lines. Δ_1 is the threshold. If (21) is satisfied, it can be deemed that an internal ac grounding fault has occurred.

B. DISCRIMINATION OF INTERNAL AND EXTERNAL FAULTS

1) In normal operation or when a dc fault occurs, ac systems are symmetric, so $|3i_0| = 0$.

2) When an ac fault occurs at the grid-side of the transformer, there is no zero-sequence current at the valve-side due to the transformer's delta connection. Moreover, SM capacitors won't discharge in this fault, so $|3i_0| = 0$.

3) When an internal phase-to-phase fault occurs, since the fault point is not grounding, $|3i_0| = 0$.

4) When an internal asymmetric grounding fault occurs, $|3i_0|$ consists of three parts: ac zero-sequence current, capacitor charging current on the upper arm of faulted phases, and capacitor discharging current on the lower arm of faulted phases, which are shown in Fig. 14. Therefore, $|3i_0| > 0$.

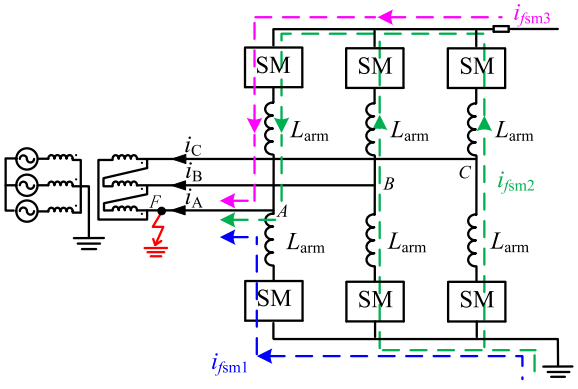

FIGURE 14. Fault current path of a single-phase-to-ground fault.

5) When an internal three-phase-to-ground fault occurs, although there is no current fed by the ac system at the ac-side of MMC, discharging current and charging current of SM capacitors will arise in three-phase ac lines with the same direction, as is shown in Fig. 15. Therefore, $|3i_0|$ is the sum of capacitive current in three phases and $|3i_0| > 0$.

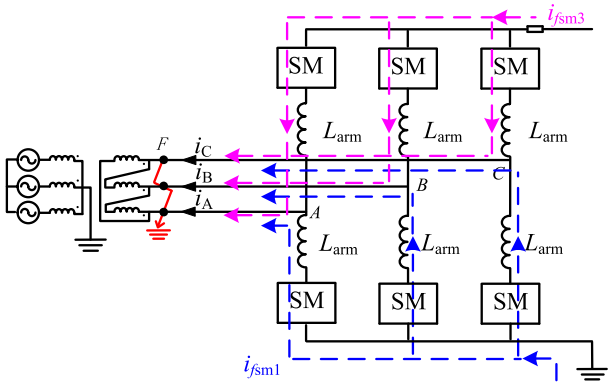

FIGURE 15. Fault current path of a three-phase-to-ground fault.

C. THRESHOLD SETTING AND FAULT RESISTANCE

The threshold should be set suitably to ensure reliability and sensitivity of the protection. According to the analysis above, when an external fault (for instance, a dc fault or a grid-side ac fault) occurs, $|3i_0|$ is theoretically equal to zero. Considering power fluctuation, transforming error of CTs, and precision of devices, some margin should be reserved. As a result, the threshold is set as follows:

$$\Delta_1 = 0.1 I_m \tag{22}$$

where I_m is the amplitude of valve-side ac phase current in normal operation.

According to the analysis in Section IV-B, main components of $|3i_0|$ are capacitive current in faulted phases. In other words, the more faulted phases exist, the larger the value of $|3i_0|$ is. Therefore, the value of $|3i_0|$ in a single-phase-to-ground fault is the smallest among three types of grounding faults. To verify the ability of the protection to endure fault resistances, only a single-phase-to-ground fault needs to be analyzed. If the protection can operate reliably in a single-phase-to-ground fault, it naturally operates well in other grounding faults.

When a single-phase-to-ground fault occurs, (23) can be obtained approximatively if ac zero-sequence current in $|3i_0|$ is ignored.

$$|3i_0| \approx |i_{fsm1} + i_{fsm2} + i_{fsm3}| \tag{23}$$

The calculation methods for i_{fsm1}, i_{fsm2}, and i_{fsm3} are given in Section III. It should be noted that R_1, R_2, and R_3 are replaced by R_1+R_g, R_2+R_g, and R_3+R_g, respectively. R_g represents fault resistance. The fault resistance of 220kV-level ac lines will not be more than 100Ω. Considering that it is a station internal fault, the actual fault resistance will be smaller. The value of fault resistance is setting to 100Ω and the value of $|3i_0|$ obtained by (23) is shown in Fig. 16. At 0.34ms after the fault occurs, the value of $|3i_0|$ reaches 0.2kA, which is equal to Δ_1. Therefore, the protection criterion can rapidly detect station internal ac grounding faults with various fault resistances within 1ms after the fault occurs.

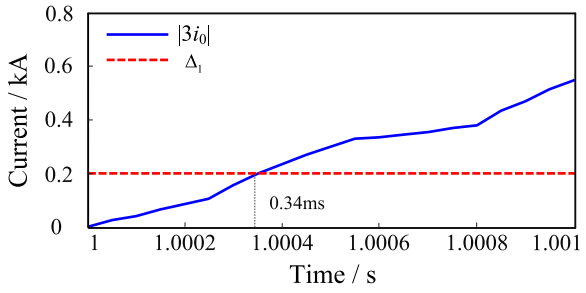

FIGURE 16. Value of $|3i_0|$ ($R_g = 100\ \Omega$).

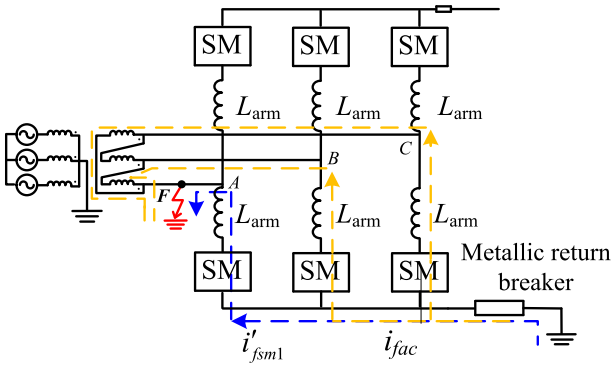

FIGURE 17. Metallic return breaker.

D. FAULT CLEARING STRATEGY

The main damages caused by three types of station internal ac grounding faults are summarized as follows.

1) On-state SM capacitors on the lower arm of faulted phases discharge acutely, resulting in severe overcurrent on the bridge arm. After the MMC is blocked, the current decays slowly due to the large time constant, making diodes withstand overcurrent for a long time.

2) Discharging current of SM capacitors in non-faulted phases will cause severe overcurrent in the fault path and overvoltage on upper arm SM capacitors in faulted phases. After the MMC is blocked, the freewheeling current decays to zero quickly, but lower arms in non-faulted phases will produce large fault current with dc offset, resulting in the grid-side ACCB cannot be tripped.

3) The discharging current of the opposite MMC causes severe overcurrent on dc lines and overvoltage on upper arm capacitors in faulted phases. After the MMC is blocked, the large current begins to feed into non-faulted phases.

This paper develops a clearing strategy which is applied to three types of grounding faults based on the damages above.

When an internal ac grounding fault is detected, the faulted MMC should be immediately blocked to prevent SM capacitors from discharging. At the same time, the dc breaker near the faulted MMC is tripped to cut off the discharging path of the opposite MMC.

After the MMC is blocked, freewheeling current on the lower arm of faulted phases decay slowly. Although diodes are protected by the existing paralleled thyristors, this freewheeling current may result in the thyristors overtemperature and even burn out. In addition, the large current arising on lower arms of non-faulted phases cannot be cleared since the ACCB cannot be tripped. As is shown in Fig. 17, i'_{fsm1} represents the freewheeling current in the faulted phase and i_{ac} is the fault current in non-faulted phases.

A LR parallel circuit is employed to damp the dc component of the fault current and in turn to trip the grid-side ACCB in [21]. But this method will affect the transient operation of the healthy pole and aggravate the overvoltage on the upper arm of phase A. In order to clear these two current above, a dc breaker will be installed on the metallic return in this paper. These two current can be cleared within 3ms after the fault is detected by tripping the metallic return breaker.

After the metallic return breaker is tripped, current decay to zero rapidly and then, the grid-side ACCB can be tripped to ensure safety of the system. Total protection schemes are shown in Fig. 18.

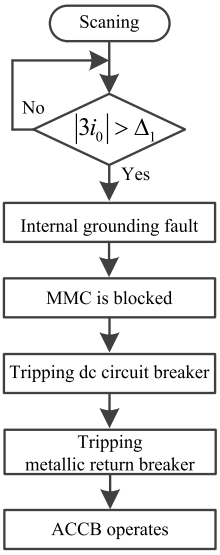

FIGURE 18. Total protection schemes.

V. SIMULATION RESULTS AND ANALYSIS

A. SIMULATION MODE

To verify the correctness of analysis of fault characteristics and proposed protection schemes, a two-terminal bipolar MMC-based HVDC link has been built in PSCAD/EMTDC, as shown in Fig. 19. Station S1 adopts control strategy of constant dc voltage and constant reactive power. Station S2 adopts control strategy of constant power and constant

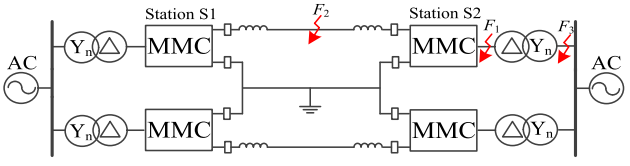

FIGURE 19. Bipolar MMC-based HVDC link.

TABLE 1. Simulation parameters of the test model.

Parameter	Value
DC voltage	±400 kV
AC voltage	230 kV
Transformer ratio	230 / 204
Air core reactance of transformers	0.2 pu
Rated transmission power	1200 MW
Number of SMs per bridge arm	10
Bridge arm inductance	90 mH
IGBT on-state resistance	0.01 Ω
Diode on-state resistance	0.01 Ω
Current limiting reactor	200 mH
SM capacitance	480 μF
Rated parameter of IGBTs	4.5kV / 3kA
Threshold of the overcurrent protection of arms	5.06kA

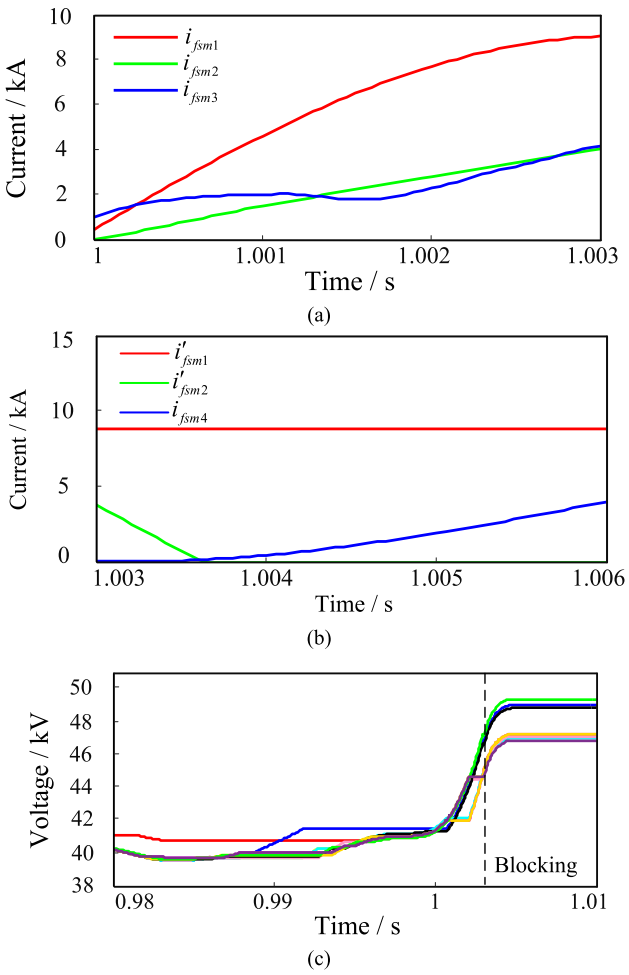

FIGURE 20. Simulation results of fault characteristic analysis (a). pre-blocking discharging current (b). post-blocking discharging current (c). Voltages of SM capacitors on the upper arm of phase A.

reactive power. Specific parameters of the model are listed in Table 1.

B. VERIFICATION OF FAULT CHARACTERISTIC ANALYSIS AND CALCULATION THEORY

A station internal ac singe-phase-to-ground fault is set at t = 1s in phase A of the positive MMC in station S2, shown as F_1 in Fig. 19. The faulted MMC is blocked 3ms after the fault occurs.

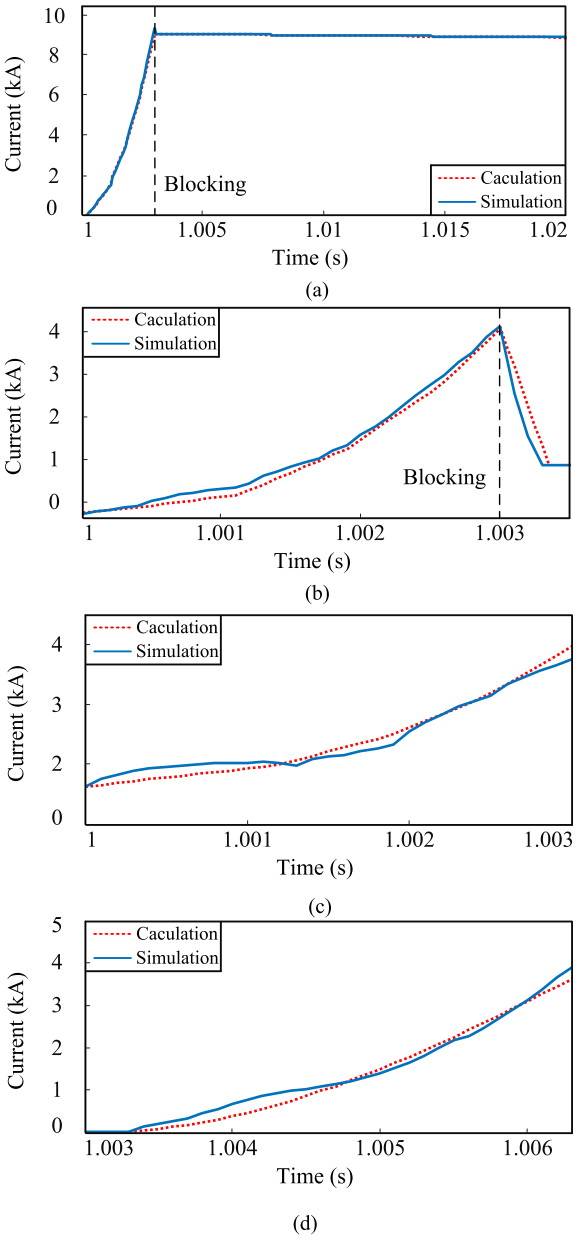

FIGURE 21. Comparison between numerical solutions and simulated values of fault current. (a). Discharging current of lower arm SM capacitors in phase A. (b). Discharging current of upper arm SM capacitors in phase B. (c). Pre-blocking discharging current of the opposite MMC. (d). Post-blocking upper arm charging current in phase B.

Simulation waveforms of three parts of discharging current are shown in Fig. 20. In Fig. 20(a), three parts of discharging current grow continuously before the MMC is blocked. The discharging current of the faulted phase has the fastest growth rate and the largest amplitude, so it is most harmful to the MMC. In Fig. 20(b), when the MMC is blocked, the freewheeling current in the faulted phase decays slowly, which will cause the bridge arm to withstand overcurrent continuously and corresponding measures must be taken.

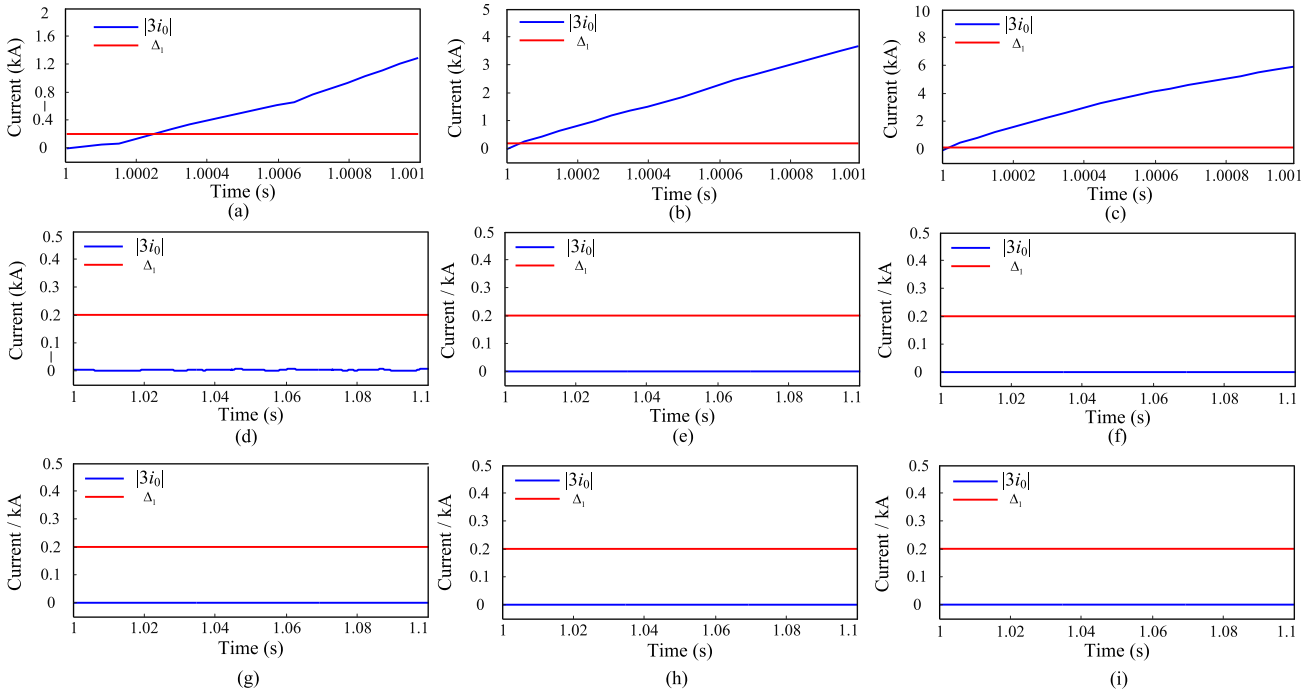

FIGURE 22. Values of $|3i_0|$ in various kinds of faults. (a) F_{1A-G} (b) F_{1BC-G} (c) F_{1ABC-G} (d) F_{1BC} (e) F_{3A-G} (f) F_{3BC} (g) F_{2P-G} (h) F_{2P-P} (i) Normal operation.

The discharging current of the non-faulted phase decays to zero rapidly, so there is no need to take measures to deal with it. The discharging current of the opposite MMC continues to feed into non-faulted phases, which may cause overcurrent. As is shown in Fig. 20(c), on-state SM capacitors on the upper arm of phase A are charged by i_{fsm2} and i_{fsm3} once a fault occurs. After the MMC is blocked, All the SM capacitors on the upper arm of phase A will be charged by dc voltage until the sum of capacitor voltages is equal or higher than dc voltage. Finally, the capacitor voltages reach about 1.2p.u. Therefore, the correctness of analysis of fault characteristics in Section III can be verified here.

The fourth-order Runge-Kutta algorithm is applied to solve the second-order differential equations with variable coefficients in this paper. The comparison between numerical solutions and simulated values is shown in Fig. 21. As we can see from Fig. 21, the calculated value of fault current is basically consistent to simulation results, verifying the correctness of the proposed calculation theory. In Fig. 21(c)-(d), some errors exist between two waveforms because the distributed capacitors on dc lines have been ignored.

C. VERIFICATION OF THE PROTECTION CRITERION

The proposed protection criteria should rapidly detect grounding faults occurring anywhere from the transformer's valve-side leads to the MMC. In Fig. 19, we simulate an internal single-phase-to-ground fault ($F_{1\mathrm{A-G}}$), an internal two-phase-to-ground fault ($F_{1\mathrm{BC-G}}$), an internal three-phase-to-ground fault ($F_{1\mathrm{ABC-G}}$), an internal phase-to-phase fault ($F_{1\mathrm{BC}}$), a grounding fault at the grid-side of the transformer ($F_{3\mathrm{A-G}}$), a phase-to-phase fault at the grid-side of the transformer ($F_{3\mathrm{BC}}$), a dc pole-to-ground fault ($F_{2\mathrm{P-G}}$), a dc pole-to-pole fault ($F_{2\mathrm{P-P}}$) and the normal operation. Values of $|3i_0|$ in various kinds of faults are shown in Fig. 22, where Δ_1 equals to 0.2 kA. It can be seen from Fig. 22(a)-(c) that 1ms after the fault occurs, the value of $|3i_0|$ becomes much larger than Δ_1 in any internal grounding fault, so the protection has operated reliably. When the system operates normally or other faults occur, the value of $|3i_0|$ fluctuates around zero and is less than Δ_1 all the while, as is shown in Fig. 22(d)-(i), so the protection will not operate. Therefore, the protection criterion can reliably and rapidly determine whether the fault is internal or external.

When a dc fault occurs in a MMC-based multi-terminal HVDC grid, $|3i_0|$ cannot be detected in any converter station, so the protection will not operate. When an internal grounding fault occurs in a converter station, $|3i_0|$ cannot be detected in other converter stations. The protection operates only when a grounding fault occurs in the converter station where the protection is equipped. Therefore, the proposed protection is not only applicable to MMC-based HVDC transmission systems, but also to MMC-based multi-terminal HVDC grids.

D. VERIFICATION OF FAULT RESISTANCE

Based on the analysis in Section IV-C, Fault resistance ranging from 0 Ω to 100 Ω is selected to verify the ability of the protection to endure fault resistance and simulated results are shown in Fig. 23.

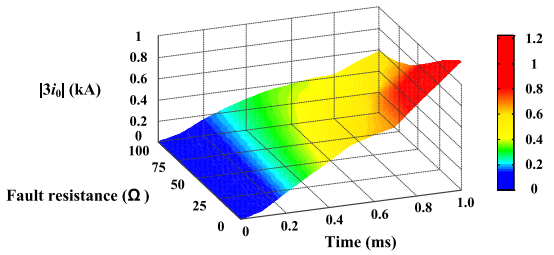

FIGURE 23. $|3i_0|$ in a single-phase-to-ground fault with different fault resistances.

When the fault resistance becomes 100 Ω and 0.3ms after the fault occurs, the value of $|3i_0|$ reaches 0.2 kA, which is equal to Δ_1. The theoretical operating time is 0.34ms in Section IV-C, which is in good agreement with the simulated value. Therefore, both theoretical analysis and simulation have verified that the protection criterion can rapidly detect station internal ac grounding faults with various fault resistances within 1ms after the fault occurs.

E. COOPERATION BETWEEN THE OVERCURRENT PROTECTION OF ARMS AND THE PROPOSED PROTECTION

For station internal ac-line protected zone, the proposed protection is employed as the main protection and the overcurrent protection of arms is used as the backup protection. Therefore, the proposed protection must operate before the overcurrent protection of arms when an internal ac grounding fault occurs.

The setting principle of the overcurrent protection of arms is shown in [27] and the threshold can be obtained as follows.

$$\Delta_2 = i_{block} - i_{m\arg in} - \frac{U_{dc.\max}}{2L_{arm}} t_{delay} \tag{24}$$

i_{block} represents the IGBT's maximum blocking current, which equals to twice the rated value. t_{delay} is the total time delay of measurement and execution of the protection. $U_{\text{dc.max}}$ is the largest steady-state dc voltage.

In the simulation, the rated value of an IGBT is 4.5KV/3kA and Δ_2 is set to 5.06kA, which is obtained by (24). As is shown in Fig. 24, when an internal metallic grounding fault occurs, the overcurrent protection of arms operates at 3.08ms after the fault while the proposed protection operates at 0.24ms after the fault. When a grounding fault occurs with different fault resistance, corresponding operating time of two protections is given in Table 2. It can be seen that the proposed protection can always operate before the overcurrent protection. Therefore, when a station internal ac grounding fault occurs, the overcurrent protection of arms and the proposed protection cooperate very well.

F. VERIFICATION OF THE FAULT CLEARING STRATEGY

To verify validity of the fault clearing strategy, A station internal single-phase-to-ground fault is set at t = 1s in phase A of the positive MMC in station S2, shown as F_1 in Fig. 19. The fault resistance is set to be 0.1Ω. When the value of $|3i_0|$

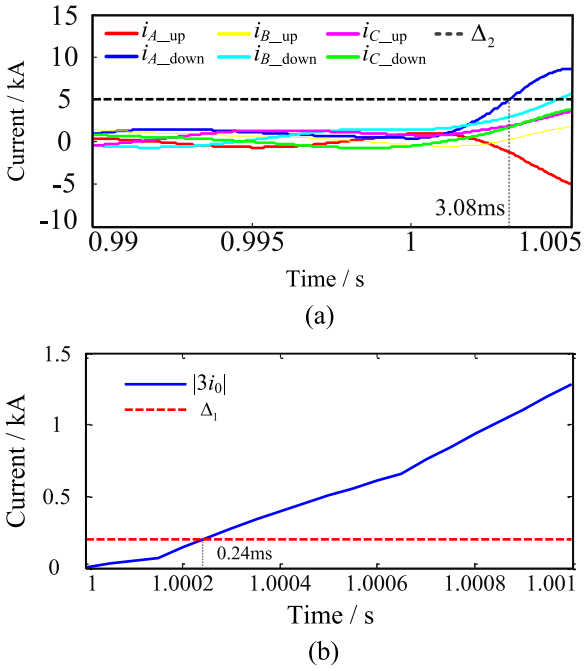

FIGURE 24. Operating time of two protections in a single-phase-to-ground fault without fault resistance. (a) Operating time of the overcurrent protection of arms. (b) Operating time of the proposed protection.

TABLE 2. Operating time of two protections.

fault resistance (Ω)	Operating time of the overcurrent protection (ms)	Operating time of the proposed protection (ms)
0	3.08	0.24
25	9.29	0.25
50	13.42	0.27
75	61.82	0.29
100	101.63	0.30

reaches to Δ_1, the proposed protection operates immediately. At the same time, the control system sends blocking and tripping signals to the MMC and breakers, respectively. After 3ms, the dc breaker and metallic return breaker are tripped and the fault is cleared completely.

Fig. 25 illustrates arm current in phase A when the clearing strategy is employed. The MMC is blocked once the

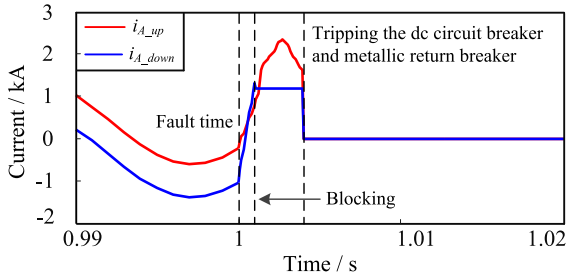

FIGURE 25. Arm current in phase A.

protection operates, suppressing the growth of lower arm current i_{A_down}. After that, i_{A_down} decays slowly and SM capacitors on the upper arm continue to be charged. The dc breaker and metallic return breaker are tripped 3ms after the protection operates and fault current of all arms decay to zero rapidly.

Fig. 26 illustrates the impact of the clearing strategy on non-faulted phases by taking phase C as an example. After the MMC is blocked, arm current i_{C_up} and i_{C_down} decay to zero quickly. Neither the discharging current from the opposite MMC nor the fault current with dc offset appears in phase C, because (14) is never satisfied before two breakers are tripped.

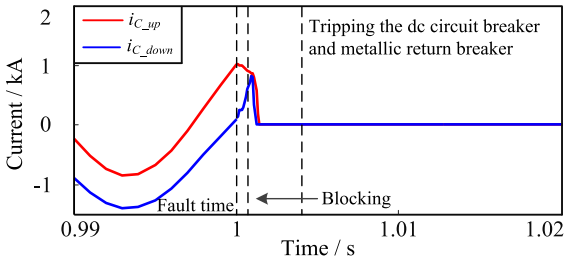

FIGURE 26. Arm current in phase C.

It can be seen from Fig. 27 that the proposed clearing strategy has a significant effect on suppressing overvoltage of the capacitors on the upper arm of phase A. The increase of i_{fsm2} and i_{fsm3} is suppressed by blocking the MMC, so that the capacitor voltages don't increase obviously. After that, all the SM capacitors on the upper arm of phase A will be charged by dc voltage, but this process is slow and discontinuous. The breakers are tripped at 3ms after the fault is detected, ensuring the overvoltage can be controlled at a lower level (about 1.04p.u.).

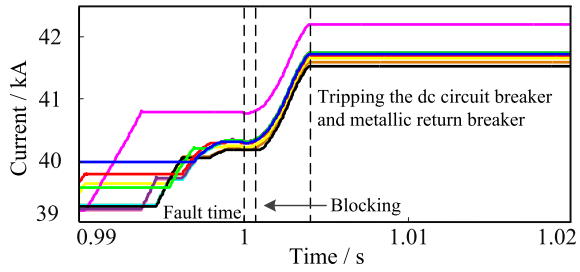

FIGURE 27. Voltages of SM capacitors on the upper arm of phase A.

The impact of the proposed clearing strategy on the voltage of the healthy pole is shown in Fig. 28. The metallic return breaker can clear fault currents at 3ms after the fault is detected. Since the breaker operates extremely fast, the impact on the healthy pole is very small.

As is shown in Fig. 29, after the dc breaker and metallic return breaker are tripped, grid-side ac phase current decays to zero rapidly and in turn, the grid-side ACCB can be tripped to ensure safety of the system.

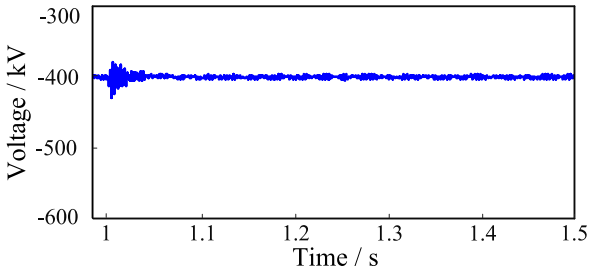

FIGURE 28. Impact on the voltage of the healthy pole.

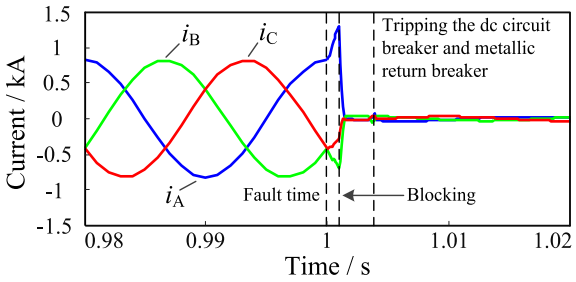

FIGURE 29. Grid-side ac current.

VI. CONCLUSION

In this paper, a single-phase-to-ground fault is taken as an example to investigate transient characteristics of station internal ac grounding faults in the symmetrical bipolar MMC-HVDC system. We proposed a calculation theory of fault current which is based on the improved RLC model and second-order differential equation with variable coefficients. A transient zero-mode current-based protection criterion is developed as the main protection for station internal ac-line protected zone and corresponding clearing strategy is designed. According to the practice above, the following conclusions are obtained.

1) Overcurrent and overvoltage caused by discharging current of SM capacitors are main characteristics of a station internal ac grounding fault. Discharging current includes discharging current of SM capacitors on the lower arm of faulted phases, discharging current of SM capacitors in non-faulted phases and discharging current of the opposite MMC.

2) The calculation theory of fault current based on the improved RLC model and second-order differential equation with variable coefficients is applicable and accurate. It can be used to accurately calculate the discharging current of a single bridge arm and the discharging current between several bridge arms.

3) Transient zero-mode current-based protection criterion can operate accurately within 1ms after the fault occurs with better quickness, reliability and ability to endure fault resistance.

4) For station internal ac-line protected zone, the proposed protection can be employed as the main protection and the overcurrent protection of arms is used as the backup protection. Two protections cooperate well and prevent internal ac grounding faults from doing harm to MMC together.

5) The proposed fault clearing strategy are applicable to three types of station internal ac grounding faults, which

can clear the fault completely within 3ms after the fault is detected.

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