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Adaptive Carrier-Based PDPWM Control for Modular Multilevel Converter With Fault-Tolerant Capability

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ABSTRACT Modular multilevel converters (MMCs) are considered very promising converters due to their modularity structure and high reliability from fault-tolerant. A fault within a submodule (SM) is one of the main issues in half-bridge MMCs with substantial switching devices. In this paper, an adaptive carrier based phase disposition pulse width modulation (PDPWM) technique for MMCs, which uses only one carrier having flexibility with fault-tolerant capability, is presented. The energy-based control is also used in this study to regulate the balancing of SMs during and after a fault. In order to investigate the performance of the proposed method, a laboratory single-phase MMC prototype has been built by using four SMs to generate nine-level. The single-phase MMC prototype is tested by assuming one of the SMs in the failure condition. The result revealed that the proposed method had been successfully applied to the MMC prototype to control the upper and lower arm during the failure. In addition, the reference command will correct the fault according to the adaptive carrier and the computational burden is lesser since it only uses one single carrier.

INDEX TERMS Modular multilevel converter (MMC), multilevel inverter, fault-tolerant, modulation technique, and reliability.

NOMENCLATURE

P_{c_u}	Upper arm instantaneous power
P_{c_l}	Lower arm instantaneous power
V_{cap}	Submodule / capacitor voltage
I_{SM}	Upper / lower arm current
V_c	Internal voltage
V_{out}	Output voltage
I_{out}	Output current
I_{circ}	Circulating current
I_{SM}	Arm currents
$W_{c\_u}^{\Sigma}(t)$	Upper energy arm
$W_{c\_l}^{\Sigma}(t)$	Lower energy arm
$W_c^{\Sigma}(t)$	Total input energy supplied
$W_c^{\Delta}(t)$	Difference energy supplied
V_u'	Upper voltage reference
V_l'	Lower voltage reference
$V_{command}^*$	Voltage reference
V_c^*	Internal voltage reference
I_{SM}	Arm currents
$\sum V_{c\_upper\_i}$	Total sum of the upper SM voltage
$\sum V_{c\_lower\_i}$	Total sum of the lower SM voltage
N_{fault}	Number of faulty SM per arm
N_{total}	Number of SM per arm

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I. INTRODUCTION

At present, MMCs have become a highly attractive topology due to their various advantages, such as remarkable advancement in designing hierarchical scheme, easy to balance

voltage capacitor, scalability to various voltage and/or power levels, and great potential in medium-voltage and high-power applications, especially in HVDC system [1]–[4]. This modularity or hierarchical structure can be very much useful, in order to decrease production cost, increase the number of levels, and redundancy ability.

Various MMC modulation strategies have been reported in the literature [5]–[8]. Selective harmonic elimination (SHE) is a low switching frequency modulation based on harmonic elimination theory, which can generate particularly less THD compared to other techniques. In consequence, increasing the voltage level will result in a complex calculation for SHE. The modulation method of carrier phase-shifted PWM (CPS-PWM) and phase disposition PWM (PDPWM) techniques were discussed in [9], [10]. The CPS-PWM distributes an equal amount of power among the SMs, resulting in the inner current control and voltage of capacitors that may reach steady-state at a satisfactory level fastly [11]. However, this method cannot obtain the closest level PWM, which results in worse harmonic performance compared with the PDPWM strategy. In [12], an improved PDPWM strategy is presented by using a single carrier modulation technique that exhibits an excellent harmonic characteristic as the conventional PDPWM. However, this method needs to change the reference waveform.

MMCs require considerable SMs for increasing voltage levels. Therefore, some faults can occur internally within an SM. If a faulty SM exists, then the converter should be able to detect the fault and continue transferring the power to guarantee the converter reliability [13]–[17]. The unbalanced SM voltages of arms and loss of some part of the voltage level occur during SM failure. To overcome this circumstance, few SM redundancy strategies have been proposed in [18]–[22] to solve faulty SM. All these strategies have been reviewed in [23]. There are two approaches to overcome the failure of SM; First, when the submodule is operating normally, the redundant SM is placed in the converter as the backup SM to replace the damaged SM for keeping the system symmetrical. Second, redundant SM is placed and operated at the same time, when an SM fails, only the faulty SM is skipped, and the other SM does not change and can work symmetrically or asymmetrically.

Most of these strategies use CPS-PWM, PDPWM and nearest level modulation (NLM). In CPS-PWM technique, each of SM needs multiple carrier waves, which is phase shifted from the other SM carriers and needs to resample or re-adjust the phase of all the carriers if SM failure occurs. In [19] and [26] the NLM technique is used to control the converter which creates high fluctuation on capacitors voltage for this technique. The authors in [24], [25] present way for fault-tolerance without having reserved SM and without worrying about the tolerance of the component. This strategy requires to inject zero-sequence voltage to change the waveform of the reference signal. However, the calculation of the required zero-sequence voltages is quite difficult. The strategy presented in [25], uses virtual loop mapping to distribute the pulses, which is also quite difficult to implement.

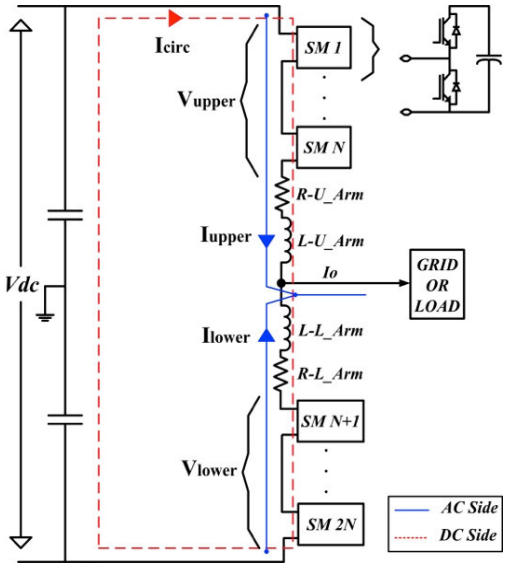

FIGURE 1. Schematic of single-phase MMC.

In this paper, an adaptive carrier PDPWM method based on the centralized capacitor voltage balancing is presented. This method has the following features, only one voltage reference and one carrier are needed for each arm, thereby considerably decreasing computational burden requirement compared to the CPS-PWM and conventional PDPWM. The adaptive carrier PDPWM is able to continue the operation of MMCs and react fastly when certain SM failure. The general energy-based control of MMC system is used in this work due to its excellent expandability [26], [27]. A prototype of MMC has been built to effectively investigate the proposed method and performance of energy-based control during the fault.

The rest of this paper is arranged as follows. Section II presents the principle operation and control structure of the MMC system. Section III presents the improved modulation strategy that has fault-tolerance on a specific SM. The experimental results are presented in Sections IV. Finally, Sections V concludes the study.

II. MATHEMATICAL MODEL AND CONTROL STRUCTURE

A. WORKING PRINCIPLE OF MMC

Fig. 1 illustrates the single-phase MMC structure. The main property of MMC is the cascaded connection of a large number of SMs or power cells. SM models, such as half-bridge, full-bridge, and clamp double SM, have been introduced in the literature. A half-bridge SM, which only consists of two switches working complementary and a power capacitor, is selected. The converter is formed by N SMs, wherein half of them are placed in the upper arm and the other half on the lower arm.

Fig. 2 shows the current flow through the SM during different modes of operation. An SM has two conditions of voltage,

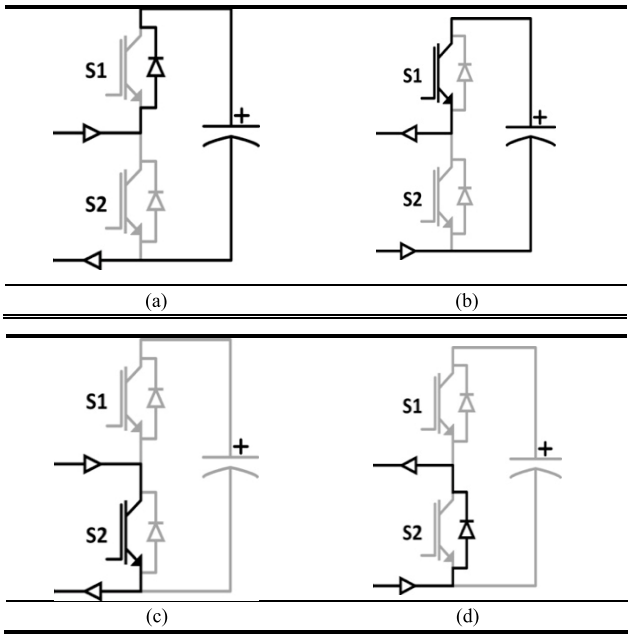

FIGURE 2. Current flow in SM; (a) MODE I: Charging, (b) MODE II: Discharging, (c) MODE III: Unchanged, (d) MODE III: Unchanged.

which are V_{cap} and zero depending on the state of each SM (i.e., ''Inserted'' and ''Bypassed'', respectively). The capacitor will be charged or discharged during the inserted and, according to the direction of the arm current (I_{SM}). When both switches are OFF, the capacitor will work on MODE I, as shown in Fig. 2(a). This mode is used to charge all capacitors to half of the desired voltage. Specifically, this mode only works when $I_{SM} > 0$ for uncontrolled charging purposes. In addition, two inductors are placed in each arm to compensate the voltage imbalance between the upper and lower voltages.

The MMC scheme can be simplified into AC and DC sides. The output AC voltage is the difference between the lower and upper arm voltages. The operation principle of the MMC is to control the upper and lower arm voltages of the sinusoidal with a DC offset up to half of the DC link voltage with an opposite phase of 180°. In this way, The DC side voltage controls the AC side phase voltage as a sinusoidal with the magnitude of up to half of the DC link.

The structure of the MMC with a cascaded SM string can react as a fairly ideal voltage source within the boundaries specified by a series of capacitor voltages. Thus, the power exchange among the SMs must be considered. The power flow should be balanced over time (i.e., at the terminal, the power transfer is not always constant) among the arms. The stored energy among the arms can also be calculated by integrating the power delivered into the upper arm (P_{c_u}) and lower arm (P_{c_l}), which can be expressed in (1) and (2).

$$\frac{dW_u}{dt} = P_{c\_u} = (V_c - V_{out})\left(\frac{I_{out}}{2} + I_{circ}\right). \quad (1)$$

$$\frac{dW_l}{dt} = P_{c\_l} = (V_c + V_{out})\left(-\frac{I_{out}}{2} + I_{circ}\right). \quad (2)$$

The sum of capacitors' voltage in the upper and lower arms of SM series is crucial to be controlled. As mentioned before, when the sum of capacitors' voltage of SM series in the upper or lower arms is equal to the DC input voltage and divided equally among them, the system will be fairly ideal in AC voltage with magnitude half of the DC input voltage. Therefore, the sum of the upper ($W^{\Sigma}_{c\_u}(t)$) and lower ($W^{\Sigma}_{c\_l}(t)$) arm's energy is set equal to the input energy supplied from the DC input side ($W^{\Sigma}_{c}(t)$), which can be expressed in (3). The imbalance between the arms can be sensed by subtracting the lower arm's energy from the upper arm's energy. In an ideal situation, the difference energy supplied ($W^{\Delta}_{c}(t)$) should be zero, thereby ensuring balanced energy among the arms, as expressed in (4).

$$W^{\Sigma}_{c}(t) = W^{\Sigma}_{c\_u}(t) + W^{\Sigma}_{c\_l}(t). \quad (3)$$

$$W^{\Delta}_{c}(t) = W^{\Sigma}_{c\_u}(t) - W^{\Sigma}_{c\_l}(t). \quad (4)$$

Expression (3) and (4) give dynamic relation involving the balancing of the individual SMs capacitor voltages within the string. The capacitor voltage slightly varies between the SMs given that all the SMs are not inserted or bypassed simultaneously. The controller locally regulates each arm to keep the individual capacitor voltage between the upper and lower arms identical.

B. MODEL OF CONTROLLER STRUCTURE OF MMC

In this works, MMC control based on the centralized method is used to achieve voltage balancing by selecting particular SMs for specific switching states depending on the capacitor voltage, current arm direction (i_u and i_l), and the number of SMs under the ON state. The overall DC side control structure of the MMC operating as an inverter is presented in Fig. 3. The outer loop controller (Fig. 3(a)) consists of $W^{\Sigma}_{c}(t)$ and $W^{\Delta}_{c}(t)$ controllers, having a function to control all the SMs capacitors' voltage according to its reference (V_{DC}), wherein the circulating current reference (I^{*}_{circ}) is being the output. Then, the circulating current through the sum of arms currents is regulated by the inner circulating current control loop to regulate the internal voltage of the converter leg.

The total and differential energy controllers are designed by using proportional-integral (PI) controllers, where the sum of the SMs capacitors' voltage applies a low pass filter (LPF) with 50 Hz and 100 Hz cut-off frequencies. In addition, the circulating current controller uses a proportional-resonant (PR) controller, in which the feedback of the circulating current is calculated by summing up the upper and lower arm currents. This control strategy is used due to its capability to reduce the negative sequence current control compared to the synchronous reference frame d-q theory. Moreover, this method is also convenient for a single-phase converter and is stable because phase-locked-loop (PLL) is not used. Generally, different forms of closed-loop controls are required to maintain the capacitor voltage balance at the desired set point over time.

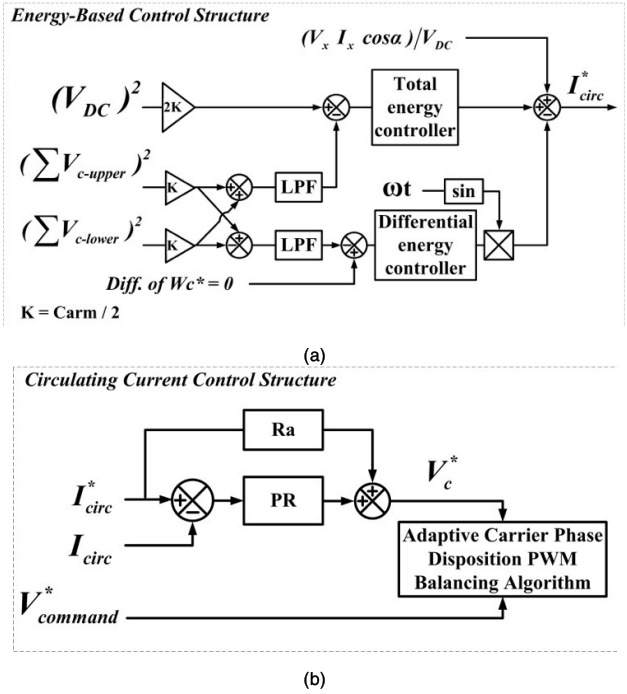

FIGURE 3. Overall DC side control structure; (a). Energy-based control structure, (b). Circulating current control structure.

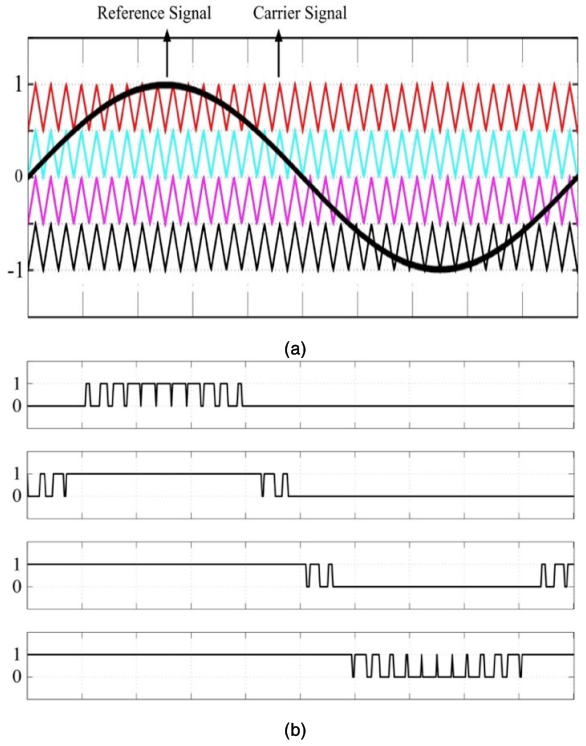

FIGURE 4. Conventional PDPWM; (a) a single reference and four carriers. (b) Direct pulse distribution.

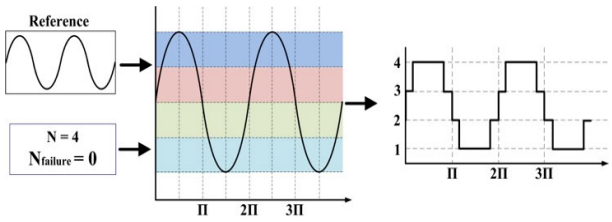

FIGURE 5. Illustration of staircase generation.

III. IMPROVE PHASE DISPOSITION PWM METHOD

A. ADAPTIVE CARRIER BASED PDPWM METHOD

MMCs have interesting modulation control methods. Based on the mathematical model of MMC, the output voltage is controlled by the upper and lower arm references, which can be expressed in (5) and (6).

$$V'_u = \frac{V^*_c}{2} - V^*_{command}. \tag{5}$$

$$V'_l = \frac{V^*_c}{2} + V^*_{command}. \tag{6}$$

The reference signals of the upper arm (V_u) and lower arm (V_l) have a 180° phase shift. In the PWM technique, the reference signals are compared with a specified carrier to generate pulses, which are sent to SMs. The MMC can generate two types of voltage levels, which are $N + 1$ or $2N + 1$ level [11]. The difference of 180° phase shift between the upper and lower arms provide independent pulses to the upper and lower arm SMs, which generates an output of $2N + 1$ levels. Moreover, when the carriers are interleaved, the pulses for the upper and lower arms will be dependent which generates an output of $N + 1$ levels.The required voltage output waveform can be synthesized from different combinations of the SM switching states. Therefore, a proper PWM strategy is needed to determine the SM state and achieve an appropriate power quality.

The PDPWM is a type of level-shifted carrier methods that have been greatly used for multilevel converters. PDPWMs use one voltage reference and some carriers that are stacked on top of each other, thereby dividing the available voltage range among them, as shown in Fig. 4(a). After generating the pulses, the pulses are distributed to all the SMs. The power flow from/into the SMs slightly varies if the pulses are directly assigned to the N-th SM, as shown in Fig. 4(b) [28].

An ascending-sorting algorithm is used in this study. Then, the ON-, OFF-, and PWM-state are provided by the next algorithm, which gives the commands to distribute the pulses among the SMs. Fig. 5 shows that the command signal is divided into 4 regions, which refer to the number of SMs used in this work. Hence, a staircase signal is generated due to an intersection between the command signal and four defined areas. Thus the staircase signal will follow the time and frequency of the command signal. The staircase waveform is needed to determine the number of SM that should be ON and OFF in each arm.

PDPWM methods have the same phase angle and different level offsets. Logically, only one carrier and one voltage reference are necessary for each arm. This study uses only

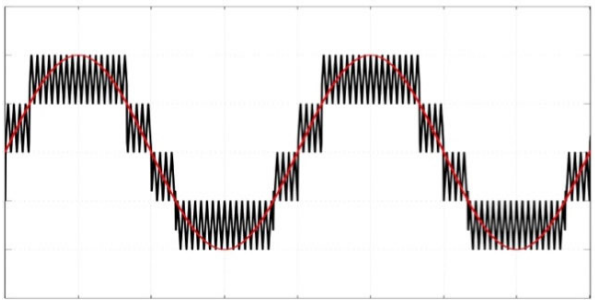

FIGURE 6. Waveform of the reference signal and the adaptive carrier.

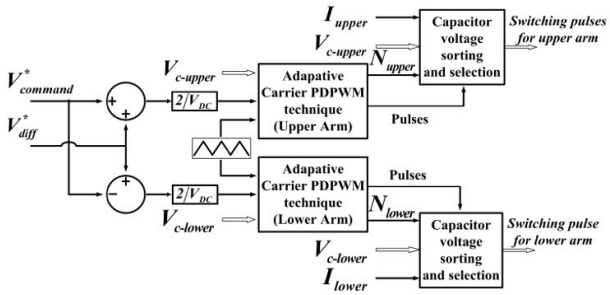

FIGURE 7. Proposed PWM block diagram.

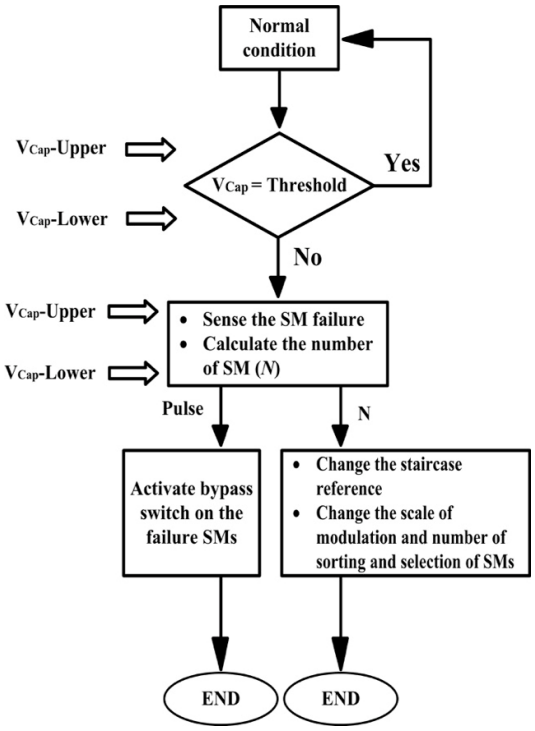

FIGURE 8. Flowchart of the fault tolerant action.

one carrier signal that can be programmed easily and more flexible carrier signal than conventional ones. In this method, the staircase waveform is used to arrange the carrier in accordance with the upper and lower reference signals. Thus, this approach can be called the adaptive carrier, as shown in Fig. 6. The generated pulses will be distributed to all SMs by following ON-, OFF-, and PWM-state. Moreover, if an SM get failure or under maintenance, this method can respond immediately by changing the scale of the carrier waveform. Fig. 7 shows the overall PWM block diagram for the MMC.

B. FAULT-TOLERANT ABILITY

According to the parameters in Table 1, the MMC generates nine-level voltages in normal conditions. The arms voltage consists of five output voltage levels each other. Assume that SM number 4 (SM#4) in the lower arm in the phase malfunctions. Then, the sensor will detect the abnormal SM, and the faulty SM#4 is bypassed. Thus, the output voltage of SM#4 is expressed as follows:

$$SM_{\#4\_lower} = 0.$$

The total number of the SMs (N) is four, but when the SM#4 is bypassed, the number of SMs that can be inserted is limited to three. Therefore, the faulty SM in the phase can generate three-pole voltage levels (i.e., $+V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$, except $+V_{dc}/2$).

The above condition can cause an imbalance among the capacitor voltages. This study uses the scenario; when an upper arm SM fails, a lower arm SM is removed to maintain the arm voltage symmetry. One of the other SMs at the other arm should also be in a bypassed mode, even in a healthy condition, to balance the capacitor voltage among the arms.

When the faulty SMs are applied bypassed mode, the rest of the healthy SMs tend to rise. The percentage of the increment can be calculated by (7). This percentage needs to be considered for selecting the rating of capacitor and IGBT during the fault. The sensing the faulty SM can be sense by giving threshold to the whole of SMs.

$$Tolerance(\%) = \frac{N_{fault}}{N_{total} - N_{fault}} x100\%. \tag{7}$$

Fig. 8 shows a simplified flowchart that illustrates a fault occurring among the SMs. The sensors provide a fault signal to the controller. Here, SM#4 in the lower arm is assumed to have a malfunctioned operation. The controllers sense the failure and start to deactivate SM#4 in the lower arm. The other SM in the upper arm is also placed in an OFF state (deactivated). The new staircase signal will be generated according to the failure signal, as shown in Fig. 9. The new number of SM ($N = 3$) is obtained after sensing the failure signal, and the converter automatically works $N = 3$.

IV. HARDWARE IMPLEMENTATION

A. NORMAL OPERATION

The single-phase MMC prototype inverter with inductive loads is built and tested to validate the proposed method, as shown in Fig. 10. The parameters used in the experiment are listed in Table 1. The control and modulation techniques are programmed in a Speedgoat real-time target machine. The proposed method is designed in MATLAB/Simulink

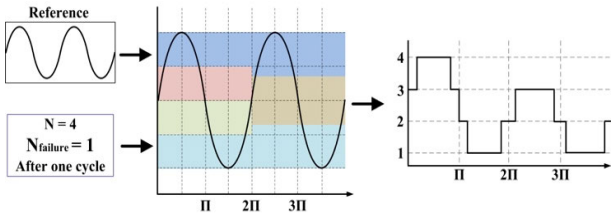

FIGURE 9. Illustration of staircase reaction when a fault occurs.

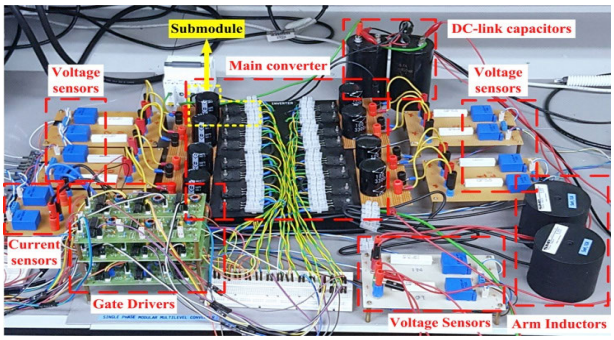

FIGURE 10. Experimental setup.

TABLE 1. The parameter of single phase MMC under experimental validation.

Items	Value
Fundamental Frequency	50 Hz
DC-Link Voltage	200 V
Arm Inductance	5 mH
Arm Equivalent Resistance	0.2 Ω
SM Capacitor	3300 μF
Number of SM in each arm (N)	4
Switching Frequency	2.5 kHz
Modulation Index	0.9

platform. PI controllers are used for energy-based control. Then, PR controllers are used for inner-loop circulating-current control.

The output voltage (nine-level) and current waveform in normal conditions with an inductive load are shown in Fig. 11, wherein all the capacitor voltages are well balanced at 50 V with a particularly small ripple as shown in Fig. 12. The fluctuation of the capacitor voltages is not clearly shown in the oscilloscope due to the high capacitance being used in the hardware setup. The experimental results show a good performance of the proposed control for MMC in inverter mode.

B. FAULT OPERATION – BYPASSED THE FAULT SM

A fault signal from SM#4 at the lower arm is programmed in the system to evaluate the balancing control and proposed fault tolerance. The output voltage, current, and recharge capacitor voltages during the fault are shown in Fig. 13. The system detects the fault signal from SM#4 at the lower arm,

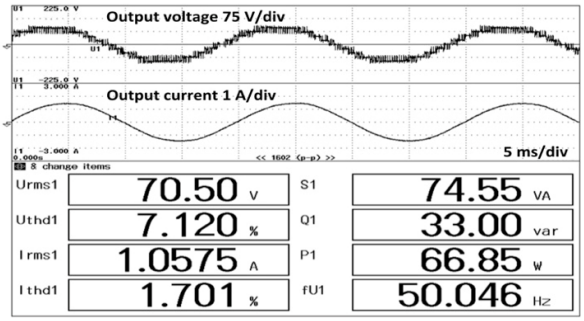

FIGURE 11. Output voltage of nine-level and output current under normal state form measured by a power analyzer.

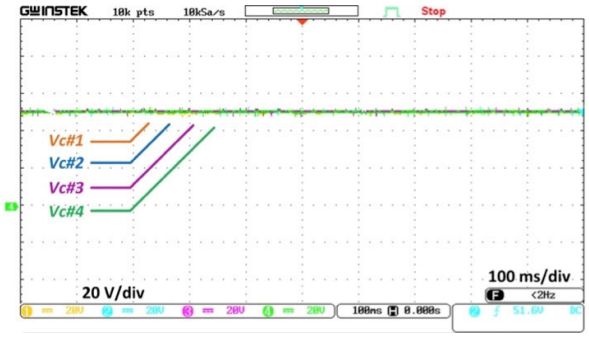

FIGURE 12. Lower arm capacitor voltage under normal condition.

TABLE 2. Tolerance of redundancy.

No of SM fault	N = 4	N = 5	N = 15	N = 44, [15]
	Tolerance	*Tolerance*	*Tolerance*	*Tolerance*
1	33.33%	25%	7.14%	2.32%
2	100%	66.67%	15.38%	4.76%

and the algorithm calculates the new number of SMs (N). Subsequently, the SM#4 at the lower arm and the other SMs in the upper arm are bypassed. The new scale modulation signal is activated. Then, the remaining SMs are recharged at the new desired voltage ($V_{dc}/N; N = 3$) by energy-based control. The output level immediately becomes seven-level. The voltage output waveform eventually becomes normal after one cycle.

From the experimental result in Fig. 13(b), the healthy SMs voltages increase by 33.3% from the normal condition. This increase should be taken into consideration when designing the converter to set the limit of converter tolerance. The number of SMs changes the percentage of tolerance of components. For a larger number of SM, this tolerance can be decreased significantly as calculated in Table 2. The percentage of tolerance for redundancy can be calculated using (7).

C. FAULT OPERATION – RE-INSERT THE SM

Fig. 14 shows the performance of the converter after clearing the fault, wherein SM#4 is re-inserted. The capacitor

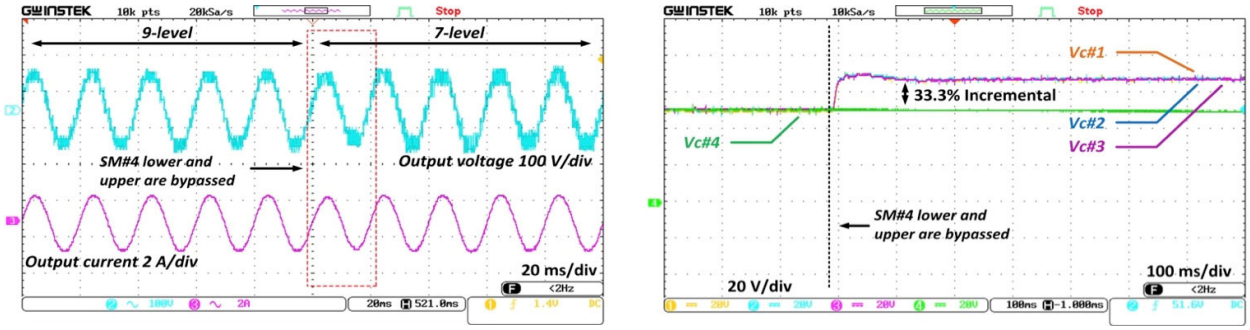

FIGURE 13. During SM#4 failure; (a) Output voltage and current waveforms, (b) SM capacitor voltages waveforms at the lower arm.

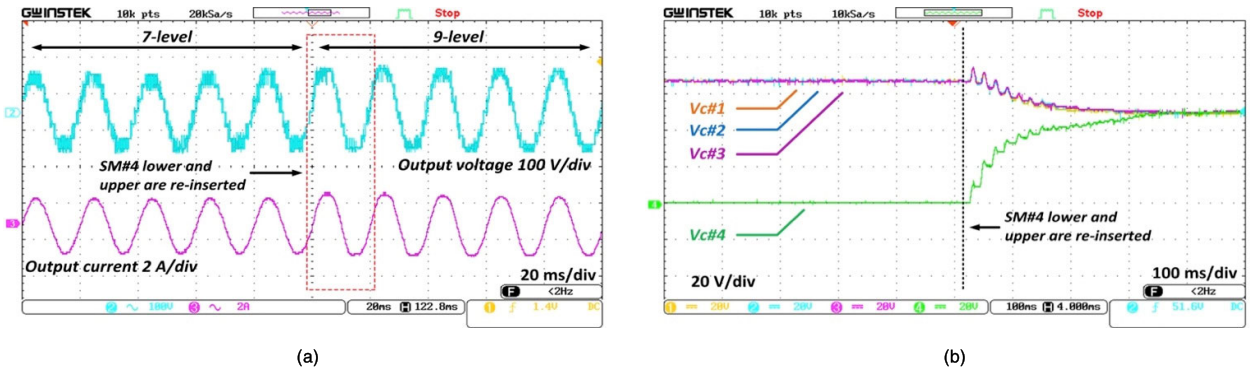

FIGURE 14. During SM#4 re-inserted; (a) Output voltage and current waveforms, (b) SM capacitor voltages waveforms at the lower arm.

voltage in SM#4 is rebalanced, and the other capacitor voltages are automatically re-adjusted to the same voltages ($V_{dc}/N; N = 4$) as shown in Fig 14(b). The whole capacitor voltages return to 50 V from 66.65 V.

Fig. 15 shows the influence of the recharge capacitor voltages to the newly desired voltage on the circulating current. This phenomenon occurs due to the DC side needs to inject current for energizing the remaining capacitors that are controlled by the energy-based controller. Fig. 16 shows the phenomena of circulating current when the SM#4 at the lower arm is activated. The re-inserting of SM#4 leads to the fluctuation of the upper and lower currents in a short time due to the voltage difference between SM#4 at the lower and the other healthy SMs. The peak of the fluctuation current will be diminished for a large number of SMs and also can be minimized by using cold-reserved submodule proposed by [29]. The energy-based controller is used to minimize the oscillation and regulate the imbalance condition among the SMs. Moreover, charging the SM externally to the desired voltage before inserting to the arm also can reduce this fluctuation. This condition occurs because the input voltage is equally divided on the number of SMs.

Fig. 17 and Fig. 18 show the simulation result of the behavior of the adaptive carrier of PDPWM during the transition from normal condition to faulty SM condition, where the waveform of the adaptive carrier of PDPWM is influenced by the change of the staircase signal. Moreover, Fig. 17 shows the change of the adaptive carrier during normal conditions to bypass (failure of SM#4) mode. Fig. 18 shows the transition from bypassed mode of SM#4 to the normal mode by re-inserting SM#4. Thus, the proposed technique does not interrupt the upper and lower arm reference signals, where the reference signals are adapted with the change of the carrier. So, The amount of power shared between upper and lower arm are equal.

A comparison between what has been presented in the literature and the proposed method, which involves a broad range of features, is presented in Table 3. There are three main strategies to overcome the failure of SM, which are reserved / spare redundant SM, redundancy tolerance on SM, and without redundant SMs. Reserved SMs require extra spare SM, which used when the fault happens. However, reserved SM will cause an increase in the volume and cost of the converter. Redundancy tolerance on SM is suitable for large number of SMs where the increasing number of SM will reduce the tolerance percentage of redundancy. In [24], the authors proposed fault-tolerant without redundant SM, where it will not increase the cost and volume of the converter. However, this method negates the pulses for the failure SM by injecting zero-sequence or change the direction of pulses in order to keep the capacitor voltages remain the same. Consequently, this method has low performance on the output side.

TABLE 3. Comparison of fault-tolerant under SM failure.

Method	Reserved Redundant SM	Redundancy Tolerance	Modulation Technique	Performance on the fault	Computational burden	Hardware Cost
Proposed by [22], [23]	No	Yes	CPS-PWM	High	High	Low (for large No. of SM)
Proposed by [19], [20]	Yes	No	NLM	High	High	High
Proposed by [17]	No	Yes	CPS-PWM	High	High	Low (for large No. of SM)
Proposed by [24]	No	No	CPS-PWM	Low	High	Low
Proposed by [25]	No	No	CPDPWM	Medium	High	Low
Proposed by [30]	No	Yes	PDPWM	High	High	Low (for large No. of SM)
Proposed Method	**No**	**Yes**	**Adaptive Carrier PDPWM**	**High**	**Low**	**Low (for large No. of SM)**

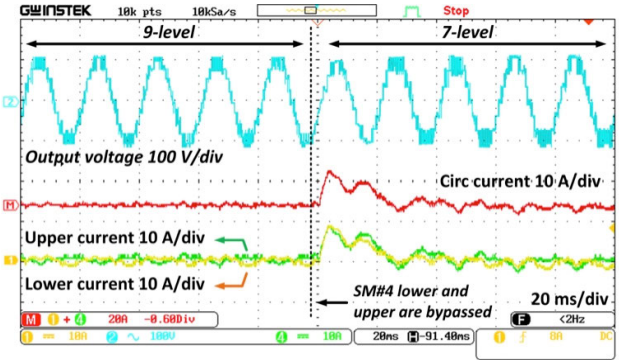

FIGURE 15. Output voltage, circulating current, and upper and lower arm current waveforms when SM#4 is under failure and bypassed.

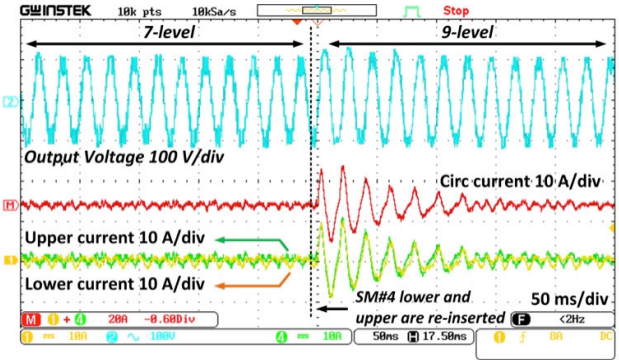

FIGURE 16. Output voltage, circulating current, and upper and lower arm current waveforms when SM#4 at the lower arm is re-inserted.

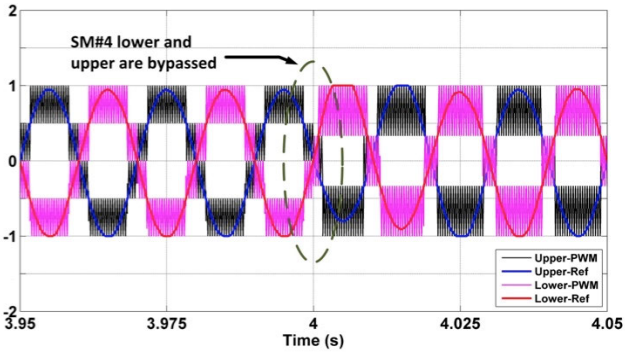

FIGURE 17. Change of adaptive carrier waveforms when SM#4 at lower arm is the failure (bypassed).

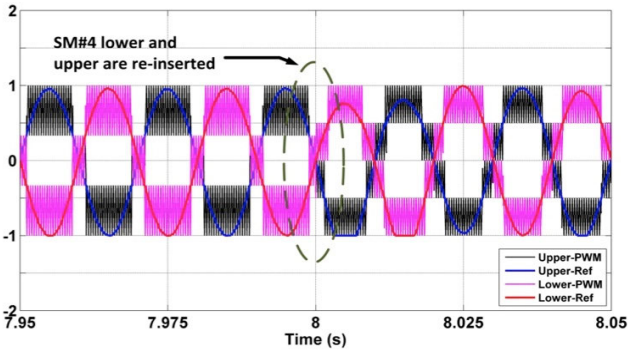

FIGURE 18. Change of adaptive carrier waveforms when SM#4 at the lower arm is re-inserted.

The conventional PDPWM and CPS-PWM use multiple carriers for the multilevel converter. In MMC, one carrier deputizes one SM, which means a large number of carriers are required for a large number of SMs, which increases the computational burden. In CPS-PWM, the phase-shifted between all the all carriers need to re-adjust to isolate the faulty SM. Thus, the proposed method has a low computational burden by using only one single carrier that can be adapted immediately with the new level-number when an SM is under a fault. This proposed method also reduces the complexity in terms of the implementation of the PDPWM modulation technique practically. Since this method is implemented using symmetric operation to maintain the symmetry of arm voltage, it is suitable for a large number of SM.

V. CONCLUSION

This paper presents a modulation technique for MMC based on PDPWM with $2N+1$ level output voltage. The flexibility of the adaptive carrier signal can act as a fault-tolerant

control strategy for MMC based half-bridge SM. The highest magnitude of the output pole voltage is decreased when a faulty SM is bypassed, which results in imbalanced capacitor voltages. The proposed control strategy changes the scale of the staircase signal, that is, it changes the scale of the adaptive carrier signal and the number of the active SM in each arm. Then, the general energy-based and circulating current control structures are highly adaptable to rebalance the remaining healthy SMs.

The experimental setup is assembled to validate the proposed method in real implementation. The proposed control method assures that the converter effectively delivers excellent quality power without decreasing the performance of the converter. After fault clearing in the faulty SM, the converter can immediately return to its normal nine-level voltage. This method has advantages for a large number of SM in terms of cost. The adaptive carrier can adapt immediately when the fault is happening in SM. Moreover, this method can be used for adding more SMs into the arms without turning off the power supply.

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