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A Novel Planar Architecture for Heterojunction TFETs With Improved Performance and Its Digital Application as an Inverter

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ABSTRACT A novel planar architecture is proposed for tunnel field-effect transistors (TFETs). The advantages of this architecture are exhibited, taking the InAs/Si TFET as an example, and the effects of different device parameters are analyzed in detail. Owing to the gate field being parallel to the tunneling interface, the gate control is enhanced, and a better electrical performance is obtained. Moreover, different from a conventional TFET, in which the effective tunneling area and current can hardly be modulated by the gate length, in our proposed device, the effective tunneling area and current can be adjusted depending on the actual requirements of circuit design, which increases the flexibility of TFET-based circuit design. In addition, the device architecture can also be extended to other materials, such as Ge/Si and GaSb/InAs, and thus be used for both n-type and p-type devices. The results show that the complementary digital inverter structure with InAs/Si as the n-type TFET and Ge/Si as the p-type TFET would be helpful for future ultralow power applications. This proposed structure without any complicated fabrication steps shows better compatibility with CMOS technology compared to other TFETs with heterojunction and structural innovations presented in theoretical works.

INDEX TERMS Tunnel field-effect transistor, band-to-band tunneling, InAs/Si heterojunction, complementary TFET inverters.

I. INTRODUCTION

TFETs based on the band-to-band tunneling (BTBT) mechanism can break the 60 mV/decade thermal limitation of the subthreshold swing (SS) and offer steep switching under further scaled supply voltage (V_{DD}), becoming promising for future low power applications [1]–[4]. TFETs have been intensively investigated in recent years and are expected to be seen in semiconductor products after 2022 [5], [6].

Benefiting from the highly mature CMOS technology, many Si TFETs are experimentally reported to break the 60 mV/decade limitation [7]–[9]. However, owing to the low BTBT probability arising from the large and indirect bandgap, the silicon TFET suffers from an unacceptably low on-state current (I_{ON}), which is even lower than the demand reported by the International Technology Roadmap for Semiconductors (ITRS) [10]. This low on-state current leads to a large switching delay (CV_{DD}/I_{ON}), and therefore, practical application of the silicon TFET is hindered.

To resolve this issue, various design improvements have been proposed [11]–[18]. In [11], the Ge/Si heterojunction is proposed, and a U-shaped gate with an n+ pocket is introduced to enhance the tunneling efficiency. Moreover, the U-shaped gate facilitates implementation of a smaller device area. In [12], a low doped pocket is added into the source of staggered heterostructure p-n-i-n TFETs to fully utilize the strain-induced increase in the on-state current. In [13], a uniaxial tensile stress is incorporated into the GeSn n-channel fin TFET to boost the device performance, and a more pronounced I_{ON} is obtained. In [14], a new resonant-TFET (R-TFET) is proposed, and a 100x current advantage over the MOSFET is obtained. In [15], a scalable GaSb/InAs

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TFET with nonuniform body thickness is introduced, and a high I_{ON} of approximately 284 A/m is exhibited. All of these studies are excellent works, and the device performance is largely enhanced by different structural innovations and heterojunctions with much lower tunneling barriers compared with that of the homojunction. However, the fabrication steps required for the novel structures are very complicated and difficult to incorporate into the current CMOS technology [19]. Fabrication compatibility with the conventional platform is extremely significant not only for the practical application of TFETs in the future but also for the TFET-CMOS hybrid design [20], [21].

Another issue that also contributes to the small tunneling current is the small tunneling area limited to the narrow channel/oxide interface near the source side. The limited and concentrated tunneling area also results in almost unchanged tunneling current with channel length [22], [23]. This phenomenon makes modulating the device driving capability to meet the actual needs during the circuit design process difficult.

In addition to the single device performance, that of the complementary TFET inverter, in which both the N-TFET and the P-TFET should be properly designed for complementary performance, is another issue. To boost the on-state current, generally, III-V materials are adopted for n-type TFETs, and group IV materials, such as Ge or GeSi, are used for p-type TFETs [24]. However, the proposed novel structures are usually only suitable for n-type or p-type TFETs due to the lack of material universality, and the two types are usually investigated separately. Thus, the proposed structure usually focuses on only one type, resulting in degraded p-type or n-type performance and accordingly unsatisfactory complementary behavior.

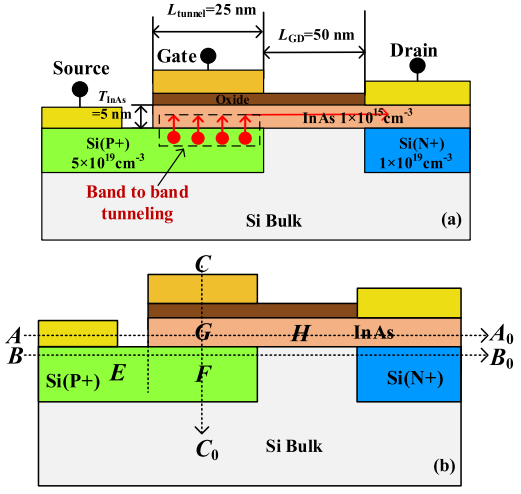

FIGURE 1. (a) Schematic cross-sectional view of the proposal planar TFET structure with an InAs/Si tunneling heterojunction, and (b) region and cutline markers for convenience of subsequent description.

In this paper, a novel architecture is proposed for heterojunction TFETs, as shown in Fig. 1(a), in which the InAs/Si tunneling heterojunction is taken as an example. Compared with the existing methods, our novel structure exhibits many advantages. First, the gate control of the tunneling process is enhanced because the gate field is aligned with the tunneling direction, and much steeper transfer characteristics with a minimum SS of approximately a few millivolts per decade are obtained. Second, the effective tunneling area is enlarged, which boosts I_{ON}. Moreover, the effective tunneling area and I_{ON} can be modulated by the gate length to meet the actual requirements of circuit design, which is of great significance for improving the circuit design flexibility. Third, the structure is the simplest compared with other works and exhibits better compatibility with CMOS technology without any complicated fabrication steps while allowing the current enhancement due to a heterojunction. Finally, the proposed structure shows better material universality. Although the InAs/Si heterojunction is taken as an example, this structure can be extended to other materials. Therefore, it is suitable for both n-type and p-type devices, which is of significance for complementary digital applications.

This article is arranged as follows: Section II presents the device structure and some important simulation details. In Section III, the effects of different device parameters are studied, and the optimized device performance is compared with that of novel TFET structures presented in other theoretical works. The performance of the complementary TFET inverter based on the proposed structure is studied in Section IV. The conclusions are highlighted in Section V.

II. DEVICE STRUCTURE AND NUMERICAL SIMULATION

In this paper, the proposed structure is introduced, taking the InAs/Si TFET as an example considering its very low tunneling mass. However, this does not mean that the structure can only be used for the InAs/Si material. It can be extended to other materials such as the Ge/Si heterojunction, as discussed later. Fig. 1(a) shows the schematic structure of the proposed planar InAs/Si TFET. The uniform doping profiles of the InAs channel layer, P+-doped Si, and N+-doped Si are $N_{InAs} = 1\times10^{15}$ cm^{-3}, $N_{Sour} = 5\times10^{19}$ cm^{-3}, and $N_{Drain} = 1\times10^{19}$ cm^{-3}, respectively. The gate oxide thickness of SiO_2(T_{OX}) and the InAs layer thickness (T_{InAs}) are 1 nm and 5 nm, respectively. The overlapping part of the InAs layer and the P+-doped Si is L_{tunnel} = 25 nm, and the underlapped length between the gate metal and the drain metal L_{GD} is set as 50 nm.

For convenience of subsequent analysis and description, some regions and cutlines are marked in Fig. 1(b). Region G indicates the InAs channel directly under the gate metal, and region H is the InAs part between the gate metal and the drain metal. The P+-doped Si directly under region G is marked as region F, and the rest is region E. Cutlines AA_0 and BB_0 are 1 nm above and below the InAs/Si interface, respectively. CC_0 is perpendicular to the InAs/Si interface and goes through the gate metal and regions G and F. Obviously, the gate (metal and dielectric), InAs channel (region G), and P+-doped Si (region F) form a sandwich structure. Once the conduction band edge of InAs ($E_{C,InAs}$) in region G

modulated by the gate voltage (V_{GS}) is lower than the valance band edge of Si ($E_{V,Si}$) in region F, the carriers in region F can tunnel into region G and then drift in the InAs channel until they are collected by the drain.

The performance of the device has been simulated using the Synopsys Sentaurus Technology Computer-Aided Design (TCAD) tools as in other theoretical works [25], [26]. The BTBT model with the dynamic nonlocal path accounting for the arbitrary tunneling barrier with a nonuniform electrical field is adopted. To obtain reasonable parameters and numerical results as reliable as possible, the experimentally calibrated tunneling parameters $A_{path} = 3\times10^{19}$ $cm^{-3}\cdot s^{-1}$ and $B_{path} = 2.6\times10^{6}$ $V\cdot cm^{-1}$ are adopted in the BTBT model for InAs [27]. For the Si side, the default values of $A_{path} = 4\times10^{14}$ $cm^{-3}\cdot s^{-1}$ and $B_{path} = 1.9\times10^{17}$ $V\cdot cm^{-1}$ are used, which are also obtained from experimental data [28]. To ensure the accuracy of the results at very small dimensions of T_{InAs}, the modified local-density approximation (MLDA) is used to account for the quantum confined carrier distributions. The doping-dependent mobility along with the high-field saturation model, the Shockley-Read-Hall (SRH) recombination model, the band gap narrowing model, and Fermi statistics are also applied in the simulation.

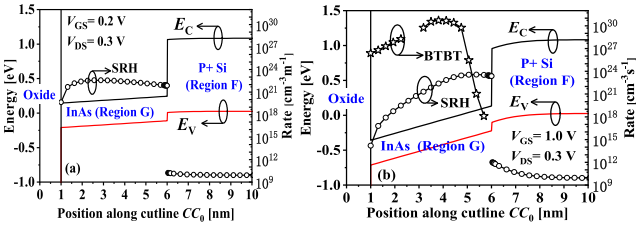

FIGURE 2. Energy band diagrams of the planar InAs/Si TFET along cutline CC_0 in the (a) off-state and (b) on-state.

The device principle can be understood based on the energy band diagrams, BTBT rate, and SRH generation rate along cutline CC_0 demonstrated in Fig. 2. In the off-state, BTBT under the gate from region F to G is forbidden since the $E_{C,InAs}$ in region G is misaligned with the $E_{V,Si}$ in region F, as shown in Fig. 2(a). When a larger V_{GS} is applied, $E_{C,InAs}$ can be lower than $E_{V,Si}$, as exhibited in Fig. 2(b); the current starts to be mainly dominated by the carriers flowing vertically from region F to region G via BTBT, and thus, the device is turned on. Obviously, the gate field is aligned with the carrier tunneling direction in our device, which is different from the gate field being perpendicular to the tunneling direction in conventional TFETs. This alignment enhances the gate control efficiency and improves the device performance, as demonstrated in Fig. 3, which shows the simulated transfer and output characteristics. A small SS_{min} as low as 4.67 mV/dec is obtained, and SS can be less than 60 mV/dec for 3 decades of current, exhibiting excellent transfer properties.

III. KEY PARAMETERS AND DEVICE OPTIMIZATION

In this section, different parameters, including L_{tunnel}, T_{InAs}, T_{ox}, N_{InAs}, N_{Sour}, N_{Drain}, and L_{GD}, are studied in detail,

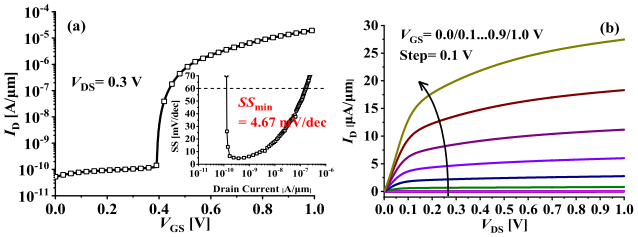

FIGURE 3. (a) I_{DS}-V_{GS} characteristics and SS-I_{DS} curve (insert) and (b) output characteristics of the proposed planar InAs/Si TFETs.

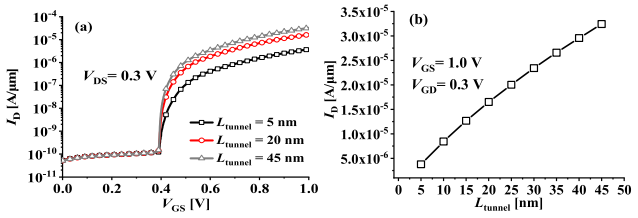

FIGURE 4. Effect of L_{tunnel} on the (a) I_{DS}-V_{GS} characteristics and (b) on-state current.

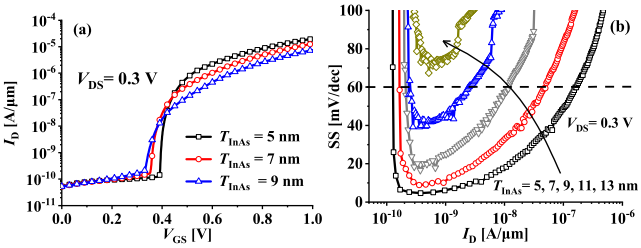

FIGURE 5. Effect of T_{InAs} on the (a) I_{DS}-V_{GS} characteristics and (b) SS.

and the device performance is enhanced by adopting the optimized values.

In the on-state of our proposed device, the carriers vertically tunnel from region F to G. The interface length L_{tunnel} between regions F and G dominates the effective tunneling area. Therefore, a large L_{tunnel} is intuitively understood to result in enhanced I_{ON} due to the enlarged tunneling area, as presented in Fig. 4(a). In a conventional TFET, the carrier tunneling is limited to the channel/oxide interface near the source side. The effective tunneling area and the tunneling current can hardly be modulated by the gate length [22], [23]. However, in our devices, the almost linear relationship between I_{ON} and L_{tunnel} indicated in Fig. 4(b) allows designers to easily adjust I_{ON} to meet the actual demand of different circuits and thus enhances the flexibility of circuit design, similar to that in MOSFETs.

Because the InAs layer is between the gate and the tunneling junction, a thick InAs layer would lead to weakened gate control of the InAs/Si tunneling junction. The influence of T_{InAs} on the device performance is exhibited in Fig. 5. A thicker T_{InAs} obviously results in slightly decreased I_{ON} and degraded SS characteristics. Actually, SS, namely, the gate voltage required to change the drain current by one order of magnitude when the transistor is operated in

the subthreshold region, can be expressed as follows [29].

$$SS = \underbrace{\frac{dV_G}{d\varphi_{\text{inter}}}}_{m} \underbrace{\frac{d\varphi_{\text{inter}}}{d\left(\log_{10} I_{ON}\right)}}_{n} \tag{1}$$

where φ_{inter} is the potential at the tunneling interface between regions G and F. The term m reflects the efficiency of control of φ_{inter} by V_{GS}, and the smaller m is, the stronger the gate control efficiency and the smaller the SS. The term n is a factor that characterizes the change in the drain current with potential φ_{inter}, reflecting the conduction mechanism. For our proposed structure, the gate (metal and dielectric), InAs channel (region G), and P+-doped Si (region F) form a sandwich structure. The term m can be obtained using the gate oxide capacitance C_{ox}, InAs layer capacitance C_{InAs}, and depletion capacitance C_{dep} in series, as in (2).

$$m = \frac{dV_G}{d\varphi_{\text{inter}}} = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{dep}}{C_{InAs}} \tag{2}$$

m obviously exhibits a minimum of 1. Increased C_{ox} and C_{InAs} and decreased C_{dep} help reduce m and SS. Therefore, a thicker T_{InAs} leads to degraded SS owing to the decreased C_{InAs}. To achieve SS less than 60 mV/dec over at least two decades of drain current, T_{InAs} should be kept thinner than approximately 10 nm, which is not a great issue for modern nanotechnology [30], [31].

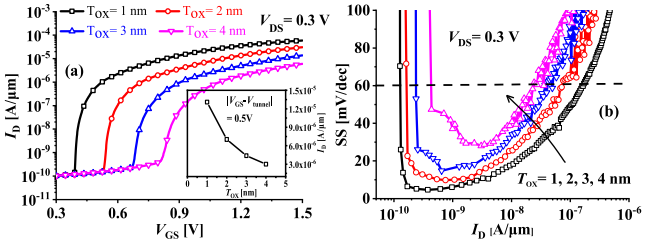

FIGURE 6. Effect of T_{ox} on the (a) I_{DS}-V_{GS} characteristics and I_{ON} extracted at $|V_{GS}-V_{tunnel}| = 0.5$ V (insert) and (b) SS.

T_{ox} is also an important factor affecting device performance, and its influence is exhibited in Fig. 6(a). A thicker T_{ox} leads to increased V_{tunnel} at which the drain current starts to be higher than the reverse leakage current. The increased V_{tunnel} indicates a weakened tunneling capability. The I_{ON} extracted at $|V_{GS}-V_{tunnel}| = 0.5$ V is presented in the insert of Fig. 6(a), and obviously, a thicker T_{ox} results in a reduced I_{ON}. In addition to I_{ON}, SS can also be degraded with thicker T_{ox}, as shown in Fig. 6(b) by the increased SS_{min} and the reduced current range over which SS is less than 60 mV/dec. Actually, this result is similar to the influence of T_{InAs}. The decreased C_{ox} caused by a thicker T_{ox} results in an increased m in (2) and thus a degraded SS in (1).

The InAs layer doping density N_{InAs} has a great effect on the device performance, as shown in Fig. 7. With increased N_{InAs}, I_{OFF} and SS are significantly degraded, and the device cannot be turned off for $N_{InAs} = 5 \times 10^{18}$ cm^{-3}. Fig. 8(a) gives the SRH and BTBT rates along cutline AA_0 in the off-state. The BTBT rate in region H is clearly much larger than

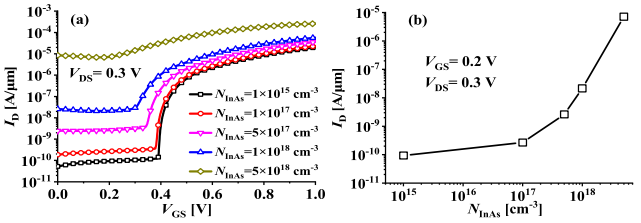

FIGURE 7. Device (a) I_{DS}-V_{GS} characteristics and (b) off-state current as a function of the InAs layer doping density N_{InAs}.

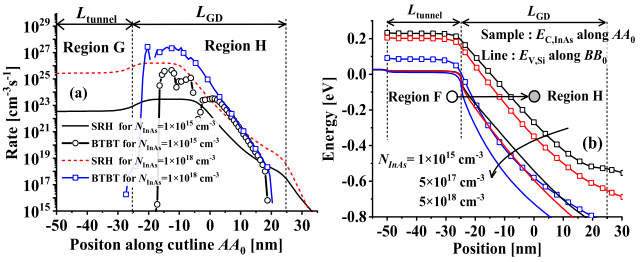

FIGURE 8. (a) SRH and BTBT rates along cutline AA_0 and (b) $E_{C,InAs}$ along AA_0 and $E_{V,Si}$ along BB_0 in the off-state (V_{GS} = 0.2 V, V_{DS} = 0.3 V) for different N_{InAs}.

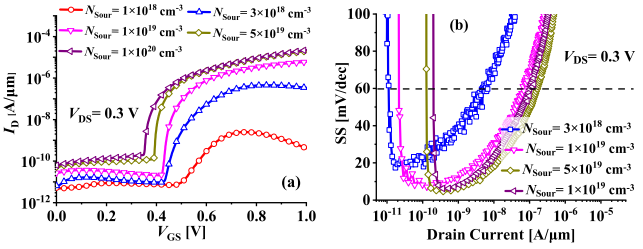

FIGURE 9. Device (a) I_{DS}-V_{GS} and (b) SS-I_D characteristics as a function of the P+ Si doping concentration N_{Sour}.

the SRH generation rate and should dominate I_{OFF}. To determine where the carriers in region H tunnel from, Fig. 8(b) illustrates the $E_{C,InAs}$ along AA_0 and the $E_{V,Si}$ along BB_0. The $E_{V,Si}$ in region F obviously overlaps with the $E_{C,InAs}$ in region H, allowing electrons to tunnel from region F into H. The unexpected parasitic tunneling dominates I_{OFF}. Moreover, with increased N_{InAs}, $E_{C,InAs}$ becomes lower, which reduces the tunneling barrier width between regions F and H. Thus, the BTBT rate in region H becomes higher (Fig. 8(a)), and I_{OFF} increases (Fig. 7(b)).

The impact of N_{Sour} is shown in Fig. 9(a), and increased N_{Sour} clearly leads to increased I_{OFF} and I_{ON}. However, for N_{Sour} above 1×10^{19} cm^{-3}, I_{OFF} and I_{ON} are not very different. Considering that the current range over which SS is below 60 mV/dec is reduced with N_{Sour} above 1×10^{19} cm^{-3}, as depicted in Fig. 9(b), taking $N_{Sour} = 1 \times 10^{19}$ cm^{-3} as the optimal value is reasonable.

The slightly P+-doped Si region can be considered to be depleted, and the gate voltage drops in both regions G and F. In other words, the $E_{C,InAs}$ in region G and the $E_{V,Si}$ in region F simultaneously decrease when V_{GS} increases. Thus, the $E_{C,InAs}$ in region G and the $E_{V,Si}$ in region F cannot overlap, and carrier tunneling from region F to G never occurs,

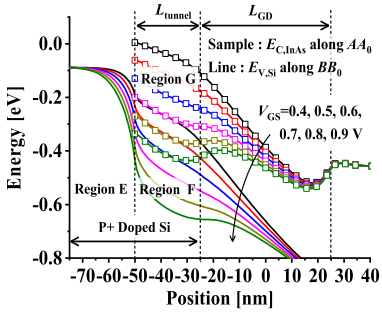

FIGURE 10. $E_{C,InAs}$ along AA_0 and $E_{V,Si}$ along BB_0 for $N_{Sour} = 1 \times 10^{18}$ cm^{-3}.

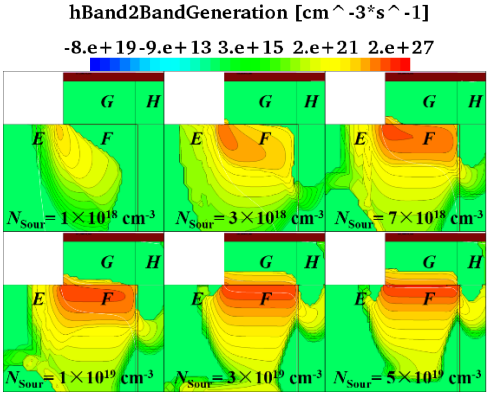

FIGURE 11. Contour mapping of the hole BTBT rate distribution for the devices with different N_{Sour} at $V_{GS} = 1.0$ V.

as demonstrated in Fig. 10, which shows the $E_{C,InAs}$ along AA_0 and the $E_{V,Si}$ along BB_0 for a device with a low P+ doping concentration of $N_{Sour} = 1 \times 10^{18}$ cm^{-3}. However, the $E_{V,Si}$ in region E drops slower than the $E_{C,InAs}$ in region G, and the $E_{V,Si}$ in region E overlaps with the $E_{C,InAs}$ in region G with increased V_{GS}. This phenomenon allows the carriers in region E to tunnel into region G, dominating the drain current. With increased N_{Sour}, the P+-doped Si in region F is no longer depleted, and the large number of carriers in region F screen the gate electric field. Therefore, the gate voltage mainly drops in region G, and the $E_{V,Si}$ in region F remains almost unchanged when the $E_{C,InAs}$ in region G decreases with increased V_{GS}. Thus, carrier tunneling from region F to G occurs. Fig. 11 illustrates the contour mapping of the hole BTBT rate distribution for different N_{Sour}. For slightly doped N_{Sour}, the tunneling process mainly occurs between regions E and G, and holes are mainly generated in region E. With increased N_{Sour}, the tunneling process gradually moves to between regions F and G, and the hole generation gradually moves to region F.

As a part of the tunneling junction, the P+-doped Si is the source of carriers tunneling into the InAs channel. Different from this, the N+-doped Si region does not participate in the tunneling process. The main role of the N+-doped Si is to form a reverse PN junction with the P+-doped region obstructing the current path in the Si substrate and allowing

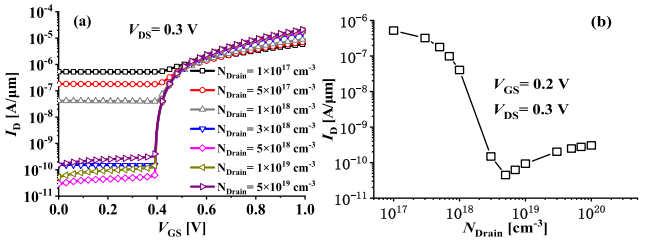

FIGURE 12. Device (a) I_{DS}-V_{GS} characteristics and (b) I_{OFF} as a function of the N+ Si doping concentration N_{Drain}.

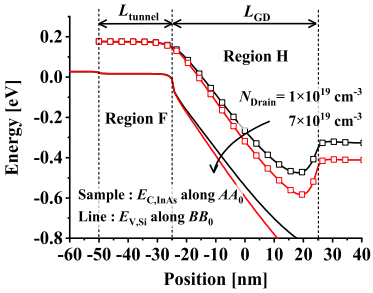

FIGURE 13. $E_{C,InAs}$ along AA_0 and $E_{V,Si}$ along BB_0 for different N_{Drain} at $V_{GS} = 0.2$ V and $V_{DS} = 0.3$ V.

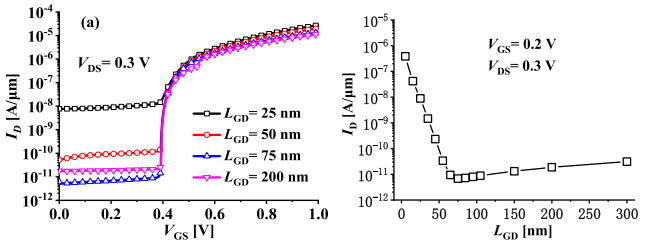

FIGURE 14. Device (a) I_{DS} $-V_{GS}$ characteristics and (b) I_{OFF} as a function of L_{GD}.

current flow only through the InAs/Si junction by tunneling. The influence of the N+ doping concentration N_{Drain} is shown in Fig. 12, and the device with a lightly N+-doped region exhibits large I_{OFF}. For $N_{Drain} = 1 \times 10^{17}$ cm^{-3}, the device cannot be thoroughly turned off, as the current directly flows from the P+-doped region to the N+-doped region via drift. With increased N_{Drain}, I_{OFF} is suppressed. However, the slightly increased I_{OFF} above $N_{Drain} = 5 \times 10^{18}$ cm^{-3} indicates an optimal value of approximately 5×10^{18} cm^{-3} at which I_{OFF} reaches the minimum value. This result can be explained using Fig. 13, which shows the $E_{C,InAs}$ along AA_0 and the $E_{V,Si}$ along BB_0 in the off-state. Although the increased N_{Drain} suppresses the current component through the Si bulk, it also induces a larger electric field and a steeper energy band profile between the P+ Si region and the N+ Si region, leading to a smaller tunneling width and an enhanced tunneling probability from region F to H.

The distance between the gate metal and the drain metal L_{GD} is another important parameter, and its effect is exhibited in Fig. 14. Similar to N_{Drain}, L_{GS} also mainly affects I_{OFF}, and

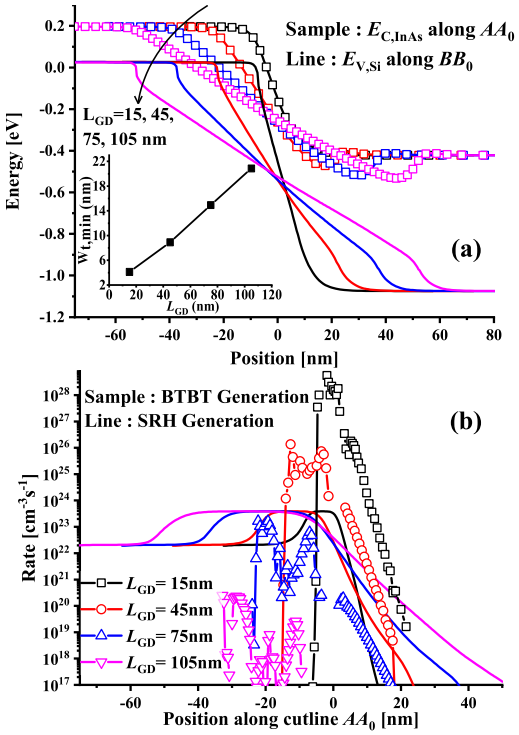

FIGURE 15. (a) $E_{C,InAs}$ along AA_0, $E_{V,Si}$ along BB_0 and tunneling width (insert) and (b) SRH and BTBT rates along AA_0 for different L_{GD} at V_{GS} = 0.2 V and V_{DS} = 0.3 V. Note that the edge of regions G and H is at position = $-L_{GD}/2$ because the coordinate origin is set at the midpoint of region H in our work.

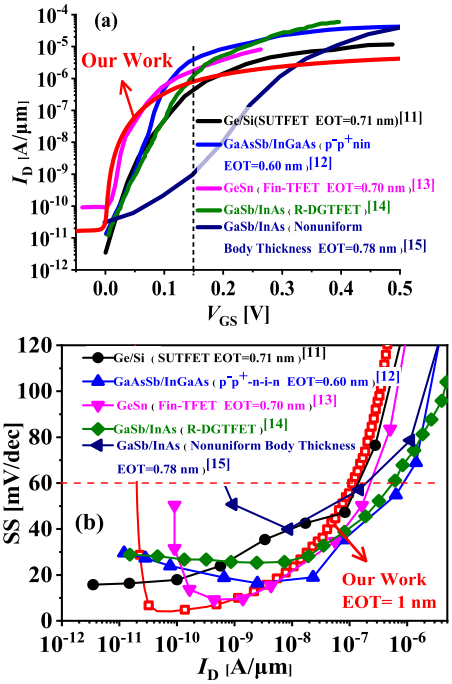

FIGURE 16. (a) I_{DS}-V_{GS} and (b) SS-I_{DS} characteristic comparison among the proposed InAs/Si TFET and novel TFET structures presented in other theoretical works.

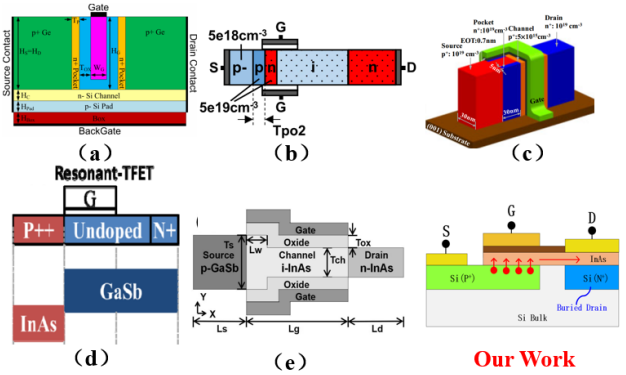

FIGURE 17. Structure comparison of some novel TFET devices. (a) Ge/Si SUTFET, (b) GaAsSb/InGaAs P$^-$ P$^+$ TFET, (c) GeSn Fin-TFET, (d) GaSb/InAs R-DGTFET, and (e) GaSb/InAs TFET with nonuniform body thickness.

an optimal value of approximately 75 nm is obtained. Considering that I_{OFF} mainly arises from the parasitic tunneling between regions F and H, Fig. 15(a) depicts the $E_{C,InAs}$ along AA_0 and the $E_{V,Si}$ along BB_0 in the off-state for different L_{GD}. An increased L_{GD} obviously leads to a smooth energy band profile and thus an increased tunneling width (insert in Fig. 15(a)) between regions F and H, which suppresses the parasitic tunneling probability, as demonstrated in Fig. 15(b). This phenomenon is why I_{OFF} decreases with increasing L_{GD} below 75 nm. However, as shown in Fig. 15(b), the parasitic BTBT rate only dominates I_{OFF} for $L_{GD} < 75$ nm, and for $L_{GD} > 75$ nm, the SRH rate plays the major role. Therefore, I_{OFF} shows a slight linear increase with increasing L_{GD} above 75 nm owing to the enhanced SRH current resulting from the enlarged SRH area.

Fig. 16 presents a performance comparison among the optimized InAs/Si TFET and other TFETs with heterojunction and structural innovations presented in theoretical works [11]–[15]. The transfer curves have been translated so that the tunneling current starts to be higher than I_{OFF} at $V_{GS} = 0$ V for ease of comparison. Despite the relatively low I_{ON} at $V_{GS} = 1.0$ V, our proposed InAs/Si TFET exhibits the highest I_{ON} for $V_{GS} < 0.15$ V (Fig. 16(a)) and the lowest SS (Fig. 16(b)) even with a relatively large effective oxide thickness (EOT), indicating that the proposed device is much more promising for future ultralow power applications.

In addition to the excellent performance, our proposed architecture also presents advantages in terms of structure design and fabrication process. Fig. 17 demonstrates the novel device structures in [11]–[15] with corresponding transfer curves in Fig. 16. The proposed device structures in Fig. 17(a)-(e) are clearly relatively complicated and show poor compatibility with the conventional CMOS technology. By comparison, our proposed structure is planar and the simplest. The basic steps of the process flow are exhibited in Fig. 18 in a convenient manner. Obviously, our structure is more compatible with the conventional CMOS fabrication, which is of extreme significance for the practical application of TFETs in the future.

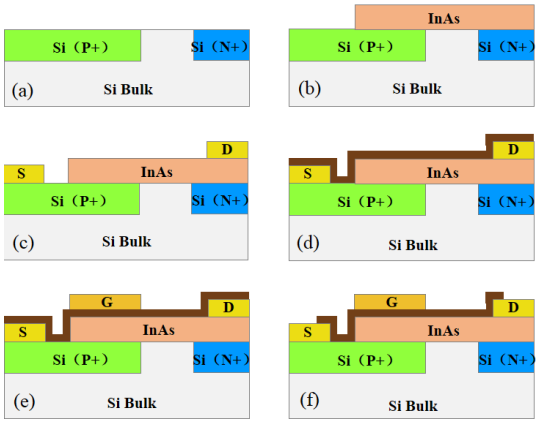

FIGURE 18. Proposed process steps for the planar InAs/Si TFET. (a) P+ and N+ ion implantation and annealing in the Si bulk. (b) InAs layer epitaxy. (c) Source and drain metal patterning. (d) Gate dielectric deposition. (e) Gate metal patterning. (f) Dielectric etching.

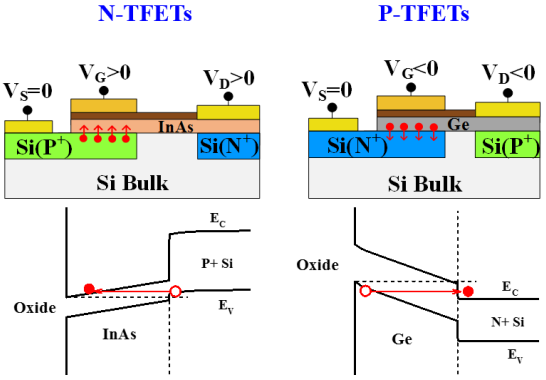

FIGURE 19. Proposed InAs/Si N-TFET and Ge/Si P-TFET, and corresponding energy band profiles along cutline CC_0 in the on-state.

IV. PERFORMANCE OF THE COMPLEMENTARY TFET INVERTER BASED ON THE PROPOSED STRUCTURE

As noted in Section I, the N-TFET and P-TFET are usually investigated separately to obtain the optimal performance for only one type of device, which results in unsatisfactory complementary behavior due to the lack of material universality and degraded p-type or n-type performance. By comparison, our proposed structure is suitable for different materials, such as InAs, Ge, and GaSb, and is more suitable for complementary device performance and inverters. Taking Ge as an example, Fig. 19 shows the proposed InAs/Si N-TFET and Ge/Si P-TFET along with the corresponding energy band along cutline CC_0 in the on-state. The principle of the Ge/Si P-TFET is similar to that of the InAs/Si N-TFET discussed above. As the valance band of Ge is elevated to be higher than the conductance band of N+ Si, electrons can tunnel from the Ge to N+- doped Si region, and thus, a current flows from the source to the drain.

For the device parameters listed in Table 1, the highly complementary performance shown in Fig. 20(a) is obtained. Both the N-TFET and the P-TFET show steep I_{DS}-V_{GS} characteristics, and SS can be less than 60 mV/dec over almost four decades of current, which indicates that the devices are promising for further reducing the supply voltage. The transient response of the complementary inverter is exhibited in Fig. 20(b), and the inverted output signal with the input signal at a supply voltage of 0.3 V reveals that our proposed devices are promising for future low power digital applications.

TABLE 1. Device parameters adopted in the TFET inverter based on the proposed InAs/Si N-TFET and Ge/Si P-TFET.

Symbol	Ge/Si P-TFET	InAs/Si N-TFET
EOT	0.71 nm	1 nm
T_{Ge}/T_{InAs}	5 nm	5 nm
N_{Ge}/N_{InAs}	1×10^{18} cm^{-3}	1×10^{18} cm^{-3}
N_{Sour}	2×10^{19} cm^{-3}	1.2×10^{19} cm^{-3}
N_{Drain}	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
L_{tunnel}	30 nm	30 nm
L_{GD}	50 nm	50 nm

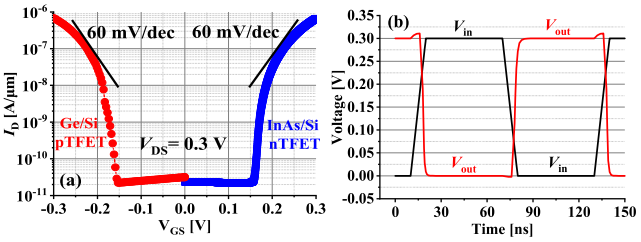

FIGURE 20. (a) I_{DS}-V_{GS} characteristics of the complementary TFET using the InAs/Si N-TFET and Ge/Si P-TFET with the parameters listed in Table 1. (b) Input signal and transient response of the complementary TFET inverter with our proposed devices.

V. CONCLUSION

A novel architecture is proposed for TFETs, and taking the InAs/Si TFET as an example, the device parameters are investigated in detail. The advantages of the proposed architecture include the following: First, the gate control is enhanced and the electrical performance is improved owing to the gate field being parallel to the tunneling direction. Second, the effective tunneling area and current in our proposed devices can be adjusted depending on the actual requirements of circuit design, which increases the flexibility of TFET-based circuit design. Third, the device architecture exhibits better material compatibility and can be adopted for both n-type and p-type devices. Fourth, this proposed structure shows good compatibility with CMOS technology without any complicated fabrication steps. In summary, the proposed architecture would be helpful for future ultralow power digital applications.

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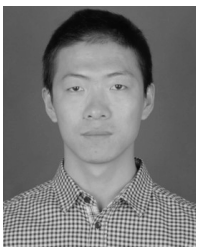

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