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Geometric Analysis and Systematic Design of Millimeter-Wave Low-Power Frequency Dividers in 65-nm CMOS

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ABSTRACT Broadband current-mode logic static divide-by-2 and divide-by-4 circuits fabricated in 65-nm CMOS are presented. The low-power frequency dividers are analyzed in a geometric way. The self-oscillation frequency and locking range of current-mode dividers are analyzed based on current vectors. A systematic design methodology is proposed to reduce power consumption and enhance the locking range. The divide-by-2 circuit operates from 8 to 40 GHz with 0 dBm input signal and consumes dc power of 4.6 mW with a 1.0 V supply. The divide-by-4 circuit operates from 12.4 to 38.4 GHz with 0 dBm input signal and consumes dc power of 7.5 mW with a 1.0 V supply. The core areas of divide-by-2/4 circuits are only $25 \times 33\ \mu m^2$ and $47 \times 28\ \mu m^2$ respectively.

INDEX TERMS Frequency dividers, CMOS, millimeter-wave IC, low power.

I. INTRODUCTION

The Federal Communications Commission (FCC) has allocated 24, 28, 37 and 39 GHz bands as key frequency bands for 5G millimeter-wave (mm-Wave) communication [1]. As CMOS gate size scales aggressively, the technology has provided high-speed performance for the mm-Wave analog system and is becoming a strong candidate for the 5th generation communication design platform [2]. A frequency divider is an essential building block in the high-performance frequency synthesizer to guarantee high-quality 5G links. Injection-locked frequency dividers (ILFD) and current-mode logic (CML) frequency dividers are widely used in the mm-Wave band. Injection-locked dividers lend themselves to the higher frequency of operation and less power consumption but occupy more area and provide limited locking range (LR) [3]. Compared to the injection-locked divider, the current-mode logic divider is an attractive candidate featured by the wide locking range [4]. Therefore, it is able to cover the complete 5G millimeter-wave bands worldwide from 24 to 40 GHz. A wide LR is also necessary to overcome the process-voltage-temperature (PVT) variations.

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The different insights have been presented to analyze the CML frequency dividers. Traditionally,the analysis of the block is based on digital flip-flops [5]. This method fails to explain the self-oscillation and the existence of the lower limit of operation frequency. The work in [6] models the CML divider as a single-balanced mixer and with steady-complex analysis at output frequency but fails to explain the upper limit of the locking range. The work in [7] presents a novel insight based on injection-locking phenomena but does not detail the analysis of working conditions.

In this brief, the main determinants of self-oscillation frequency, small-signal gain, and boundaries of locking range are proposed, which are applicable to CML dividers with any frequency division ratio. A geometric analysis of CML dividers is detailed in a straightforward way. A systematic design methodology is proposed to improve LR and reduce power consumption. Fabricated in 65-nm CMOS, divide-by-2 and divide-by-4 circuits achieve measured LRs from 8 to 40 GHz and from 12.4 to 38.4 GHz respectively with 0 dBm input power level.

This paper is organized as follows. Section II describes the proposed geometric analysis of the frequency dividers. The main determinants of self-oscillation frequency, small-signal gain, and locking range are analyzed. Design and

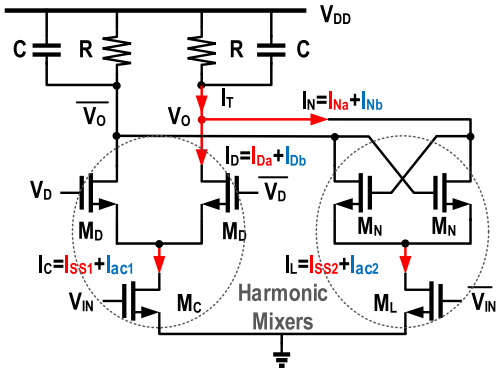

FIGURE 1. A CML latch consisting of a differential pair and a regenerative pair.

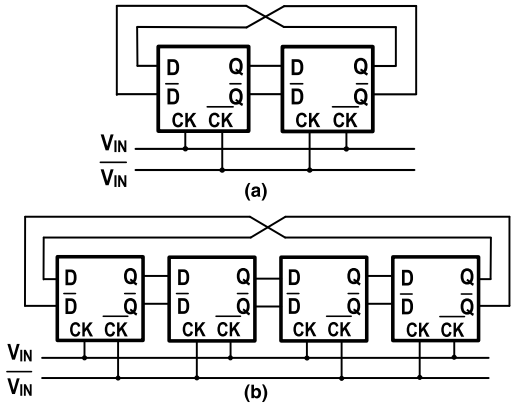

FIGURE 2. (a) Divide-by-2 circuit topology. (b) Divide-by-4 circuit topology.

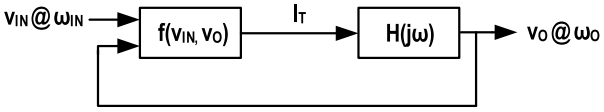

FIGURE 3. The general model for the injection-locked dividers.

implementation details are given in Section III. Section IV provides the measurement results of two CML dividers designs.Concluding remarks are given in Section V.

II. GEOMETRIC ANALYSIS OF THE FREQUENCY DIVIDERS

A cascade of an even number of latches closed in a feedback loop can realize a frequency divide-by-n circuit [8]. CML dividers can be viewed as master-slave flip-flops consisting of CML latches. The CML latch is composed of an input differential pair (M_D), a cross-coupled pair (M_N) and a clocked pair (M_C, M_L) as depicted in Fig. 1. The topologies of divide-by-2 and divide-by-4 circuits are shown in Fig.2.

CML dividers have two operating states, input-locked (IL) mode and self-oscillation (SO) mode. In the absence of an input signal, the circuit simply works as a ring oscillator. In the IL mode, the circuit behaves as an oscillator that is injection-locked to the input signal. A unified model for injection-locked frequency dividers depicted in Fig. 3 has been presented in [9] and is also applicable to the analysis of CML dividers. Assume that f (v_{IN}, v_O) is a memoryless

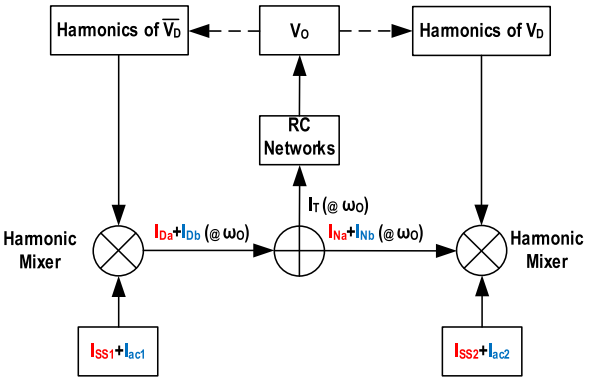

FIGURE 4. CML dividers model based on harmonic mixers.

nonlinear function of both v_{IN} and v_O. The linear filter H(jω) rejects frequency components far from ω_O. The active devices of the CML latch work as two equivalent harmonic mixers as depicted in Fig. 1, modeled by the function f. Assuming a weak input signal, f (v_{IN}, v_O) can be expressed as

$$f\left(v_{IN}, v_O\right) = \sum_{m=0}^{\infty} A_m \cos\left(m\omega_O t + m\varphi\right) + \frac{1}{2}\sum_{m=0}^{\infty} V_{IN} A'_m cos\left[\left(m\omega_O \pm \omega_{IN}\right) t + m\varphi\right] \tag{1}$$

where

$$A'_m = \left.\frac{\partial A_m}{\partial v_{IN}}\right|_{v_{IN}=V_{DC}}$$

The coefficients A_m are functions of the amplitude of v_{IN} and v_O. Note that the first sum term of f (v_{IN}, v_O) corresponds to the free-running ring oscillator. It is independent of the input signal v_{IN} and is produced by v_O and DC offset V_{DC} through the nonlinear network. In CML dividers, the components generated by two mixers are given by I_{Da} and I_{Na} which correspond to the component working at ω_O in the first term. The second sum term of f (v_{IN}, v_O) corresponds to the injected signal in the IL mode. It is generated by v_{IN} and the harmonics of v_O. I_{Db} and I_{Nb} correspond to the components of the second term operating at ω_O. Based on the analysis above, the CML frequency dividers behavior model is shown in Fig. 4.

The operation of the CML divide-by-n circuit must fulfill three conditions which will be the basis of the following analysis. First, the total phase shift of the loop is 360°. Since the negative feedback introduces 180°, the signal in each latch experiences (180/n)° frequency-dependent phase shift, Second, the small-signal loop gain at the self-oscillation frequency (f_{OSC}) is larger than unity. Third, the differential pair experiences nearly complete switching. The first two conditions are consistent with the Barkhausen criterion. The last one makes equivalent harmonic mixers work properly.

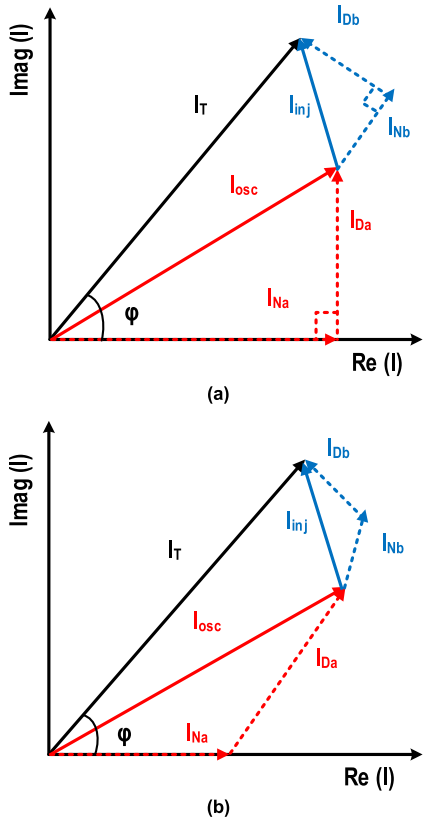

FIGURE 5. Phasor diagrams of current vectors of divide-by-2/4 latches. (a) Divide-by-2 latches. (b) Divide-by-4 latches.

A. THE ANALYSIS OF SELF-OSCILLATION FREQUENCY

Since signals $\overline{v_D}$ and v_O are (180/n)° frequency-dependent phase shift, $\overline{v_D}$ and $\overline{v_O}$ have (180/n)° phase difference. Hence the phase of I_{Na} lags that of I_{Da} by 90° in divide-by-2, and 45° in divide-by-4. According to equation (1), the phase difference between I_{Db} and I_{Nb} is equal to that of I_{Da} and I_{Na}. Assuming that the initial phase of the AC current I_{Na} is 0°, I_T can be given by

$$I_T = I_{Da} + I_{Na} + I_{Db} + I_{Nb} = I_{OSC} + I_{inj} \tag{2}$$

where $I_{OSC} = I_{Da} + I_{Na}$, $I_{inj} = I_{Db} + I_{Nb}$. These current components operate at output frequency ω_O with different amplitudes and phases and can be treated as vectors. In Fig. 5, the phasor diagrams summarize the current relationship of divide-by-2 and divide-by-4 circuits. Vectors superposition makes the phase of I_T deviate from that of I_{Na} by φ. Note that I_{Na} is generated by passing $\overline{v_O}$ and V_{DC} through the equivalent harmonic mixer. Therefore, I_{Na} is in phase with $\overline{v_O}$ and has (180)° phase difference from v_O. v_O can also be expressed as

$$v_O = -I_T Z_{RC} \tag{3}$$

where Z_{RC} is the impedance of the RC network. $I_T Z_{RC}$ and I_{Na} must remain in phase. Therefore, the RC network contributes a phase shift to cancel the phase of I_T (i.e., φ).

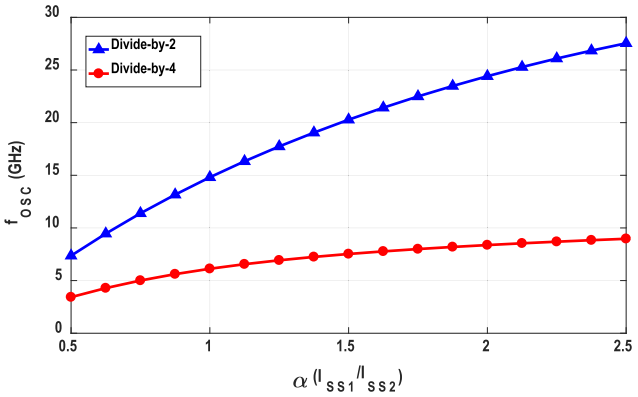

FIGURE 6. Simulated f_{OSC} versus α when I_{SS2} = 800 μA, R = 400 Ω, $W_{MD} = W_{MN}$ = 8 μm. All transistors are minimal length.

According to the phase-frequency characteristics of RC parallel circuits, We have

$$\varphi = -\varphi_{RC} = \arctan(\omega_o RC)\,. \tag{4}$$

φ_{RC} is the phase shift of the RC network at ω_O. In SO mode, (i.e., $|I_{inj}| = 0$ and $I_T = I_{OSC}$), vectors of I_{Da}, I_{Na} and I_{OSC} form a triangle as depicted in Fig. 5. Then the phase shift φ_0 can be obtained as

$$\varphi_0 = \arctan\left(\frac{|I_{Da}|\sin\frac{\pi}{n}}{|I_{Na}| + |I_{Da}|\cos\frac{\pi}{n}}\right) \tag{5}$$

The self-oscillation frequency can be calculated from (4) and (5)

$$\omega_{OSC} = \frac{|I_{Da}|\sin\frac{\pi}{n}}{|I_{Da}|\cos\frac{\pi}{n} + |I_{Na}|} \cdot \frac{1}{RC} \tag{6}$$

It can be rewritten as

$$\omega_{OSC} = \frac{\sin\frac{\pi}{n}}{\cos\frac{\pi}{n} + \frac{1}{\alpha}} \cdot \frac{1}{RC} \tag{7}$$

where

$$\alpha = \frac{|I_{Da}|}{|I_{Na}|}$$

Assume that the two equivalent harmonic mixers have the same conversion gain. Then

$$\alpha = \frac{I_{SS1}}{I_{SS2}} \tag{8}$$

Obviously, ω_{OSC} is positively related to α and inversely proportional to RC. It is a feasible method to enhance self-oscillation frequency ω_{OSC} by increasing α. Further analysis shows that ω_{OSC} is negatively related to frequency division ratio n (n≥2), which means high output frequency is hard to achieve in case of a large n. Simulation results confirm the relationship between ω_{OSC} and α as depicted in Fig. 6. The curve is flatter with a large n. If we keep α constant, ω_{OSC} and $I_{SS1,2}$ are irrelevant. The simulation has been done and the results are depicted in Fig. 7.

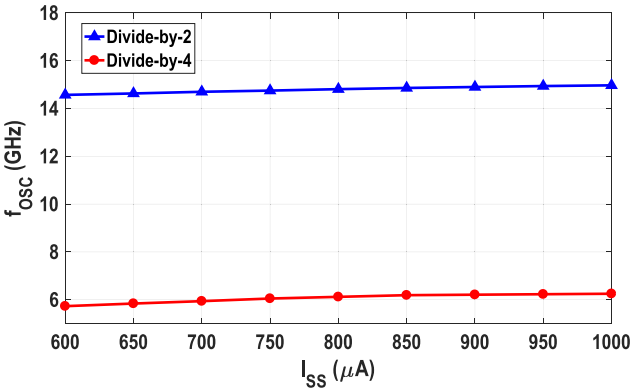

FIGURE 7. Simulated f_{OSC} versus I_{SS} ($I_{SS} = I_{SS1} = I_{SS2}$) when $\alpha = 1$, R = 400 Ω, $W_{MD} = W_{MN} = 8$ μm. All transistors are minimal length.

B. THE SMALL SIGNAL GAIN OF RING OSCILLATOR

The above analyses are based on the phase conditions of the Barkhausen criterion. In this part, the small-signal gain of CML dividers at ω_{OSC} is discussed.

$$I_{OSC} = I_{Da} + I_{Na} = g_{mD}\overline{v_D} + g_{mN}\overline{v_O} \tag{9}$$

v_O and $\overline{v}_O$ can be expressed in the form of amplitude and phase.

$$I_{OSC} = g_{mD}\left|\overline{v_D}\right| e^{j\cdot\frac{\pi}{n}} + g_{mN}\left|\overline{v_O}\right| e^{j\cdot 0} \tag{10}$$

From equation (3), I_{OSC} can also be expressed as

$$I_{OSC} = -\left(\frac{1}{R} + j\omega_{OSC}C\right)\cdot|v_O|\, e^{j\cdot\pi} \tag{11}$$

The real part of I_{OSC} flows through the resistor R and the imaginary part charges and discharges the capacitor. It can be obtained through further calculations as

$$g_{mD}\left|\overline{v_D}\right|\cdot\cos\frac{\pi}{n} + g_{mN}\left|\overline{v_O}\right| = \frac{1}{R}\cdot|v_O| \tag{12}$$

$$g_{mD}\left|\overline{v_D}\right|\cdot sin\frac{\pi}{n} = \omega_{OSC}\cdot C\cdot|v_O| \tag{13}$$

Substitute formula (7) into (12) and (13). We get that (12) and (13) are equivalent at the self-oscillation frequency. Therefore, the second condition of the Barkhausen criterion can be expressed as

$$g_{mD}\cdot\cos\frac{\pi}{n} + g_{mN} \geq \frac{1}{R}. \tag{14}$$

Consistent with intuition, the small-signal gain is positively related to transconductance g_{mD} and g_{mN} and is also proportional to R. Besides, as the angle between I_{Da} and I_{Na} becomes smaller (i.e., a large n), I_{OSC} increases and a larger gain can be obtained.

C. THE LOCKING RANGE OF CML DIVIDERS

When an input signal is applied, the circuit can no longer oscillate at ω_{OSC}, because the phase of I_T at this frequency deviates from φ_0 by θ. Assuming that $\left|I_{inj}\right|$ is constant and the phase difference θ between I_{inj} and I_{OSC} varies from 0° to 360°, the end-point of vector I_T forms an input locked circle

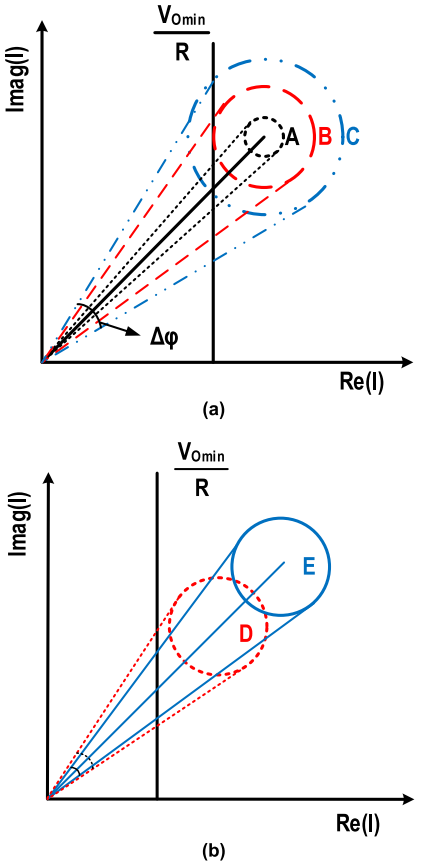

FIGURE 8. Input locked circle and phasor diagrams of the circuit in different working situation. (a) Variation of locking range with different I_{inj}. (b) Variation of locking range at the same oscillation frequency f_{OSC} and I_{inj}.

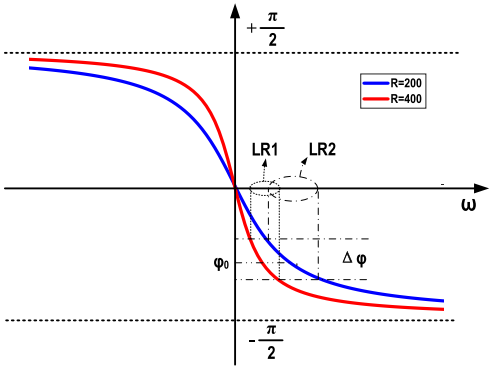

FIGURE 9. The RC phase-frequency curves and the relationship between $\Delta\varphi$ and LR (C = 30 fF).

as depicted in Fig. 8(a). Considering angle θ, not every point on the circle is a solution for the circuit, but it is useful for the circuit behavior visualization. The angle of I_T varies by $\Delta\varphi$ corresponding to the LR under this $\left|I_{inj}\right|$ as shown in Fig. 8(a) and Fig. 9.

According to the third condition, for M_D and M_N to undergo near-complete switching, a sufficient output voltage is required. It can be given by

$$|v_O| \geq V_{Omin} \approx \frac{1}{2}\sqrt{\frac{2I_{C,L}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{MD,MN}}}. \tag{15}$$

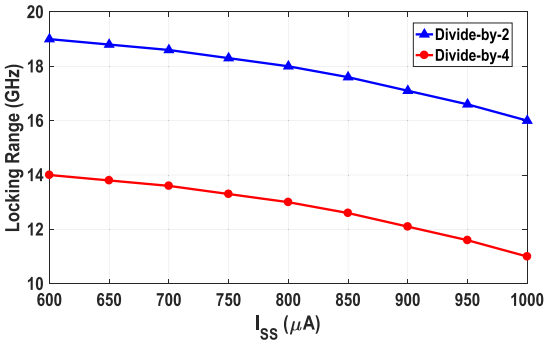

FIGURE 10. Simulated LR versus I_{SS} ($I_{SS} = I_{SS1} = I_{SS2}$) when $\alpha = 1$, $W_{MD} = W_{MN} = 8$ μm, R = 400 Ω, $|I_{inj}| = 100$ μA. All transistors are minimal length.

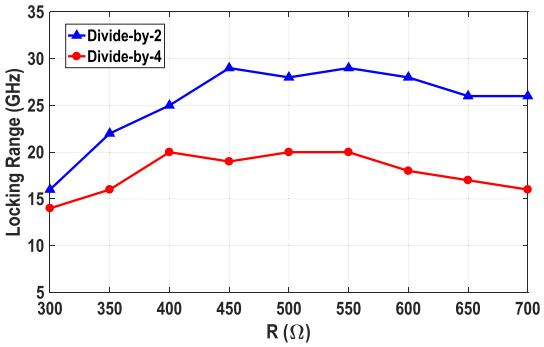

FIGURE 11. Simulated LR versus R when $I_{SS1} = I_{SS2} = 800$ μA, $|I_{inj}| = 400$ μA, $W_{MD} = W_{MN} = 8$ μm. All transistors are minimal length.

Also,

$$|v_O| = R \cdot real\,(I_T)\,. \tag{16}$$

Hence, the following condition must be satisfied:

$$real\,(I_T) \geq \frac{V_{Omin}}{R} \tag{17}$$

The LR of CML dividers can be expressed as

$$\text{LR}=\frac{\tan(\varphi_{max})}{RC} - \frac{\tan(\varphi_{min})}{RC} \tag{18}$$

where C consists of parasitic capacitances at the output. It can be expressed as $C = C_{DB1}+C_{GD1}+C_{GS2}+C_{DB2}+4C_{GD2}+C_{Load}$. The subscripts "1" and "2" represent the parasitic capacitances of M_D and M_N, respectively. Since every stage of the circuit is the same, C_{Load} is approximately equal to C_{GS1}. C is difficult to design accurately, therefore the main determinants of LR in the design are $\Delta\varphi$, φ_0, and R. The direct way to enhance $\Delta\varphi$ is to increase the input signal power. $\Delta\varphi$ is positively related to $|I_{inj}|$. Near ω_{OSC}, the CML dividers can work with a small input signal. Beyond the point of ω_{OSC}, the required input signal must increase, thus forming a "V" shaped sensitivity curve. However, as $|I_{inj}|$ increases, the value of φ_{max} is limited by V_{Omin}/R (see Fig. 8(a)). When $|I_{inj}|$ is relatively small and constant, $\Delta\varphi$ can also be improved by lowering $|I_{OSC}|$ as shown in Fig. 8(b). In other words, if the input signals have the same power, the larger the I_{SS}, the smaller the bandwidth. The simulation results confirm this analysis conclusion as shown in Fig. 10.

Based on the previous analysis, the increase of φ_0 must be achieved by increasing α. In this case, the input locked circle will move to the straight line V_{Omin}/R. φ_{max} is almost unchanged and φ_{min} increases, which means $\Delta\varphi$ decreases and so does LR.

Comparing to the influence of $\Delta\varphi$ and φ_0 on LR, R affects LR in two different ways. On one hand, the increase of R relaxes the restrictions of φ_{max}. On another hand, a greater R leads to a steeper phase-frequency curve of RC which means a narrower LR as depicted in Fig. 9. When R is relatively small, the former way is dominant, and LR increases as R increases. As R becomes larger, the increase of R is no longer helpful for the improvement of LR, and it also reduces the operating frequency. The simulation results are presented in Fig. 11.

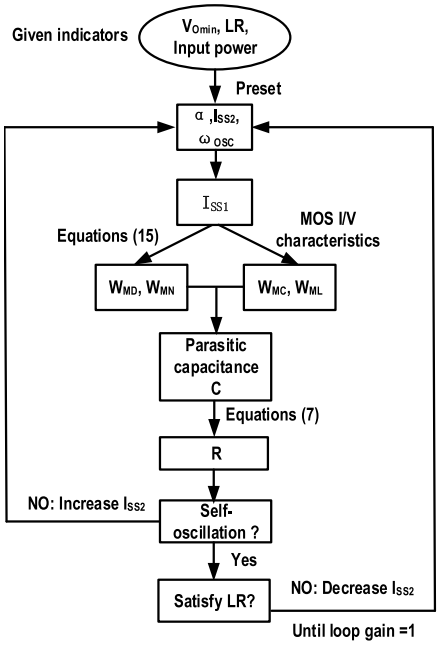

FIGURE 12. The proposed CML design and optimization flow.

TABLE 1. Device dimensions of the CML dividers.

	/2	/4
M_N	6 μm/60 nm	6.5 μm/60 nm
M_D	6 μm/60 nm	6.5 μm/60 nm
M_C	30 μm/60 nm	16 μm/60 nm
M_L	30 μm/60 nm	16 μm/60 nm
R	320 Ω	310 Ω

III. CIRCUITS IMPLEMENTATION

Locking range, operating frequency and power consumption of CML dividers are correlated parameters. we need to make a trade-off between these parameters for certain optimization targets. Generally, the design requirement is to achieve the required locking range and output voltage V_{Omin} with a minimum of power consumption P_{DC}. Then P_{DC} can be

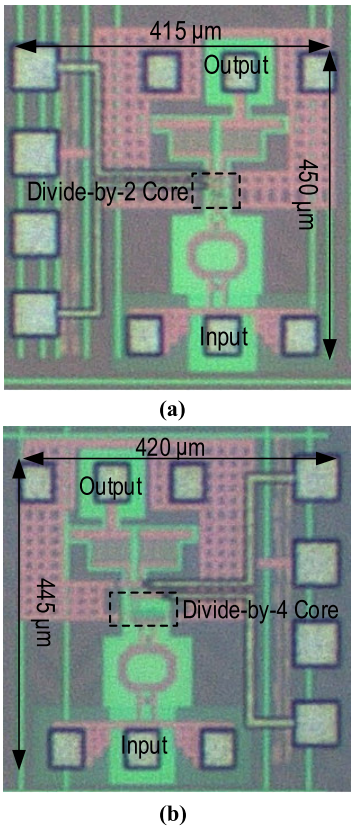

FIGURE 13. Chip micrographs of divide-by-2 and divide-by-4 circuits. (a) Divide-by-2 circuit. (b) Divide-by-4 circuit.

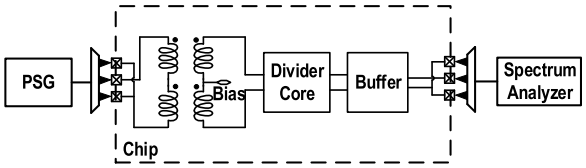

FIGURE 14. Complete test-chip diagram.

expressed as

$$P_{DC} = n \cdot VDD \cdot I_{SS2}\,(1+\alpha) \tag{19}$$

P_{DC} can be optimized by lowering I_{SS2} and α. Assume that LR, V_{Omin}, and input power are given design requirements.

The systematic design methodology of CML dividers is summarized as follows. 1) Preset initial values of I_{SS2},ω_{OSC}, and α. 2) Select the size of M_D and M_N satisfying (15) to ensure that M_D and M_N can be fully switched. Determine the size and the bias voltage of M_C and M_L according to the I/V characteristics. 3) Calculate parasitic capacitance C. 4) R can be obtained according to Eq. 7. 5) Verify that the circuit is capable of self-oscillation, if not, increase I_{SS2} and redesign. 6) Verify that the LR meets design requirements until the minimum I_{SS2} is obtained and that the circuit has sufficient gain to oscillate as depicted in Fig. 12. 7) Smaller α can be obtained through iterative design to achieve lower power consumption.

Based on the proposed methodology, divide-by-2 and divide-by-4 blocks are realized in CMOS 65-nm technology.

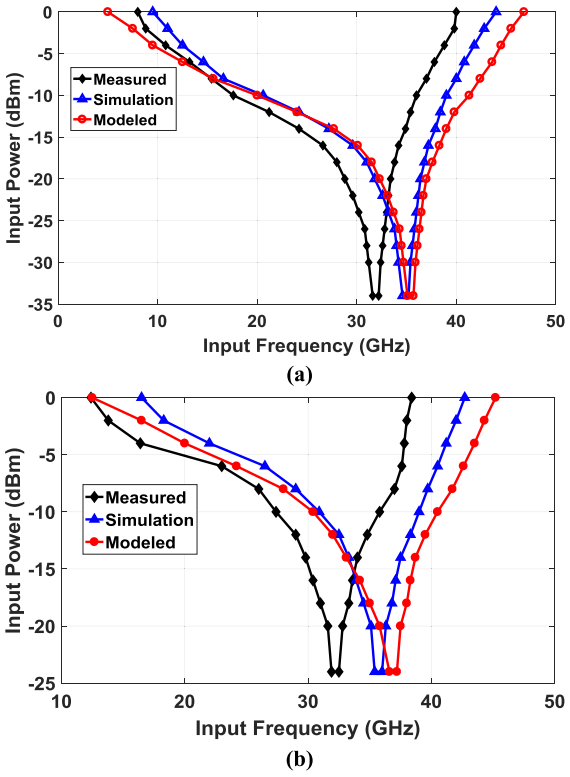

FIGURE 15. The theoretical analysis, simulation and measured sensitivity curves of divide-by-2/4 circuits. (a) Divide-by-2 circuit. (b) Divide-by-4 circuit.

For covering the mm-Wave 5G band, the maximum operating frequencies of divide-by-2/4 blocks are designed to be 40 GHz and 38 GHz respectively. The I_{SS1} and I_{SS2} of divide-by-2 block are both 670 μA, while I_{SS1} and I_{SS2} of divide-by-4 block are both 750 μA. The dimensions for all the transistors are summarized in TABLE 1. For testing purposes, an ultra-broadband transformer-based matching network with -3 dB loss is added at the input of each divider while an inverter-based buffer amplifier is added at the output.

IV. MEASUREMENT RESULTS

Fabricated in 65-nm CMOS, Fig. 13 shows the chip micrographs. The core areas of divide-by-2 and divide-by-4 circuits are $25 \times 33\mu m^2$ and $47 \times 28\mu m^2$ respectively. The implemented dividers have been tested on a high-frequency probe station. In Fig. 14, the complete test-chip diagram is shown. The each divider is followed by a buffer driving the 50 Ω impedance of the spectrum analyzer. The high-frequency input signals are connected through GSG probes and a transformer-based matching network used to convert input signals from single - to differential. The input power is varied from -40 to 0 dBm. The sensitivity curves of dividers based on theoretical analysis, simulation and measurement are depicted in Fig. 15. The results of theoretical analysis and simulation have a good fit. Due to process variations, the measured results deviate from the simulation results. A locking range from 8 to 40 GHz divide-by-2 block and a

TABLE 2. Performance comparison with state-of-the-art CMOS dividers.

Ref.	Scheme	f_{in}/f_{out}	Tech. Node (nm)	P_{in} (dBm)	LR (GHz)	P_{DC} (mW)	Area (mm^2)	FoM (dB)	VDD (V)
[10]	CML	2	22	0	21.3-30	11	0.0008	20.29	0.86
[11]	CML$^{\Delta}$	2	45	0	1-60	9.6	0.01	187.4	1.2
[12]	CML	2	45	0	7.6-23	11	0.0017	21.42	1.0
[3]	ILFD-CML	4	130	0	13.5-30.5	7.3	0.33	102.47*	1.4
[13]	CML	4	90	0	13.2-18.4	10.8	0.5688	15.2*	1.2
[14]	ILFD	4	65	0	13.4-21.3	3.9	0.003	70.29*	1.2
This work#1	CML	2	65	0	8-40	4.6	0.0008	166.96	1.0
This work#2	CML	4	65	0	12.4-38.4	7.5	0.0013	176.1*	1.0

* The dc power is normalized to two-phase output.
Δ The inductive peaking is utilized.

$$\text{FoM} = \frac{\text{LR (GHz)} * \text{Center Frequency (GHz)}}{P_{DC}\ \text{(mW)} * P_{in}\text{(mW)}}$$

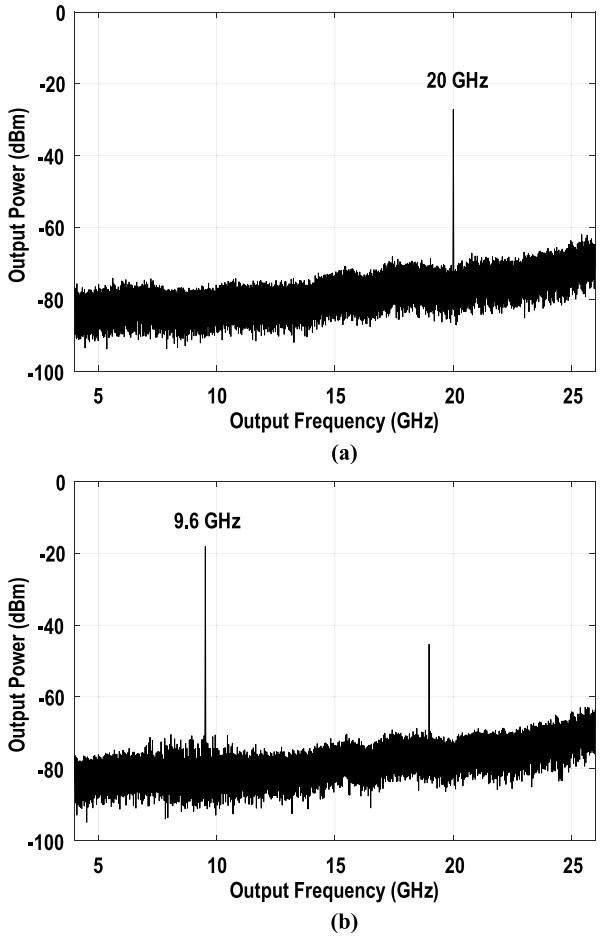

FIGURE 16. The measured spectrums of output signal. (a)Divide-by-2 block with 40 GHz input. (b) Divide-by-4 block with 38.4 GHz input.

locking range from 12.4 to 38.4 GHz divide-by-4 block are achieved, consuming 4.6 mW and 7.5 mW of P_{DC} respectively. The measured spectrums of the maximum frequency

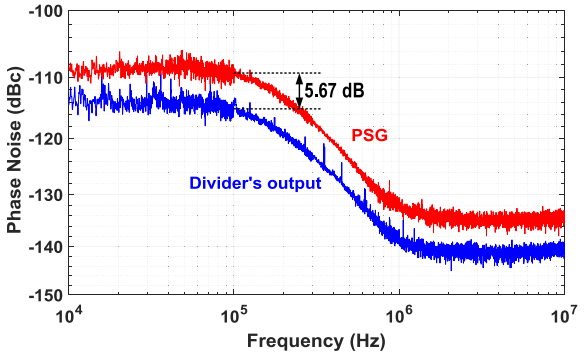

FIGURE 17. Divide-by-2 phase noise of input signal at 24 GHz and output signal at 12 GHz.

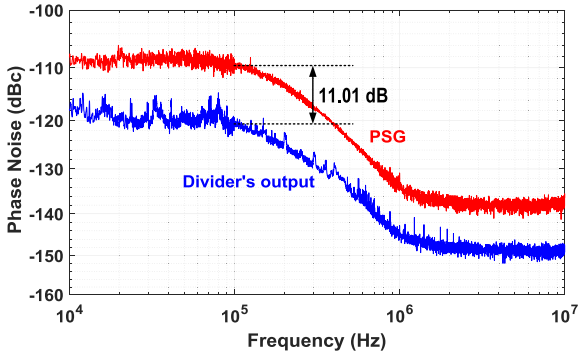

FIGURE 18. Divide-by-4 phase noise of input signal at 24 GHz and output signal at 6 GHz.

of output with 0 dBm input signal are depicted in Fig. 16. Fig. 17 and Fig. 18 compare the measured phase noise of divide-by- 2 and divide-by-4 respectively with a 24 GHz input signal. The output phase noise is 5.67 dB and 11.01 dB lower respectively at 100 kHz frequency offset, which is very close to the theoretical value of $20\log_{10}$ (n).

In TABLE 2, this work is compared with prior-art frequency dividers in CMOS. The proposed dividers achieve

competitive FoM [15] with the smallest core area for the same f_{in}/f_{out}, verifying the effectiveness of the proposed design methodology.

V. CONCLUSION

This work addresses the geometric analysis and systematic design of CML static frequency dividers. The optimum conditions of self-oscillation frequency and LR have been derived to achieve wideband low-power dividers. Fabricated in 65-nm CMOS technology, the divide-by-2/4 blocks operate from 8 to 40 GHz and from 12.4 to 38.4 GHz respectively with 0 dBm input signal and consume 4.6 mW and 7.5 mW of P_{DC} respectively.

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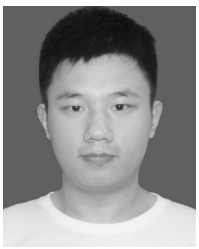

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