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A High Current Efficiency Two-Stage Amplifier With Inner Feedforward Path Compensation Technique

YAPING XIN, XIAO ZHAO, BORAN WEN, (Student Member, IEEE), LIYUAN DONG, (Student Member, IEEE), AND XIAOLONG LV
School of Geophysics and Information Technology, China University of Geosciences (Beijing), Beijing 100083, China

Corresponding author: Xiao Zhao (zhaoxiao@cugb.edu.cn)

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ABSTRACT A high current efficiency two-stage amplifier with inner feedforward path compensation (IFPC) technique is proposed in this paper. To improve the current utilization of the whole structure, the recycling folded cascode amplifier (RFC) is adopted as the first stage, and the inner feedforward path which is used to eliminate the non-dominant pole is composed of the input stage of RFC and the tail current transistor of the second stage amplifier. By using the IFPC technique, the proposed amplifier achieves an extended gain-bandwidth (GBW) and sufficient phase margin (PM) compared to that of the two-stage amplifier using single Miller compensation (SMC). Moreover, this compensation technique avoids extra power consumption since it does not require additional circuits. The proposed two-stage IFPC amplifier was fabricated in a 0.18 μm CMOS technology and the chip area of it is about 0.076mm^2. The simulated open loop AC response shows the DC gain, GBW, and PM are 130dB, 2.01MHz, and 58.3°, respectively. Measured results of transient response show when driving a 120pF load capacitance, the proposed amplifier achieves 368ns average 1% settling time, and about 1.56V/μs average slew rate (SR). Note that under the condition of 1.8V power supply, the power consumption is only 108μW, proving the proposed two-stage IFPC amplifier can achieve high current efficiency while maintaining stability.

INDEX TERMS Two-stage amplifier, current efficiency, frequency compensation, inner feedforward path.

I. INTRODUCTION

The widespread application of portable electronic equipment makes low power consumption become an inevitable development trend of amplifiers. Reducing the supply voltage is an effective method to decrease power consumption. However, with the decrease of the supply voltage, the inherent gain of the amplifiers will also deteriorate. Consequently, how to design an amplifier with high current efficiency and sufficient DC gain is worth exploring. Although the single-stage amplifiers have high speed, they are no longer suitable for electronic devices operating at low voltage since their DC gain can not meet the requirement. The multi-stage amplifiers have the advantages of high DC gain and large voltage swing, the main issue is that several high impedance nodes contained inside introduce multiple low frequency poles, resulting in system instability under closed-loop condition [1]–[8]. Obviously, frequency compensation is mandatory for systems with stability problem and the difficulty degree of it promotes with the increase of gain stage. Diverse frequency compensation techniques have been proposed in previous works for a multi-stage amplifier to ensure its stability [9]–[17]. However, complicated circuit structure and tedious transfer function calculation limit the application of multi-stage amplifiers [17]–[20]. Therefore, two-stage amplifiers become the optimum choice for the low power design [21], [22] owing to this structure can obtain the favorable tradeoff between DC gain, speed, and the complexity of the compensation techniques.

Under these circumstances, the frequency compensation of two-stage amplifiers becomes an issue worthy discussion [23], [24]. As the most commonly used compensation method, the single Miller compensation (SMC) can move the dominant pole to low frequency and the non-dominant pole to high frequency, respectively [25]. However, the drawback can not be neglected of this method is that the presence

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of the right-half-plane (RHP) zero leads to the significant decrease of phase margin (PM) [26]. What's more, the gain-bandwidth (GBW) of two-stage SMC amplifiers is one-half of that of single-stage amplifiers [27]. To solve the problem of RHP zero in the two-stage SMC amplifier, several techniques have been proposed in the past years [28]–[34]. For example, the scheme called single Miller compensation with a nulling resistor (SMCNR) which can reduce the current flowing through feedforward path by connecting a nulling resistor in series with the miller capacitance was proposed in [12]. Although this method can place RHP zero at high frequency, the lager resistance takes up excessive extra area. The compensation method using a voltage buffer can be used to eliminate the RHP zero. Nevertheless, this method limits the output swing. Note that neither of the above technologies can enhance GBW since the frequency of the non-dominant pole is not improved compared with that of the two-stage SMC amplifier. Some modified techniques based on voltage buffer compensation can enhance GBW were proposed in previous works [31], [32]. For example, the method which uses flipped voltage follower (FVF) as a voltage buffer not only achieves the same compensation effect but also improves GBW compared with conventional voltage buffer compensation [31]. What's more, in [32], the proposed method achieves a high GBW by adding a gain stage in series with the voltage buffer. However, these improved methods cannot get rid of the limitation of output swing. In order to overcome the shortcomings of the SMCNR and the voltage buffer compensation, the SMC scheme with a current buffer or a fast feedforward path was proposed in [18], [33]–[35]. The current buffer is added to the feedback path leading to the non-dominant pole is placed at high frequency. As for the two-stage SMC amplifier with a fast feedforward path, it eliminates the non-dominant pole by creating a left-half-plane (LHP) zero. Therefore, the GBW of the amplifier using the above two methods obtain a significant improvement compared with that of the traditional two-stage SMC amplifier. However, these two methods mentioned above require extra power consumption since both of them achieved by increasing additional gain stage.

To achieve high current efficiency while ensuring high GBW and sufficient phase margin, this paper proposes a performance-enhanced structure called two-stage inner feedforward path compensation (IFPC) amplifier. The proposed amplifier obtains high current efficiency for the following two reasons, one is that the recycling folded cascode amplifier (RFC) is used as the first stage for it can improve current utilization compared with conventional amplifier [36], the other is that the proposed compensation scheme does not consume extra power since the inner feedforward path of the proposed amplifier consists of the input stage of RFC and the tail current transistor of the second stage amplifier. Besides, with appropriate circuit design, the proposed architecture is able to create a LHP zero which can be used to eliminate the non-dominant pole. As a result, the two-stage amplifier with inner feedforward path achieves a significant extension of GBW and sufficient PM. Therefore, compared with the two-stage amplifiers using the compensation methods mentioned above, the proposed amplifier is more suitable operates at low power consumption condition.

The structure of this paper is as follows. Section II not only shows the issues of the two-stage SMC amplifier but also explicit introduces the main idea of the IFPC scheme. In addition, the analysis of the slew rate (SR) is also shown in this section. In section III, the simulated and measured results of the two-stage IFPC amplifier are given, and the performance comparisons between the proposed amplifier and other amplifiers mentioned in previous works are presented. Finally, section IV gives the conclusions.

II. TWO-STAGE AMPLIFIER WITH INNER FEEDFORWARD PATH COMPENSATION

The main content of this section is as follows. It briefly introduces the problems of the two-stage SMC amplifier and gives its topology. The circuit implementation of the proposed two-stage amplifier with inner feedforward path compensation is given. In order to analyze the proposed amplifier in detail, this section presents its transfer function and the conditions for eliminating the RHP zero and the non-dominant pole can be derived. What's more, the analysis of SR is given at the end of this section.

A. TRADITIONAL SIMPLE MILLER COMPENSATION

The topology of the two-stage SMC amplifier is shown in FIGURE 1. This compensation method is extremely classical and basic, and a lot of compensation methods are extended on this basis. Therefore, it is obliged to analyze the two-stage SMC amplifier deeply. G_{m1} and G_{m2} represent the transconductances of the first and the second stage amplifiers, respectively. The C_c is the compensation capacitor, one terminal of which is connected to the output of the first stage amplifier, and the other terminal is connected to that of the second stage amplifier. The parasitic capacitor of the first stage amplifier is C_1 and the C_L represents the load capacitance of the two-stage amplifier. R_1 and R_2 are the output resistances of the first and the second stage amplifiers, respectively. The transfer function of the two-stage SMC amplifier can be expressed as [9]

$$\frac{V_{out(s)}}{V_{in_{(s)}}} = \frac{G_{m1}G_{m2}R_1R_2(1 - s\frac{C_c}{G_{m2}})}{(1 + sC_cG_{m2}R_1R_2)(1 + s\frac{C_L}{G_{m2}})} \tag{1}$$

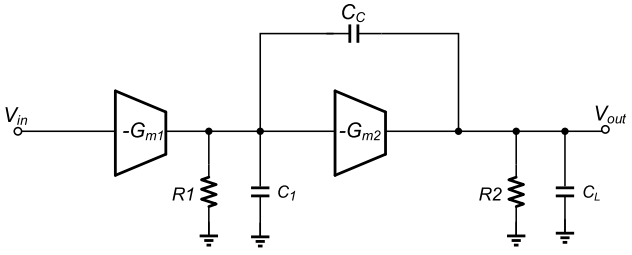

FIGURE 1. Topology of the two-stage SMC amplifier.

From this expression, it can be concluded that there is a dominant pole $p_{|-3dB|}$, a non-dominant pole p_1, and a RHP zero z_1 in this structure, which are expressed as

$$p_{|-3dB|} = -\frac{1}{C_c G_{m2} R_1 R_2} \tag{2}$$

$$p_1 = -\frac{G_{m2}}{C_L} \tag{3}$$

$$z_1 = \frac{G_{m2}}{C_c} \tag{4}$$

Thus, the GBW of the two-stage SMC amplifier can be given as

$$GBW = \frac{G_{m1}}{C_c} \tag{5}$$

In order to obtain sufficient PM, GBW is usually set to be half of p_1 and the expression that the value of compensation capacitor must satisfy is

$$C_c = 2(\frac{G_{m1}}{G_{m2}})C_L \tag{6}$$

Therefore, the GBW can be also expressed as

$$GBW = \frac{1}{2}(\frac{G_{m2}}{C_L}) \tag{7}$$

It can be clearly seen from (7) that the GBW of the two-stage SMC amplifier is equal to one-half of that of the single-stage amplifier. As for PM, it can be evaluated by the following expression [9]

$$PM = 180^\circ - tan^{-1}(\frac{GBW}{p_{|-3dB|}}) - tan^{-1}(\frac{GBW}{p_1}) - tan^{-1}(\frac{GBW}{z_1}) \approx 63^\circ - tan^{-1}(\frac{G_{m1}}{G_{m2}}) \tag{8}$$

From this expression, it can be concluded that the PM of the two-stage SMC amplifier is affected by the RHP zero. Therefore, it is essential to find a method to improve the GBW and eliminate the RHP zero.

B. CIRCUIT IMPLEMENTATION OF THE PROPOSED AMPLIFIER

FIGURE 2 shows the circuit implementation of the proposed two-stage amplifier using inner feedforward path compensation, in which the RFC is used as the first stage amplifier for its high current efficiency. The M0 is the tail current transistor. M1, M1N, M2, and M2N form the input stage. The quiescent current flowing through them is equal and the value of it is I_b. The ratio of the two current mirrors, including M3: M3N and M4: M4N, is K:1. To enable the current mirror to accurately replicate the current, the drain potentials of M3(N) and M4(N) should be equal. Thus, M5, M6, M11, and M12 are added. The transistor M13 is the second stage amplifier whose output is connected with the output of RFC amplifier through compensation capacitor C_c. The gate of M14 is connected to that of M3N to form a current mirror and the ratio of it is M:1. The input signal is amplified by M14 after passing through input stage. Thus, the input

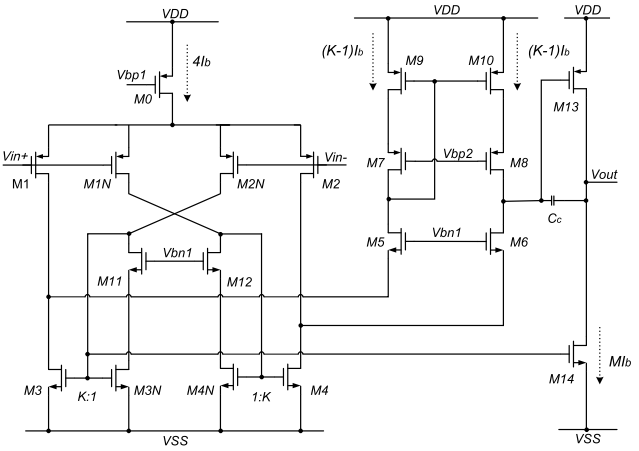

FIGURE 2. The circuit schematic of the proposed amplifier.

stage of RFC and the tail current transistor of the second stage amplifier form a fast feedforward signal path. This fast feedforward signal path between input and output is called inner feedforward path.

C. TOPOLOGY OF THE PROPOSED AMPLIFIER

In order to explain the principle of the proposed circuit more intuitively, this section gives the topology structure of the two-stage IFPC amplifier which is shown in FIGURE 3. In addition, the transfer function of the proposed amplifier and the conditions for eliminating the RHP zero and non-dominant pole are given.

Obviously, there are several poles in the amplifier which not affect the GBW owing to they are at high frequency compared with the dominant pole and the first non-dominant pole. In order to simplify the calculation, the poles inside the amplifier are omitted in the calculation of the transfer function. Under this assumption, the transfer function of the proposed two-stage IFPC amplifier is

$$H(s) = \frac{A_{dc}(1 + \frac{s}{z_1})}{(1 + \frac{s}{p_{|-3dB|}})(1 + \frac{s}{p_1})} \tag{9}$$

where A_{dc} is the DC gain and its value can be evaluated by the following expression:

$$A_{dc} = (1 + k) g_{m1} g_{m13} R_1 R_2 \tag{10}$$

What's more, $p_{|-3dB|}$ is the dominant pole and it can be given as

$$p_{|-3dB|} = \frac{1}{C_c g_{m13} R_1 R_2} \tag{11}$$

The non-dominant pole and the zero are represented by p_1 and z_1 respectively. They are given as

$$p_1 = \frac{g_{m13}}{C_L} \tag{12}$$

$$z_1 = \frac{g_{m1} g_{m13}}{(g_{mf} - g_{m1}) C_c} \tag{13}$$

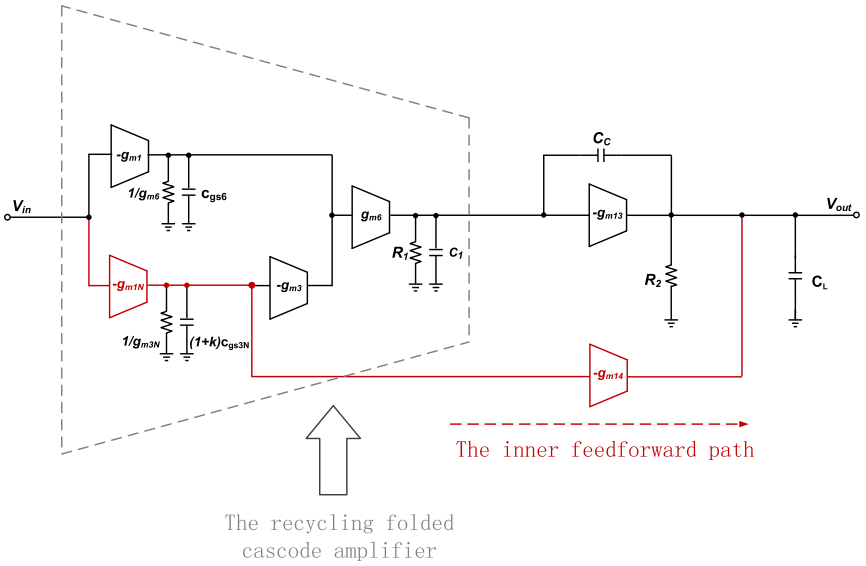

FIGURE 3. Topology of the proposed amplifier.

where g_{mf} represents the equivalent transconductance of the inner feedforward path, and the value of it can be given as

$$g_{mf} = g_{m1N}\frac{1}{g_{m3N}}g_{m14} \tag{14}$$

As mentioned above, the size ratio of transistors M14 and M3N is M. Therefore, the value of g_{mf} can be further expressed as

$$g_{mf} = Mg_{m1N} = Mg_{m1} \tag{15}$$

Equation (13) can be also expressed as

$$z_1 = \frac{g_{m13}}{(M-1)C_c} \tag{16}$$

From this expression, it can be concluded that when the value of M is less than 1, z_1 is a RHP zero. And when M is set to 1, the zero of the amplifier is eliminated. Note that once M is greater than 1, z_1 will become a LHP zero. Obviously, if the condition $p_1 = z_1$ can be satisfied, then the non-dominant pole p_1 can be canceled. The relationship can be further expressed by the following equation:

$$\frac{g_{m13}}{C_L} = \frac{g_{m13}}{(M-1)C_c} \tag{17}$$

Therefore, the value of M must meet

$$M = \frac{C_L}{C_c} + 1 \tag{18}$$

In this case, the GBW of the proposed amplifier can be given by

$$GBW = \frac{(1+k)g_{m1}}{C_c} \tag{19}$$

Note that after the original first non-dominant pole p_1 is canceled, the pole p_2 introduced by the internal structure of the amplifier becomes the new first non-dominant pole. The maximum value that GBW can achieve is greatly improved since its value is limited by p_2 which is at higher frequency than p_1. Therefore, the proposed two-stage IFPC amplifier can achieve an extended GBW compared with the two-stage SMC amplifier.

What affects the PM of the proposed amplifier is the dominant pole $p_{|-3dB|}$ and the pole p_2. The value of PM can be evaluated by

$$\begin{aligned} PM &= 180^\circ - tan^{-1}(\frac{GBW}{p_{|-3dB|}}) - tan^{-1}(\frac{GBW}{p_2}) \\ &= 90^\circ - tan^{-1}(\frac{GBW}{p_2}) \end{aligned} \tag{20}$$

D. SLEW RATE OF THE PROPOSED AMPLIFIER

In order to analyze the large signal response of the proposed amplifier, suppose a large positive step is applied to *Vin*+, M1(N) will turn off and the current flowing through M4N is zero. Both M2 and M4 will turn off, leading to the current flowing through M2N is $4I_b$. Then this current is magnified to $4KI_b$ after passing through the current mirror M3:M3N. Thus, the output current of the first stage amplifier is $4KI_b$, and the SR_1+ of the first stage amplifier can be expressed as

$$SR_1+ = \frac{4KI_b}{C_c} \tag{21}$$

What's more, for the second stage of the proposed two-stage IFPC amplifier, C_C and C_L discharge at the same time, and the current generated by the discharge of these two capacitors is equal to $4MI_b$. Therefore, the value of SR_2- is

$$SR_2- = \frac{4MI_b}{C_c + C_L} \tag{22}$$

The value of SR− of the proposed amplifier is limited to the minimum value between SR_1+ and SR_2-, this relationship

can be expressed as

$$SR- = min\{SR_1+, SR_2-\} \tag{23}$$

And the condition for SR− to get maximum value is given as

$$\frac{4KI_b}{C_c} = \frac{4MI_b}{C_c + C_L} \tag{24}$$

When a large negative voltage is applied to *Vin*+, for the first stage of the proposed amplifier, the value of SR_1- is equal to that of SR_1+. Thus, the value of SR_1- can be expressed as

$$SR_1- = \frac{4KI_b}{C_c} \tag{25}$$

The output current of the second stage amplifier is I_{DS13}, this current needs to charge compensation capacitance C_c and load capacitance C_L at the same time. Therefore, the value of SR_2+ can be given as

$$SR_2+ = \frac{I_{DS13}}{C_c + C_L} \tag{26}$$

Obviously, the SR+ of the proposed two-stage IFPC amplifier is limited by SR_1-, and it can be expressed as

$$SR+ = min\{SR_1-, SR_2+\} = \frac{4KI_b}{C_c} \tag{27}$$

III. RESULTS AND PERFORMANCE COMPARISONS

The proposed two-stage IFPC amplifier is fabricated in a CMOS 0.18 μm process and the supply voltage of it is 1.8 V. What's more, the quiescent current I_b is set to 2.5μA, the values of K and M are 3 and 16 respectively, and the value of C_c is 8pF. Thus, the total current consumption of the proposed amplifier is 60μA. The area of this amplifier is about 0.076mm^2 and its chip microphotograph is shown in FIGURE 4.

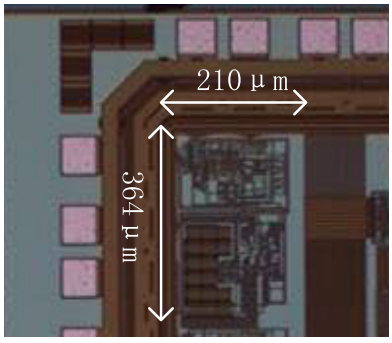

FIGURE 4. Microphotograph of the proposed amplifier.

The measured platform of this amplifier including a EDUX 1002G digital oscilloscope and a DC power supply DP831A. The oscilloscope has two functions here, one is to provide the input signal for the amplifier, and the other is to measure the output signal of the amplifier. Measured indicators include closed-loop AC response, transient response, and total harmonic distortion (THD).

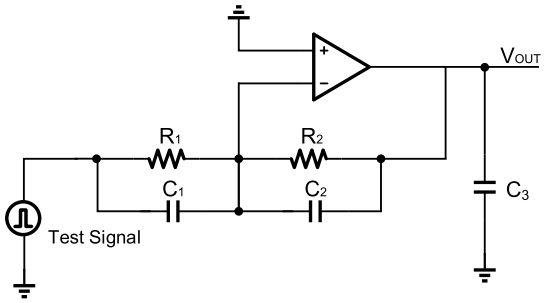

FIGURE 5. The test setup used to measure the performance of the proposed amplifier.

The test setup which is used to measure the performance of the proposed amplifier is given in FIGURE 5. In order to obtain high output impedance, the values of the load resistance R_1 and R_2 are 1MΩ. What's more, the capacitance C_1 and C_2 are set to 40pF. Note that the Keysight N2142A active probe has a capacitance C_3 of 100pF. Thus, the total load capacitance is 120pF.

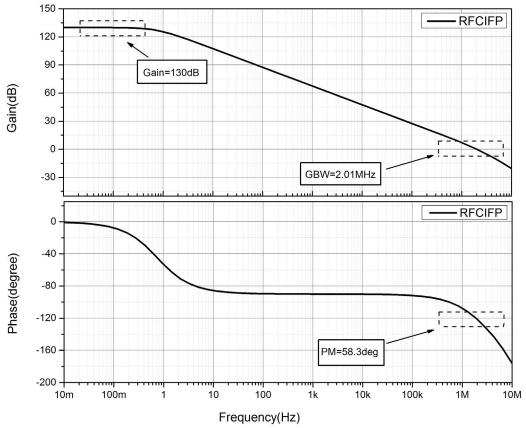

FIGURE 6. Simulated open-loop AC response of the proposed amplifier.

FIGURE 6 gives the simulated open-loop AC response of the proposed two-stage IFPC amplifier. The simulation is carried out under the condition of unity-gain configuration. The DC gain, GBW and PM are 130dB, 2.01MHz and 58.3°, respectively. The value of PM is less than 90° due to the influence of the poles introduced by the internal structure of the amplifier.

FIGURE 7 shows the measured closed-loop AC response of the proposed amplifier. It can be concluded that the 3dB bandwidth of this amplifier is about 1MHz. Note that the closed-loop feedback coefficient of the test configuration is 0.5. Therefore, the GBW of the proposed amplifier is about 2MHz. That demonstrates the measured result of the GBW is consistent with its simulated result.

In order to obtain the small signal transient response of the proposed amplifier, a square wave at 100KHz with a peak-to-peak value of 100mV is added to *Vin*−. The measured results are given in FIGURE 8, showing the average 1% settling time is 368ns.

TABLE 1. Comparisons with prior works.

Parameter	[22]	[26]*	[35]*	[12]*	[10]	[16]	This work
Year	2011	2014	2015	2017	2019	2019	2019
Technology (μm)	0.13	0.065	0.045	0.13	0.18	0.065	0.18
Supply voltage (V)	1.2	1.2	1.4	2.4	1.8	1.2	1.8
Power (mW)	0.11	0.75	0.25	0.01961	0.85	12.6	0.108
Load Capacitance(pF)	>5.5	1	5	0.05	5	2	120
Architecture	2^{st}	2^{st}	2^{st}	2^{st}	3^{st}	3^{st}	2^{st}
Area(mm^2)	0.012	-	-	-	0.45	0.04	0.076
DC gain(dB)	>70	-	88	88.61	105.5*	72.9	130*
GBW(MHz)	35	780	6.8	111.2	231.77	2410	2
phase margin($^\circ$)	>45	-	68	68.56	53*	82.6	58.3*
Average SR (V/μs)	19.5	124	5.4	90.53	13.25	1725	1.56
Average 1% Settling Time(ns)	-	-	-	-	99	1.41	368
Input Referred Noise@1MHz (nV/$\sqrt{Hz}$)	-	-	-	-	194.244*	-	37.25*
FoM_s $(MHz \cdot pF/mW)$	1750	1040	136	283.5	1214	382.5	2222.22
FoM_L $((V/us) \cdot pF/mW)$	975	165	108	230.8	78	273.8	1733.33

* Simulation Results

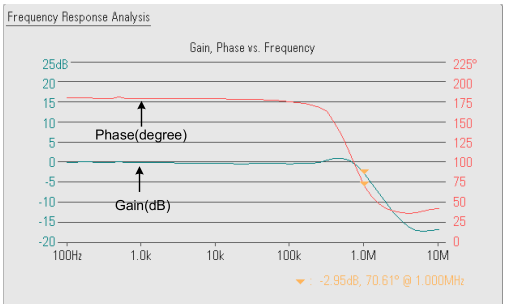

FIGURE 7. Measured closed-loop AC response of the proposed amplifier.

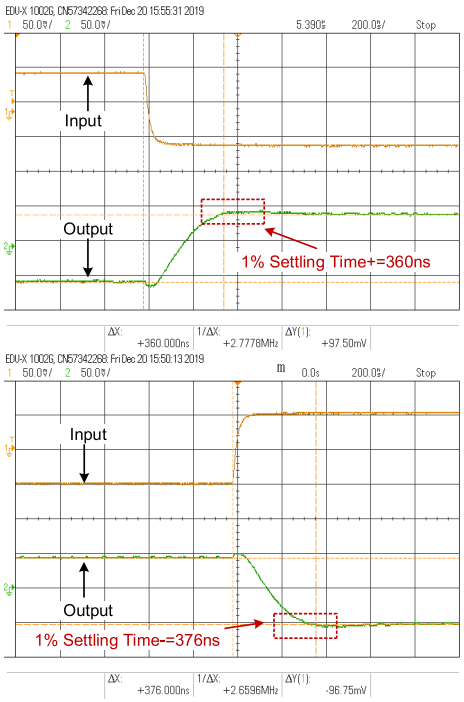

FIGURE 8. Measured small signal transient response of the proposed amplifier.

As for the large signal transient response, the measured result of it is shown in FIGURE 9. The input signal is a square wave at 100KHz with a peak-to-peak value of 400mV and the value of average SR is about 1.56V/μs.

The THD is a significant indicator which reflects the linearity of the amplifier. It can be measured by fast Fourier transform (FFT) analysis of an oscilloscope. When a sine wave with a frequency of 20kHz and amplitude of 160mV_{pp} is applied to $Vin-$, the value of the THD is -68.125dB as shown in FIGURE 10.

The noise performance of the proposed amplifier can be characterized by simulation. FIGURE 11 shows power spectral density (PSD) of the equivalent input referred noise. Note that the PSD is 37.25nV/$\sqrt{Hz}$ at 1MHz.

In order to demonstrate that the proposed amplifier can achieve high current efficiency, the performance comparison with the prior works are given in TABLE 1. In general, the current efficiency of the amplifier can be characterized by Figure of Merit (FoM). The comparison parameters include FoM_s and FoM_L and their expressions are (28) and (29) respectively.

$$FoM_s = \frac{GBW \cdot C_L}{power} \tag{28}$$

$$FoM_L = \frac{SR \cdot C_L}{power} \tag{29}$$

where $power$ represents the power consumption consumed by amplifiers. TABLE 1 shows the proposed two-stage IFPC amplifier has larger FoM_s and FoM_L compared with other amplifiers which are reported in prior works. Thus, the current efficiency of the proposed amplifier is higher than other existing amplifiers shown in TABLE 1. Moreover, the DC gain of the proposed amplifier is superior to other amplifiers, and its value is 130dB.

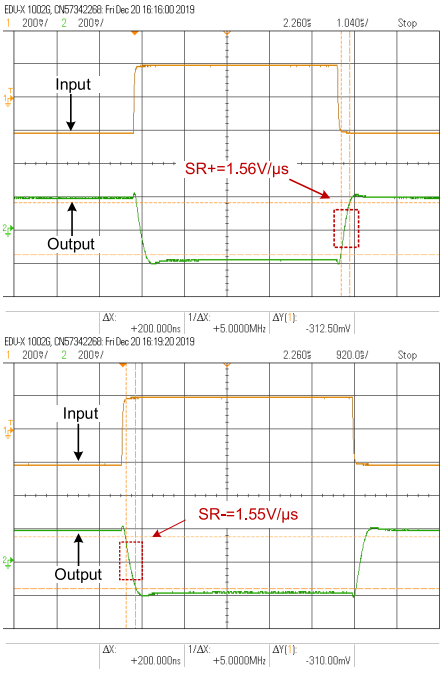

FIGURE 9. Measured large signal transient response of the proposed amplifier.

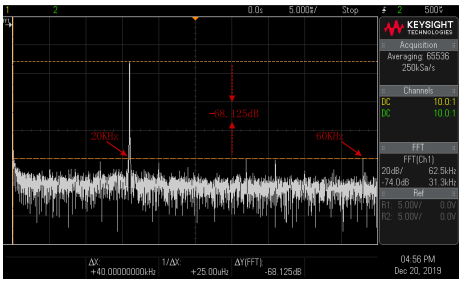

FIGURE 10. Measured FFT spectrums of the proposed amplifier.

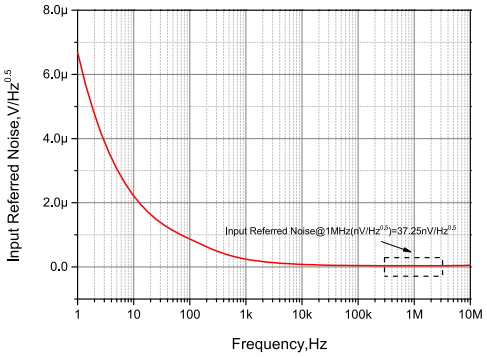

FIGURE 11. Equivalent input referred noise power spectral density.

IV. CONCLUSION

This paper presents a structure based on the two-stage SMC amplifier, which employs the inner feedforward path compensation technique. Use the LHP zero generated by the inner feedforward path which is composed of the input stage of RFC and the tail current transistor of second stage amplifier to eliminate the non-dominant pole, leading to an extended GBW and sufficient PM. The simulated open loop AC response shows that the proposed two-stage amplifier achieves 2.01MHz GBW and 58.3° PM. That demonstrates the proposed frequency compensation method is effective. Besides, this frequency compensation method avoids extra power consumption since it does not require additional circuits. Compared with the previous works, the values of FoM_s and FoM_L of the proposed amplifier have been greatly improved, proving the two-stage IFPC amplifier presented in this paper has high current efficiency.

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YAPING XIN was born in Shandong, China, in 1996. She received the B.E. degree in electronic information engineering from the Qingdao University of Technology, in 2018. She is currently pursuing the M.S. degree in electronic and communication engineering with the China University of Geosciences (Beijing), China. She has been studying the chopper and auto-zero technology. Her current researches are mainly about low noise instrumentation amplifier and high-efficiency low-dropout regulator.

XIAO ZHAO was born in Shandong, China, in 1985. He received the B.S. degree in electronics and communication engineering from Qingdao University, in 2006, the M.S. degree in electronics science from Beihang University, Beijing, China, in 2009, and the Ph.D. degree in electronics science from Tsinghua University, Beijing, in 2013. Since 2013, he has been an Assistant Professor with the Instrumentation Science and Technology Department, China University of Geosciences, Beijing. From 2017 to 2018, he was a Visiting Scholar with the College of Electrical Engineering and Computer Science, Oregon State University, OR, USA, and his advisor is Professor Gabor C. Temes. He is currently an Associate Professor. He is the author of more than 15 articles and holds nine patents. His research interests include low-power amplifier, low-noise instrumentation amplifier, high-precision sigma delta data converter, and high-efficiency low-dropout regulator.

BORAN WEN (Student Member, IEEE) was born in Inner Mongolia, China, in 1994. She received the B.E. degree in measurement and control technology and equipment from the China University of Geosciences (Beijing), in 2017, where she is currently pursuing the master's degree in electronics and communication technology with the Geophysical and Information Technology School. Her current researches are mainly about low noise instrumentation amplifier and high-efficiency low-dropout regulator.

LIYUAN DONG (Student Member, IEEE) was born in Shanxi, China, in 1996. She received the B.E. degree in measuring and controlling technology and instrument from the China University of Geosciences (Beijing), China, in 2018, where she is currently pursuing the M.S. degree in control science and engineering. She has been studying the analog circuit, including high performance OTA and low-dropout regulator. Her current researches are mainly about low noise instrumentation amplifier and adaptively biased low-dropout regulator.

XIAOLONG LV was born in Baoji, Shaanxi, China, in 1993. He received the B.S. degree in measuring and controlling technology and instrument from the China University of Geosciences (Beijing), China, in 2017, where he is currently pursuing the M.S. degree with the School of Geophysics and Information Technology. His majors in electronics and communication engineering. His research interests include mixed signal integrated circuits, high performance OTA, and high-precision sigma delta data converter.