IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 11, 2019, accepted January 10, 2020, date of publication January 17, 2020, date of current version January 27, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2967097

A CMOS RF BeiDou-1 Transceiver for Regional Positioning and Short Message Service Applications

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This work was supported in part by the Shandong Provincial Key Research and Development Plan under Grant 2018GGX101010, and in part by the Shandong Provincial Key Technology Innovation Project under Grant 2019JZZY010203.

ABSTRACT This paper presents a fully integrated CMOS radio-frequency (RF) transceiver for BeiDou-1, a radio determination satellite service system which can provide regional positioning and short message service. The proposed transceiver incorporates a low-IF receiver and a BPSK transmitter to realize a dual-way communication between users and the central control station via satellites. The receiver (RX) RF front-end down-converts the 2491.75 MHz RF signals to a 12.24 MHz IF band with a bandwidth of 8.16 MHz. The complex band-pass filter utilizes passive compensation technique to compensate the phase lag and achieve in-band flatness. The 4.08 Mchip/s baseband signal alternatively selects one of the differential 1615.68 MHz local signals to achieve BPSK modulation for the transmitter (TX). Besides, on-chip low dropout regulators adopt improved power supply rejection ratio techniques by integrating active filtering to obtain stable 1.5 V supply voltages. The transceiver is fabricated in a 130 nm CMOS technology and occupies an area of 5.88 mm^2 with electrostatic discharge circuitry and pads included. The RX channel achieves a 106 dB maximum voltage gain with a 65 dB dynamic range, a 4.95 dB noise figure and a 46 dB image rejection ratio. The output power for the TX ranges from −10 dBm to 5 dBm, with a phase error less than 1.5 degree.

INDEX TERMS BeiDou-1, RF transceiver, radio determination satellite service system, low-IF receiver, complex band-pass filter, on-chip low dropout regulators.

I. INTRODUCTION

The development and employment of the global positioning system (GPS) by the U.S. promotes the demand and potential market of location-based services in a variety of civilian applications [1]–[5]. Many countries have engaged in developing their own satellite navigation systems, such as the global navigation satellite system (GLONASS) from Russia, the Galileo system from the European Union, and the BeiDou satellite navigation system from China. As the first generation of BeiDou system, BeiDou-1 (BD1) is a radio determination satellite service (RDSS) system for regional positioning, user identification, location report and short message service (SMS) applications. The system is realized by a dual-way communication between users and the central control station via geostationary satellites [6], [7].

The associate editor coordinating the review of this manuscript and approving it for publication was Praveen Gunturi.

BD1 is registered in the international telecommunication union with an uplink frequency of 1.62 GHz (L-band) and a downlink frequency of 2.5 GHz (S-band). Unlike the global navigation satellite systems (GNSS) including the GPS, GLONASS, Galileo and the second generation of BeiDou system (''Compass'' or ''BD2''), the positioning process of BD1 is accomplished by only two satellites in geostationary orbit, as shown in Figure 1. A typical BD1 positioning process is as follows. Firstly, the central control station sends inquiry signals to the user via the two satellites. Then the user terminal sends back responding signals to both satellites as soon as the signals are received. The responding signals will be forwarded by the two satellites, and arrive at the central control station sequentially with a measurable time difference. The user's 2D position can then be calculated based on the arriving time difference and the user's 3D position can be derived by checking the 2D position with a stored digital territorial map. Finally, the 3D position data is sent back to the user via

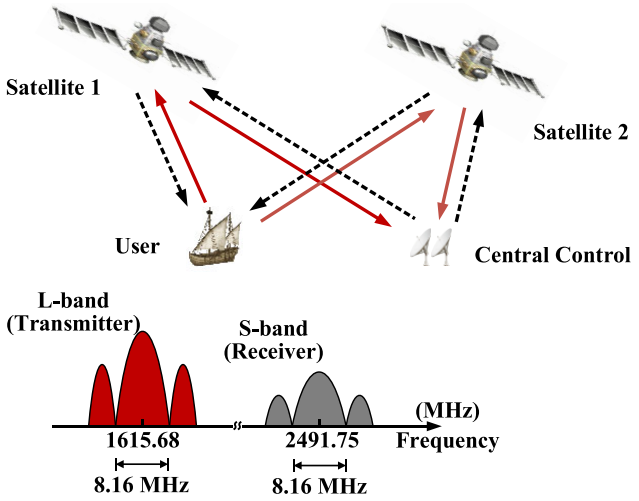


FIGURE 1. Principle of Beidou-1 system and band spectrum of the Beidou-1 signals.

one of the satellites, which concludes the positioning process. The above positioning process can also be initiated by a BD1 terminal user via SMS request to the central control station.

When used for satellite positioning, the BD1 system is not comparable to GNSS systems in terms of user capacity, positioning accuracy, user terminal power dissipation and radio silence requirements. Nevertheless, due to its two-way satellite communication system architecture, the SMS feature of BD1 system can be counted on where regular communication systems are not available. BD1 plays an important role in applications such as disaster management, aviation and navigation control etc.

Both BD1 and other GNSS systems receive signals from satellites which are over 20,000 km up in the sky and the received signals are far below the thermal noise floor when they arrive at the antennas. As a result, the low-IF architecture is applicable to the receiver (RX) part, which is similar to other GNSS systems [8]–[13]. Multi-order complex band-pass filters (CBPFs) are implemented in GNSS RXs [3], [4], [8]–[11] and complicated calibration techniques [4], [13] are discussed. Although these techniques enhance the robustness of the systems, the flatness of the CBPF passband still remains a design challenge, due to the fact of that the integrators used in the CBPF are non-ideal. This paper proposes a fully integrated RF CMOS BD1 transceiver with passive compensation techniques to compensate the phase lag and achieve pass-band flatness. To further increase the integration and reliability, on-chip low-dropout regulators (LDOs) are integrated for stable operation. For the transmitter (TX) part, a BPSK modulation is implemented to transmit the 4.08 Mchip/s baseband signal. The BPSK up-conversion is realized by using transmission gates to switch the output between two differential carrier signals. The differential signal paths are designed with good match thus the less than 3 degree phase error system specification can be met.

This paper is organized as follows. Section II describes the architecture and design considerations of the BD1 transceiver. Section III presents the detailed circuits implementations. Section IV gives the chip microphotograph and experimental results of the fabricated transceiver. Section V concludes the paper.

II. SYSTEM ARCHITECTURE

A. TRANCEIVER ARCHITECTURE

Figure 2 shows the detailed architecture of the proposed BD1 transceiver. Compared to zero-IF architectures, low-IF approach is more suitable for BD1 receiver because it can alleviate problems such as dc offset and flicker noise [3], [4], [8]–[13]. The receiver comprises a pseudo-differential low noise amplifier (LNA), a RF amplifier (RFA), a pair of quadrature down-conversion mixers, a CBPF, a programmable gain amplifier (PGA), a 4-bit flash analog-to-digital converter (ADC) and an IF automatic gain control (AGC) loop. The received RF signals are firstly

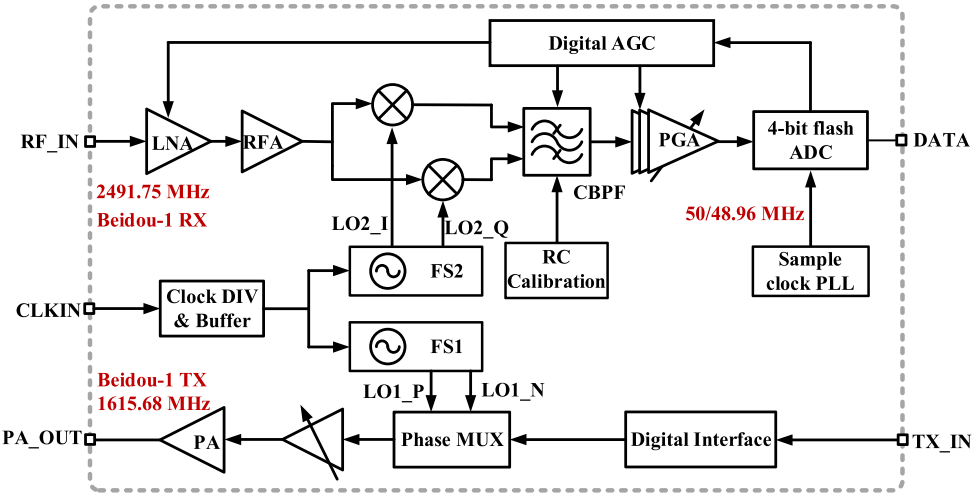


FIGURE 2. Beidou-1 transceiver architecture.

magnified by the LNA followed by the RFA to achieve an overall low noise figure (NF) and perform single-ended-to-differential transformation. The mixers are employed to down-convert the amplified RF signals to the IF band. The active fifth-order CBPF then provides moderate variable voltage gain, spectrum antialiasing and image rejection for the IF signals. To cope with PVT variations, the bandwidth and center frequency of the CBPF are calibrated during power up stage by a RC calibration module. To achieve pass-band flatness with minimum power consumption of amplifiers for the CBPF, a phase lag compensation technique is employed by using a RC network as the cross-coupling path [14]. The following fine tuning PGA and AGC loop are utilized to optimize the input range for the ADC whose output digital signals can be directly exploited to demodulate.

The transmitter is composed of a digital interface module, a phase multiplexor, a driver and a power amplifier (PA). Since BPSK modulation is chosen for BD1 system's channel coding, the baseband pseudo-random-binary-symbol (PRBS) signal selects one of the differential output signals of the frequency synthesizer through a phase multiplexor. Finally the modulated RF signals are amplified by a driver and a PA with a differential-to-single-ended inductive transformer to achieve a −10–5 dBm driving signal for an off-chip 5 W or 10 W PA.

The local oscillating (LO) signals for the mixer in RX and for the phase multiplexor in TX are generated by two independent fractional-N phase-locked loops (PLLs) with LC oscillators and on-chip automatic frequency calibration (AFC) modules. Besides, a third PLL with ring oscillator is designed to generate sampling clock for the ADC.

In order to reject ripples and high frequency noises from the power supply thus improving the power supply rejection ratio (PSRR) for a wider frequency range, LDOs with active low-pass filters (LPFs) are proposed to convert the supply voltages from 3.3 V to 1.5 V.

B. FREQUENCY PLAN

Figure 3 shows the frequency plan for the whole transceiver. The low-IF receiver down-converts the 2491.75 MHz RF signals to the 12.24 MHz IF band, and the transmitter up-converts the baseband signal to the RF band with a carrier frequency of 1615.68 MHz. The transmitter employs the direct-sequence spread spectrum (DSSS) technique, achieves the BPSK modulation by using the 4.08 Mchip/s baseband signal to switch the phases of the LO signals.

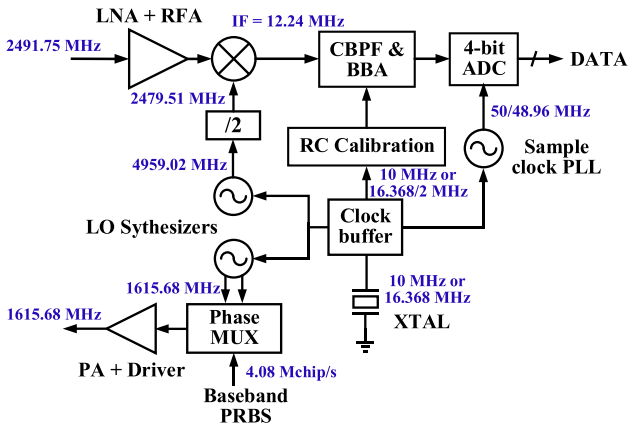


FIGURE 3. Frequency plan.

To get better noise performance for the RX and TX RF front-end, the LO frequency synthesizers utilize Fractional-N PLLs with LC voltage controlled oscillators (VCOs). A 4.3-to-5. 7-GHz PLL with a divide-by-2 divider is designed to generate quadrature signals for the down-conversion. The frequency of the PLL for TX ranges from 1.4 to 2 GHz. A third PLL provides 50 MHz or 48.96 MHz sampling clock for the ADC. All the reference clocks are derived from the same off-chip crystal whose center frequency is either 10 MHz or 16.368 MHz depending on the system usage.

C. GAIN AND NOISE IN RX

The received BD1 signals are far below the thermal noise floor as mentioned, and thus the thermal noise always dominates the input power level [15]. For the BD1 signal with a bandwidth of 8.16 MHz, a thermal noise floor of −105 dBm could be calculated. To get an optimum input peak-to-peak voltage range of 700 mV for the ADC, a 106 dB cascaded gain is needed for the receiver.

The gain dynamic range is determined by the gain variation introduced by the external components (DR_1), the PVT variation (DR_2) and the reserved safety margin. In this work, DR_1 is assumed to be 20 dB for active/passive antenna switching, and the gain variation against PVT is about 6.8 dB in simulation. If the headroom for possible gain variation (*margin*) is chosen to be 10 dB, the full dynamic range can be calculated as

$$DR = DR_1 + DR_2 + margin \approx 37dB \tag{1}$$

We can conclude that a gain dynamic range of 40 dB is sufficient for this design.

As mentioned in [15], it is more convenient to quantify noise performance for the receiver by the carrier-to-noise density ratio (C/N_0) than the signal-to-noise ratio (SNR). Once the minimum required C/N_0 at the ADC output is given by the baseband algorithms, the receiver sensitivity is uniquely determined as

$$\begin{aligned} &Sensitivity\,[dBm] \\ &= \left(\frac{C}{N_0}\right)_{min}[dB \cdot Hz] + N_0\left[\frac{dBm}{Hz}\right] + NF\,[dB] \end{aligned} \tag{2}$$

where N_0 is the thermal noise power density at the antenna port which equals to -174 dBm/Hz and NF is the noise figure of the receiver front-end chain.

The BD1 system specification demands a sensitivity of −127 dBm with a bit-error-rate (BER) less than 1×10^{-5}. Figure 4 depicts the noise and gain lineup of the BD1 RF receiver in the case of an active or a passive antenna. If an

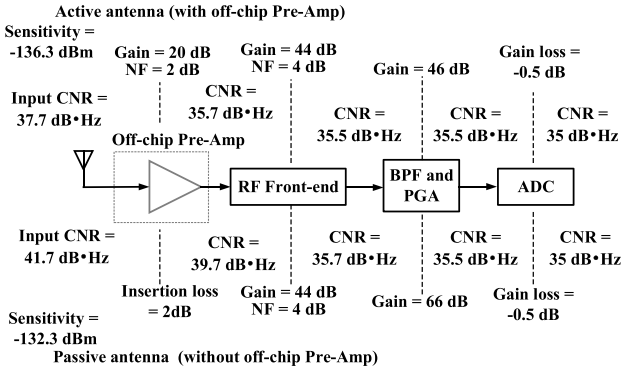


FIGURE 4. Gain and noise link budget of the receiver in the case of an active or a passive antenna.

active antenna which includes a pre-amplifier with 20 dB gain and 2 dB NF is used, a sensitivity of −136.3 dBm can be achieved with a minimum C/N_0 of 35 dB· Hz. With a passive antenna which has no extra voltage gain, the receiver sensitivity will be decreased to −132.3 dBm.

III. CIRCUIT IMPLEMENTATION

A. RX RF FRONT-END

The RX RF front-end comprises an LNA, a RFA and a pair of quadrature mixers. Figure 5 shows the schematic of the pseudo-differential LNA. The compensation capacitor C_c is incorporated to perform the single-ended-to-differential conversion, which removes the necessity of a lossy balun and provides an extra 6 dB voltage gain [16]. The phase and magnitude imbalance of the LNA could be eliminated by choosing a proper capacitance value of C_c. In this design, C_c is set to be 3.75 pF. In order to provide a large enough dynamic range, the voltage gain of the LNA is controlled by the AGC loop.

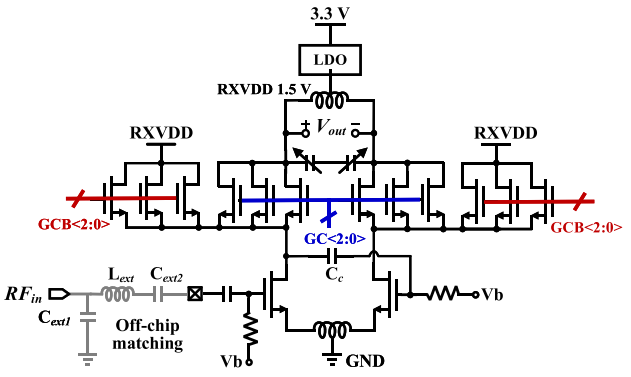


FIGURE 5. Schematic of LNA.

The input of the LNA is matched to 50 Ω by an off-chip L-type matching network with C_{ext1}, C_{ext2}, and L_{ext}, whose values are 2.7 pF, 20 pF, and 5.6 nH, respectively. With a supply voltage of 1.5 V from the ripple-cancelled LDO, the LNA provides a maximum voltage gain of 27 dB with a frequency tuning range around 100 MHz in post-layout simulation. The simulated NF for the LNA is about 2.9 dB over all corner cases.

To achieve an overall low NF for the RX front-end, a cascode RFA is added following the LNA with resistive loading, serving a 6-to-12-dB voltage gain with a gain step of 6 dB.

Figure 6 shows the double-balanced mixer based on Gilbert's topology, which provides an extra gain compared to the passive mixer implematation. With quadrature differential LO signals, the RF signals are down-converted to the IF band and divided into in-phase and quadrature paths. The mixers employ common-mode feedback (CMFB) resistors to stabilize the operating point and utilize source degenerate techniques to improve linearity. The voltage conversion gain of the mixers varies from 5 dB to 18 dB controlled by the AGC.

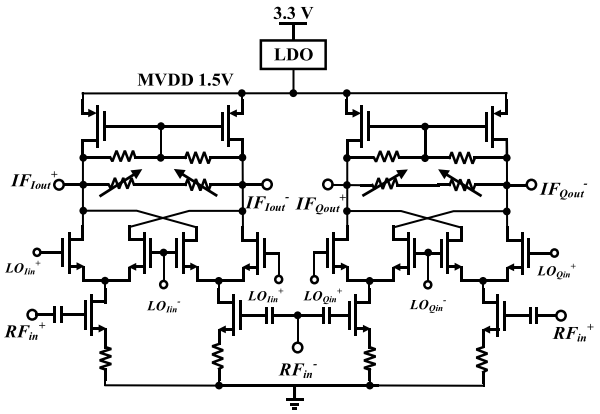


FIGURE 6. Schematic of Gilbert I/Q mixer.

In typical corner simulation, the total maximum gain of the RF front-end is 55 dB, the DSB NF is 3.2 dB and the IIP3 is −29.8 dBm. The total current is 7.5 mA with a supply voltage of 1.5 V from the LDO.

B. CBPF

Figure 7 shows the fifth-order Chebyshev-I CBPF based on active-RC integrators [17]–[23] to select the desired signals, reject the image and out-of-band spurious signals and noise. The CPBF also provides controlled IF gain with dc-offset cancellation. The CBPF is implemented by two real low-pass filters (LPFs), coupled through cross-coupling paths to shift the central frequency to the desired IF band. Unlike conventional complex filters, the proposed architecture employs parallel-RC networks as the cross-coupling paths between the in-phase and the quadrature paths to cancel the excess phase lag and reduce the in-band ripple. The phase lag compensation scheme is illustrated in Figure 8.

Figure 8 (a) shows the schematic of the cross-coupled integrators in conventional CBPF. The transfer function of the non-ideal integrators could be written as

$$H(s) = \frac{-\frac{1}{sRC}}{1+\frac{1}{RCA_0\omega_0}+\frac{s}{A_0\omega_0}} = -\frac{1}{sRC}\frac{1}{1+(\frac{1}{RC}+s)\frac{1}{A_0\omega_0}} \quad (3)$$

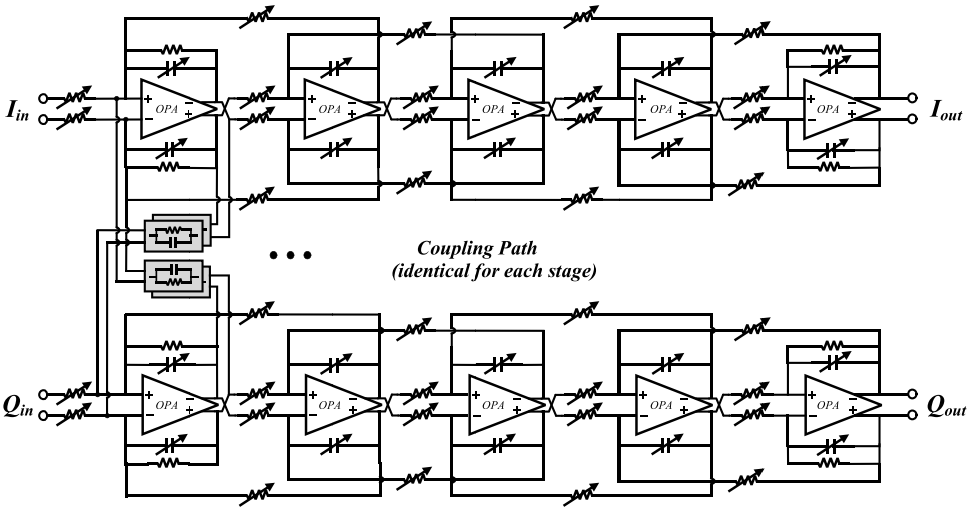
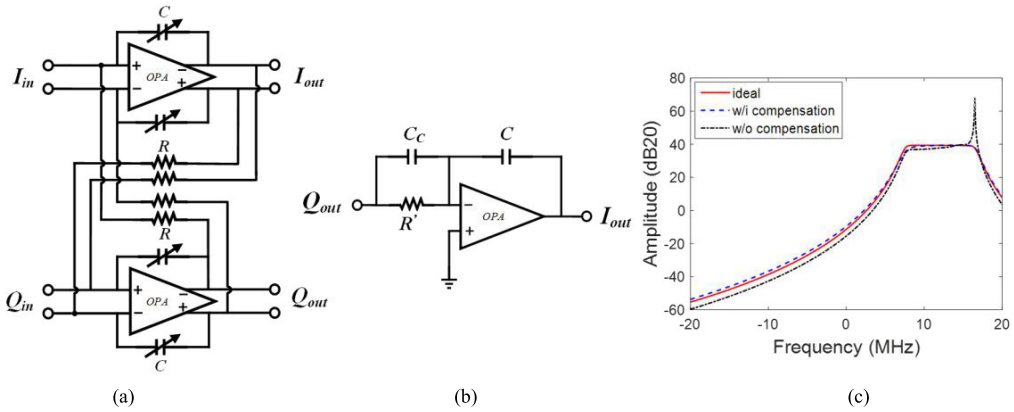


FIGURE 7. Schematic of CBPF.



(a) (b) (c)

FIGURE 8. Phase lag compensation illustration. (a) Conventional CBPF; (b) principle of phase lag compensation; (c) simulation results comparison between with and without compensation.

where A_0 and ω_0 are the dc gain and bandwidth of the operational amplifiers (OPAs) respectively. The resistance R and capacitance C jointly determine the IF frequency ($\omega_{IF} = 1/RC$). Since the gain bandwidth product (GBP) $A_0\omega_0 \gg 1$, (3) can be regarded as a form of $f(x) = 1/(1+ax)$(where $x \to 0$) and can be expressed by the 1st-order Taylor expansion as

$$\begin{aligned} H(s) &\approx -\frac{1}{sRC}\left(1-\left(\frac{1}{RC}+s\right)\frac{1}{A_0\omega_0}\right) \\ &= -\frac{1}{sRC}\left(1-\frac{1}{RCA_0\omega_0}\right)+\frac{1}{RCA_0\omega_0} \end{aligned} \tag{4}$$

To eliminate the non-ideal items caused by finite GBP of an OPA, a compensation scheme is proposed as shown in Figure 8 (b). A compensation capacitor C_C is introduced. We assume

$$\begin{cases} -\dfrac{1}{sR'C} = -\dfrac{1}{sRC}\left(1-\dfrac{1}{RCA_0\omega_0}\right) \\ -\dfrac{\frac{1}{sC}}{\frac{1}{sC_C}} = -\dfrac{1}{RCA_0\omega_0} \end{cases} \tag{5}$$

The transfer function will be close to $-1/sRC$ and the phase lag or ripple introduced by the non-ideal integrator will be compensated [14]. The value of R' and C_C can be calculated as

$$\begin{cases} R' = R(1-\dfrac{1}{RCA_0\omega_0}) \\ C_C = \dfrac{1}{RCA_0\omega_0} \end{cases} \tag{6}$$

The circuit-level simulation results of this passive compensation scheme are shown in Figure 8 (c). As the figure shows, the proposed scheme could effectively compensate the phase lag and the frequency response is very similar to the ideal result. An in-band ripple of 0.7 dB could be achieved with the proposed method without much tuning effort.

The voltage gain of the CBPF ranges from 7 dB to 55 dB, thus the CBPF also plays the role of a rough tuning PGA controlled by the AGC loop. The target center frequency and bandwidth is 12.24 MHz and 9 MHz respectively. A simple PGA is followed with a 0-to-6-dB gain for fine tuning purpose.

Since the frequency response characteristics of the CBPF will be affected by the PVT variations, a tuning circuit is required to calibrate the CBPF in real-time. As shown in Figure 9, a simple frequency calibration scheme is to compare an on-chip RC oscillator output *OSCIN* to a reference clock *RCLK*, and then set the filter RC time constant to a desired value by tuning the capacitor array. In addition, the frequency tuning result helps to identify the process corner and can be used to adjust bias currents to improve quality factor.

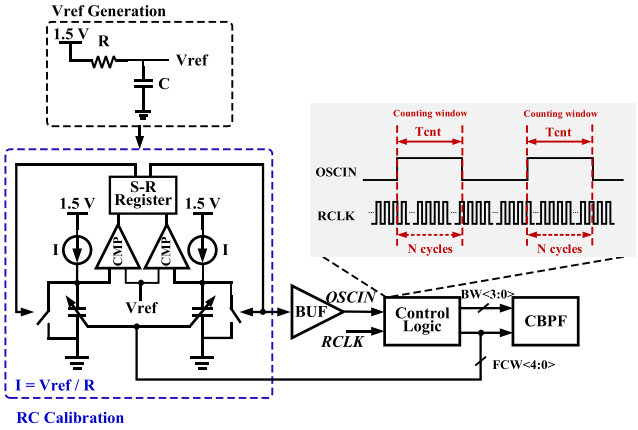


FIGURE 9. Frequency and bandwidth calibration based on RC tuning scheme.

The tuning is implemented by switching on a portion of the 31-unit capacitor array in the RC oscillator so its output clock frequency is as close as possible to a golden value derived from the reference frequency. The reference clock is used to count how many cycles are within the period of four RC oscillator clock cycles, typically 134 when *RCLK* is 10 MHz or 109 when *RCLK* is 16.368/2 MHz. If the counter value exceeds this threshold, the number of the capacitors *FCW<4:0>* should be reduced, or vice versa. The process is repeated until the counter value is the closest number to the target threshold.

C. 4-BIT FLASH ADC AND AGC LOOP

Figure 10 shows the diagram of the proposed 4-bit flash ADC. The fully differential input along with 16 reference voltages generated by a resistor string are fed into 16 parallel comparators and RS triggers, and then the output results are coded into a 17-bit thermometer code. The middle-bit of the thermometer represents the sign, and the upper 8 bits and the lower 8 bits represent the magnitude of the results. The thermometer code will then be converted to a 4-bit binary code by the thermometer to binary (T2B) encoder. The sampling clock is 50 or 48.96 MHz synthesized by a simple Fractional-N PLL with a two-stage ring oscillator.

The AGC feedback control loop, as shown in Figure 11, is employed to control the gain of the LNA, the RFA, the CBPF and the fine tuning PGA stages. The magnitude of the IF signals at ADC input node will be adjusted dynamically to an optimal level even if the input RF signal fluctuates.

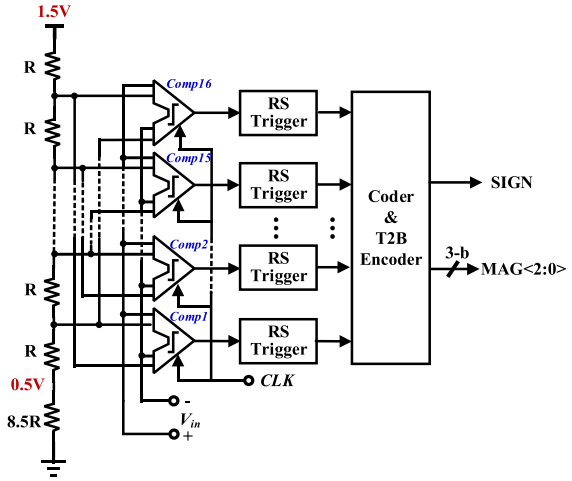


FIGURE 10. 4-bit flash ADC.

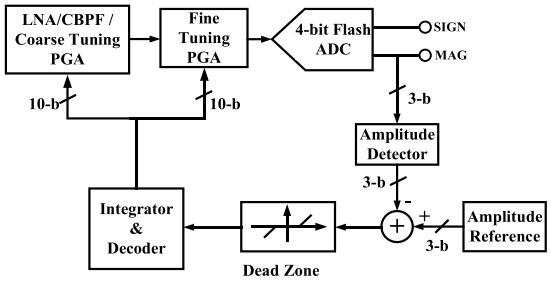


FIGURE 11. AGC loop.

For a typical gain tuning process, the digital AGC module will allocate as much as possible gain to the frontier stages to maintain an overall low NF.

D. DETAILED TX

To achieve BPSK modulation in TX, as is shown in Figure 2, the PRBS baseband data are directly sent to the phase multiplexor-based modulator to select a pair of differential LO signals synthesized by the PLL [4]. The signals chosen by the phase multiplexor are then fed to a driver amplifier to drive the on-chip PA.

Figure 12 shows the detailed schematic of the TX. The phase multiplexor utilizes two pairs of complementary transmission gates to select the corresponding LO signals according to the BPSK data pattern *D*. Since the maximum output power is required to be 5 dBm, signals from the multiplexor are fed to a driver amplifier first before the PA to assure sufficient power gain. An on-chip inductor resonating with tunable capacitor is used as load for the driver amplifier to filter out out-of-band harmonics. The PA has same topology with the driver and the output power level is controlled by a 4-bit gain control code. The PA has a differential input and a transformer is designed as an inductive load to convert the differential signal into single ended signal. The transformer primary has an inductance value of 6.5 nH and a Q factor of 23. The secondary has an inductance value of 3.2 nH and a Q factor of 15. Transformer primary side has been tied with

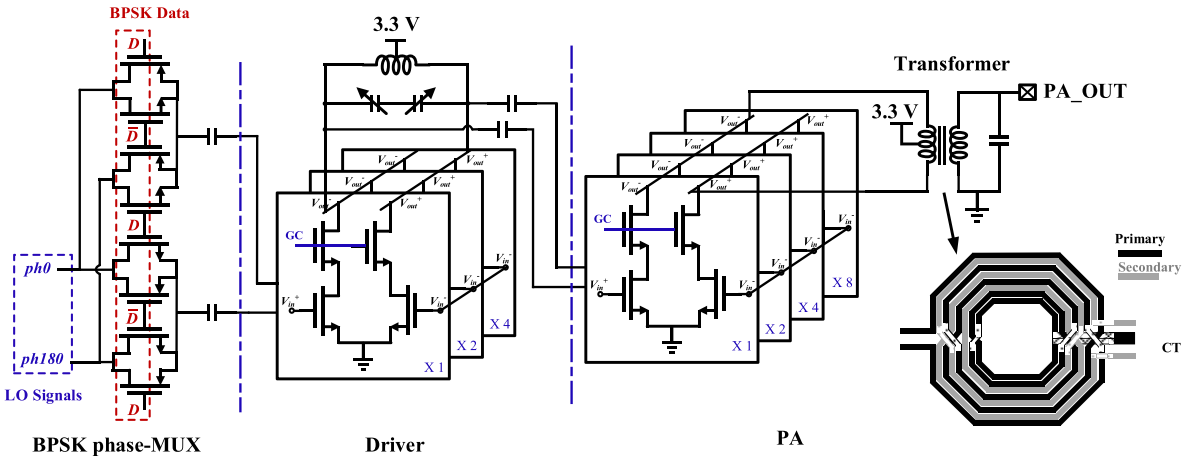


FIGURE 12. Detailed schematic of TX.

a tuning cap bank, whose capacitance can be adjusted from 0 to 850 fF with 50 fF per step, thus the center frequency can be tuned to 1.6 GHz even in case of PVT variations. The PA output impedance which is about 140 Ω is transformed to 50 Ω required by the external impedance matching. The optimized PA output impedance is designed to present to PA output differential port to make PA to deliver optimized output power up to 5 dBm.

The TX operates at 1615.68 MHz with a chip rate of 4.08 Mchip/s and a bandwidth of 8.16 MHz. The maximum gain of the driver amplifier and the PA is 6 dB and 12 dB, respectively. The output power of the PA ranges from −10 dBm to 5 dBm with a maximum power consumption of 41 mW. In order to achieve a low error probability for receiver demodulation on the satellite side, the modulation phase error is optimized to be less than 3°.

E. SYNTHESIZERS

The proposed full-duplex transceiver demands two independent frequency synthesizers for the transmitter and the receiver respectively. Figure 13 shows the schematic of the synthesizers realized by the Fractional-N PLLs which consist of a phase frequency detector (PFD), a charge pump (CP), an on-chip LPF, a VCO, a divider including a 4/5 prescaler, a programmable counter and a delta-sigma ($\Delta\sum$) module, and an AFC module. The output signals of the PLL in RX are given to the mixer after the divide-by-2 divider since the quadrature LO signals are essential for the quadrature down-conversion, and the LO signals for the TX are fed to the phase-multiplexor directly via a buffer.

Figure 13 also presents the detailed schematic of the LC-VCO with NMOS and PMOS cross-coupled topology to ensure good phase noise performance. A 4-bit binary capacitor bank controlled by the AFC is integrated in the VCO for frequency coverage [24]. Once an automatic calibration process is done, the PLL loop will be closed and a normal locking process will start.

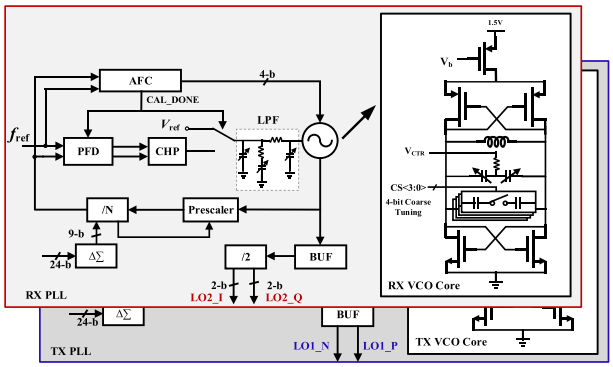


FIGURE 13. Schematics of synthesizers.

The bandwidth of the PLL in RX is set to about 150 kHz and that in TX is around 100 kHz. The output frequency of the VCO in RX ranges from 4.3 to 5.7 GHz and the K_{VCO} is around 170 MHz/V, while the VCO in TX has a 1.4-to-2-GHz frequency range and the K_{VCO} is about 70 MHz/V. The whole PLLs consume 9.5 mA and 6.2 mA current from the 1.5 V supply for the RX and TX, respectively.

With energy efficiency and low cost considerations, another individual Fractional-N PLL based on a two-stage ring VCO is designed to generate a sampling clock with a frequency of 50 or 48.96 MHz for the ADC.

F. ON-CHIP LDO WITH IMPROVED PSRR

Figure 14 shows the schematic of the LDO with PSRR improving techniques to reject the noise or ripple of the supply voltage. Different from the conventional LDOs consisting of a high gain error amplifier and an output power transistor along with an output capacitor and a load resistor [25], an active LPF implemented with an NMOS transistor, a resistor and a MOS-type capacitor is integrated in this design to improve PSRR for the LDO. The error amplifier is a simple two-stage amplifier, with one input tied to the

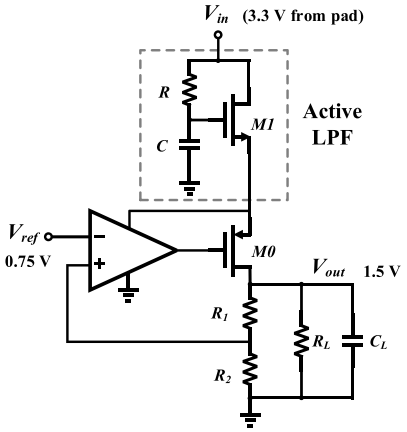


FIGURE 14. Schematics of LDO with improved PSRR.

reference voltage and the other input tied to the feedback element [26]. A 20 pF loading capacitor C_L is integrated on-chip. To get an output voltage of 1.5 V from a 3.3 V input supply, the reference voltage is set to 0.75 V. The PSRR can be improved by 20 dB with the help of the active LPF which has a dominant pole at 100 kHz and a zero at 2 MHz. With the purpose of satisfying the need of both current-hungry high-frequency circuits such as LNA, mixer and moderate current-consumption or low-frequency circuits such as CBPF, two kinds of LDO are designed with maximum output current of 30 mA and 20 mA.

IV. MEASUREMENT RESULTS

The proposed BD1 transceiver is implemented in a 130 nm CMOS technology and a die microphotograph is shown in Figure 15. The whole die area is approximately 2.4 mm × 2.45 mm including ESD protection circuitry and pads. The measurement was carried out after chip packaging and PCB design without external amplifiers. The matching networks for PA and LNA as well as testing ports are included on the PCB board.

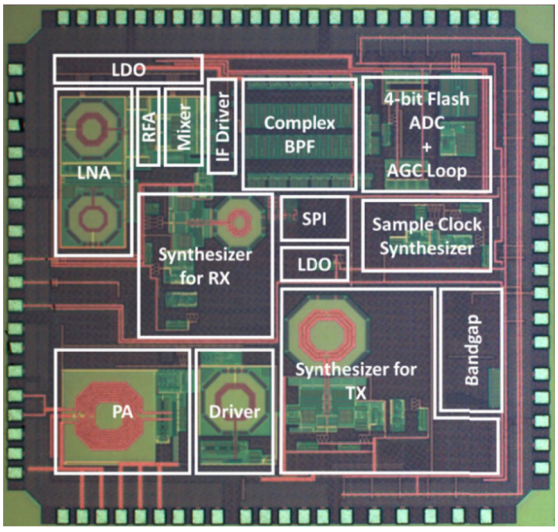


FIGURE 15. Chip microphotograph.

The measured RX input S11, as shown in Figure 16, is about −15 dB at 2.5 GHz. Besides, S11 is lower than −14 dB at the frequency range of 2.5 GHz ± 4.08 MHz. The measured voltage gain and the noise figure of the RX front-end, CBPF and PGA before the ADC are shown in Figure 17. A typical voltage gain is about 82.5 dB and a bandwidth is about 9 MHz with less than 1 dB flatness. The noise figure is 4.95 dB at 12 MHz. The measured IMRR is larger than 46 dB, as shown in Figure 18.

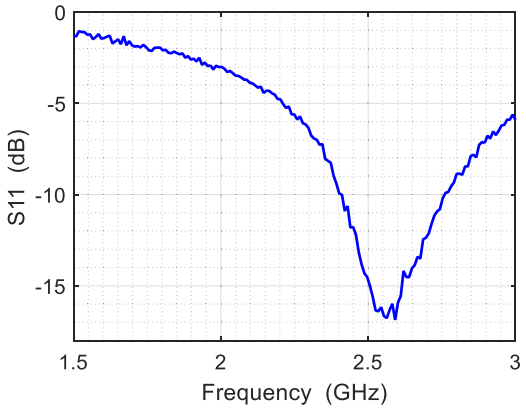


FIGURE 16. Measured S11.

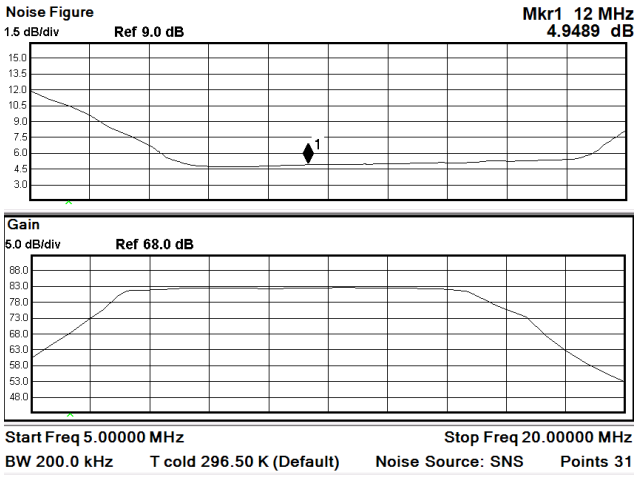


FIGURE 17. Measured gain and noise of RX front-end.

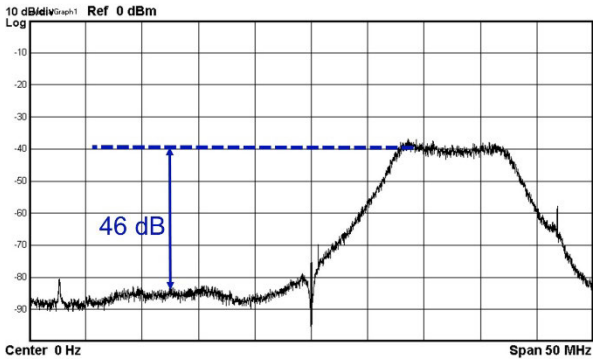


FIGURE 18. Measured IMRR.

TABLE 1. Performance summary and comparison.

Parameter	This work	2012 [3]	2015 [4]	2013 [5]	2017 [12]	2012 [13]
Technology	130 nm	180 nm	55 nm	40 nm	180 nm	65 nm
Supported systems	Beidou-1	GPS/Galileo/ BD-2	All GNSS/ Beidou-1	All GNSS	All GNSS	All GNSS
Noise Figure (dB)	4.95	2.5 – 2.7	1.92 – 2.5	2.1	N.A.	1.88 – 2.31
IF Frequency (MHz)	12.24	6/16	15.9/15.48/ 12.24	13/7/4	17	20/10/8/12/6/4
Channel BW (MHz)	8.16	2/4/20	2/4/9/10/20	2/4/9/15	33	2.2/4.2/8/10/18
Maximum Voltage Gain	106 dB	110 dB	116 dB	78 dB	N.A.	107 dB
Dynamic Range (dB)	65	73	88	26	64	52
P_{1dB} (dBm)	-39.8	-42/-39	< -25	-18	N.A.	-61
IMRR (dB)	46	28	> 49	33	59.3	~ 50
Filter Order	5	5	7	4	4	5
Active Area (mm^2)	5.88*	2.4†	8.4*	0.25†	0.73†	10.5†
Supply Voltage (V)	1.5 (3.3 for PA)	1.8	1.2	1.3	1.8	1 – 2.5
Power Dissipation (mA) †	30	25	25.8 – 30.2	7.2	30.2	8.2-13.2
EVM (%)	5.69	N.A.	6.23	N.A.	N.A.	N.A.
Phase Error (°)	1.496	N.A.	1.493	N.A.	N.A.	N.A.

*The whole transceiver area.
†RX only.

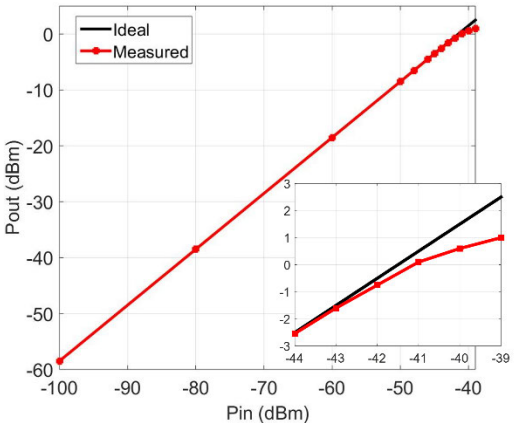


FIGURE 19. Measured P1dB.

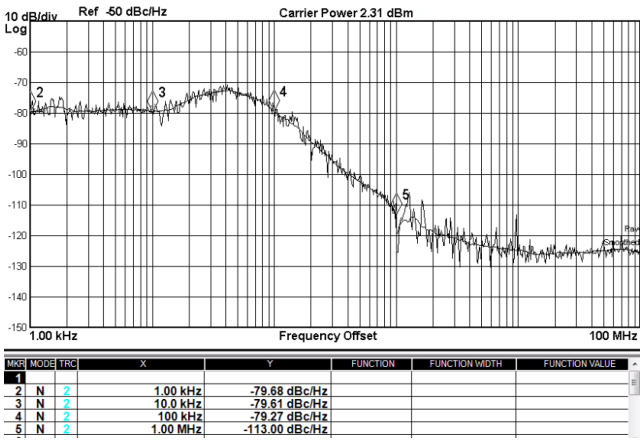


FIGURE 20. Measured phase noise of TX PLL.

The 1-dB compression point P1dB of the RF receiver can be measured by sweeping the input power and observing the output amplitude of the PGA. As shown in Figure 19, the measured input-referred 1-dB compression point is about −39.8 dBm with a 41 dB gain setting.

Figure 20 shows the measured phase noise of the PLL for TX from the PA testing port without baseband signals. When the PLL operates at 1615.68 MHz with a carrier power of 2.31 dBm, a phase noise of −113 dBc/Hz at 1 MHz frequency offset can be measured. In addition, the loop bandwidth is about 100 kHz, which is in accord with simulation results.

Figure 21 plots the measured constellation diagram of the TX BPSK signal modulated by 4.08 Mchip/s baseband signals. The measured EVM is 5.689% and the phase error is 1.496° at about 5-dBm output power. In addition, the measured ACPR is about 18 dB. The relatively small phase error provides tolerance for additional phase error possibly introduced by an off chip high power PA, thus the total phase error could be less than 3° system specification.

Figure 22 shows the test-bench, which is composed of an RF PCB board to be tested, an 8051 microcontroller for SPI interface, an FPGA for baseband signal generation and

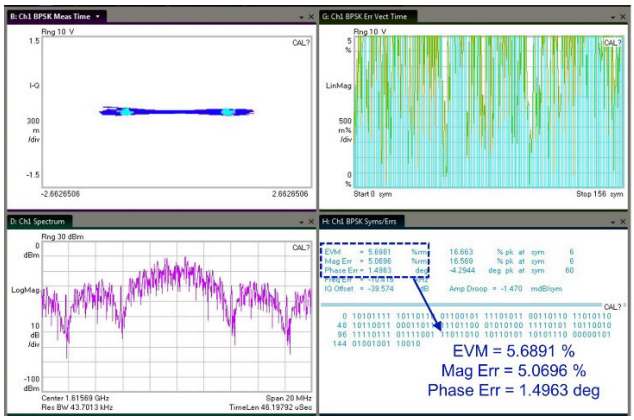


FIGURE 21. Measured EVM with 4.08 Mchip/s BPSK signal.

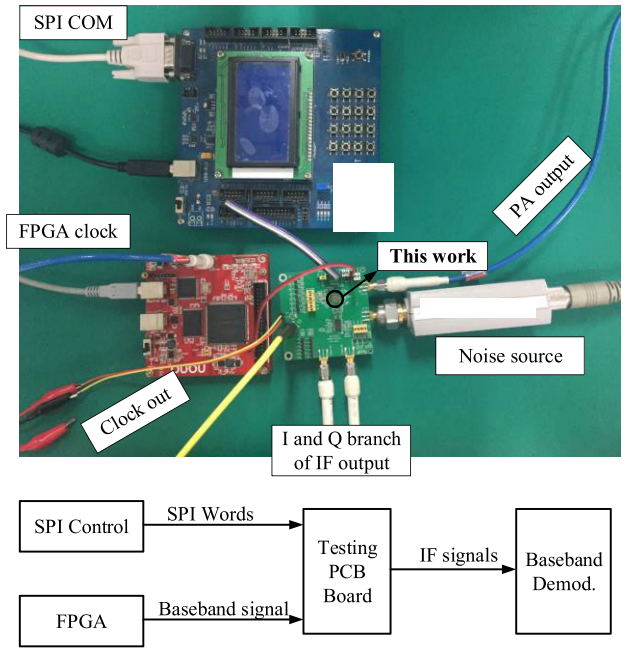


FIGURE 22. Test bench of the Beidou-1 transceiver.

other instruments such as noise source, spectrum analyzer etc. The measured performance of the BD1 RX is summarized in Table 1, and the performance comparison with the-state-of-the-art GNSS receivers is also shown since BD1 receiver works in similar fashion as GNSS receivers.

V. CONCLUSION

A fully integrated CMOS RF transceiver is proposed in this paper for BD1 system, which is a mature RDSS system providing regional positioning and short message communications service. The proposed transceiver is implemented with a low-IF receiver, a BPSK transmitter, two local frequency synthesizers and on-chip LDOs to realize a dual-way communication between users and the central control station via satellites.

The transceiver is fabricated in a 130 nm CMOS technology and the performance is comparable to the-state-of-the-art GNSS receivers and BD1 transceiver.

REFERENCES

[1] B. W. Parkinson and J. J. Spilker, "Global positioning system: Theory and applications (progress in astronautics and aeronautics)," *Amer. Inst. Astronaut. Aeronaut.*, vol. 1, pp. 57–93, Sep. 1996.

[2] C. Fernandez-Prades, L. L. Presti, and E. Falletti, "Satellite radiolocalization from GPS to GNSS and beyond: Novel technologies and applications for civil mass market," *Proc. IEEE*, vol. 99, no. 11, pp. 1882–1904, Nov. 2011.

[3] D. Chen, W. Pan, P. Jiang, J. Jin, T. Mo, and J. Zhou, "Reconfigurable dual-channel multiband RF receiver for GPS/Galileo/BD-2 systems," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3491–3501, Nov. 2012.

[4] S. Li, J. Li, X. Gu, H. Wang, C. Li, J. Wu, and M. Tang, "Reconfigurable all-band RF CMOS transceiver for GPS/GLONASS/Galileo/Beidou with digitally assisted calibration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 9, pp. 1814–1827, Sep. 2015.

[5] C. G. Tan, F. Song, T. Y. Choke, M. Kong, D.-C. Song, C.-H. Yong, W. Shu, Z. H. You, Y.-H. Lin, and O. Shanaa, "A universal GNSS (GPS/Galileo/Glonass/Beidou) SoC with a 0.25 mm^2 radio in 40 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2013, pp. 334–335.

[6] C. Williams, "Radiodetermination satellite service: Applications in railroad management," in *Proc. 36th IEEE Veh. Technol. Conf.*, vol. 36, May 1986, pp. 395–397.

[7] R. Briskman, "Radio determination satellite service," *Proc. IEEE*, vol. 78, no. 7, pp. 1096–1106, Jul. 1990.

[8] Y. Wang, B. Gao, P. Li, X. Ni, and R. Zhou, "A RF CMOS GNSS receiver with a passive mixer for GPS L1/Galileo E1/Compass B1 band," *IEICE Electron. Express*, vol. 15, no. 13, Jul. 2018, Art. no. 20180551.

[9] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 372–374.

[10] D. Sahu, A. Das, Y. Darwhekar, S. Ganesan, G. Rajendran, R. Kumar, B. G. Chandrashekar, A. Ghosh, A. Gaurav, T. Krishnaswamy, A. Goyal, S. Bhagavatheeswaran, K. M. Low, N. Yanduru, S. Dhamankar, and S. Venkatraman, "A 90nm CMOS single-chip GPS receiver with 5dBm out-of-band IIP3 2.0dB NF," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2005, pp. 308–309.

[11] T. Kadoyama, N. Suzuki, N. Sasho, H. Iizuka, I. Nagase, H. Usukubo, and M. Katakura, "A complete single-chip GPS receiver with 1.6-V 24-mW radio in 0.18- m CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 562–568, Apr. 2004.

[12] J. Zhang, Y. Xu, Z. Zhang, Y. Sun, Z. Wang, and B. Chi, "A 10-b Fourth-order quadrature bandpass continuous-time $\Sigma\Delta$ modulator with 33-MHz bandwidth for a dual-channel GNSS receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 4, pp. 1303–1314, Apr. 2017.

[13] N. Qi, Y. Xu, B. Chi, Y. Xu, X. Yu, X. Zhang, N. Xu, P. Chiang, W. Rhee, and Z. Wang, "A dual-channel compass/GPS/GLONASS/Galileo reconfigurable GNSS receiver in 65 nm CMOS with on-chip I/Q calibration," *IEEE Trans. Circuits Syst. I. Fundam. Theory Appl.*, vol. 59, no. 8, pp. 1720–1732, Aug. 2012.

[14] Y. Li, Y. Wang, and B. James Kuo, "A new passive compensation structure for Chebyshev complex band-pass filter design," *Microw. Opt. Technol. Lett.*, vol. 60, no. 10, pp. 2397–2402, Sep. 2018.

[15] J. Ko, J. Kim, S. Cho, and K. Lee, "A 19-mW 2.6-mm^2 L1/L2 dual-band CMOS GPS receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1414–1425, Jul. 2005.

[16] J. Wu, P. Jiang, D. Chen, and J. Zhou, "A dual-band GNSS Rf front end with a pseudo-differential LNA," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 58, no. 3, pp. 134–138, Mar. 2011.

[17] C.-Y. Ho, W.-S. Chan, Y.-Y. Lin, and T.-H. Lin, "A quadrature band-pass continuous-time delta-sigma modulator for a Tri-Mode GSM-EDGE/UMTS/DVB-T receiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2571–2582, Nov. 2011.

[18] G. Gramegna, P. G. Mattos, M. Losi, S. Das, M. Franciotta, N. G. Bellantone, M. Vaiana, V. Mandara, and M. Paparo, "A 56-mW 23-mm^2 single-chip 180-nm CMOS GPS receiver with 27.2-mW 4.1-mm2 radio," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 540–551, Mar. 2006.

[19] S. Lerstaveesin and B.-S. Song, "A complex image rejection circuit with sign detection only," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2693–2702, Dec. 2006.
[20] J. Lim, Y. Cho, K. Jung, J. Park, J. Choi, and J. Kim, "A wide-band active-RC filter with a fast tuning scheme for wireless communication receivers," in *Proc. IEEE Custom Integr. Circuits Conf.*, Jan. 2006, pp. 637–640.
[21] V. Della Torre, M. Conta, R. Chokkalingam, G. Cusmai, P. Rossi, and F. Svelto, "A 20 mW 3.24 mm^2 fully integrated GPS radio for location based services," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 602–612, Mar. 2007.
[22] A. Emira and E. Sanchez-Sinencio, "A pseudo differential complex filter for bluetooth with frequency tuning," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 50, no. 10, pp. 742–754, Oct. 2003.
[23] S. Li, J. Li, X. Gu, H. Wang, J. Wu, D. Yan, and Z. Zhuang, "Dual-band RF receiver for GPS and compass systems in 55-nm CMOS," in *Proc. ESSCIRC*, Sep. 2013, pp. 173–176.
[24] J. Shin and H. Shin, "A 1.9–3.8 GHz $\Delta\Sigma$ fractional-N PLL frequency synthesizer with fast auto-calibration of loop bandwidth and VCO frequency," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 665–675, Mar. 2012.
[25] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.
[26] M. Cheah, D. Mandal, B. Bakkaloglu, and S. Kiaei, "A 100-mA, 99.11% current efficiency, 2-mV_{pp} ripple digitally controlled LDO with active ripple suppression," *IEEE Trans. VLSI Syst.*, vol. 25, no. 2, pp. 696–704, Feb. 2017.

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