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GaN Power Integration for High Frequency and High Efficiency Power Applications: A Review

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ABSTRACT High frequency and high efficiency operation is one of the premier interests in the signal and energy conversion applications. The wide bandgap GaN based devices possess superior properties and have demonstrated exceeding performance than Si or GaAs devices. In order to further exploit the potential of GaN electronics, monolithic power integration is proposed. Firstly, this paper discusses the structure and properties of GaN power devices to explain the choice of lateral integration in the view of GaN power ICs. Then the state-of-the-art performance of GaN power integration in two major application areas is reviewed, which are the microwave power amplification and DC-DC power conversion. The GaN power integration technologies in MMIC platforms are summarized in terms of the gate length, operation frequency and power added efficiency of ICs. On the other hand, the smart GaN power IC platforms have boosted the development of DC-DC power converters. Demonstrations of high frequency (>1 MHz) and high efficiency (>95 %) converters with various kinds of integration technology and topology are reviewed. Lastly novel integration schemes and methods are introduced to stimulate new thoughts on GaN power integration road.

INDEX TERMS GaN, HEMT, high frequency, power conversion, power integration.

I. INTRODUCTION

In the view of minimizing power consumption and heat dissipation during signal or energy conversions, high frequency and high efficiency are most attractive among the premier interests on the power IC designers' checklist [1], [2]. The volume of magnetic energy storage components and the system conversion loss can be largely reduced under higher operation frequency [3]. Moreover, transistors, diodes and passive components can be monolithically integrated to eliminate the parasitic inductance brought by bonding wires to further push the frequency and efficiency, which leads to the wide introduction of power integrated circuits [4], [5].

Other than the development of power IC design techniques, the continuous performance evolution of power integrated devices has accelerated the adoption of novel materials [6], [7]. Compared with Si, GaN material possesses over ∼3.1 times of energy bandgap, ∼2.7 times of electron saturation velocity and ∼11.6 times of critical electric field, which makes GaN suitable for RF and power conversion applications [8]. Especially the GaN High Electron Mobility Transistors (HEMTs) exhibit a 2-Dimentional Electron Gas (2DEG) channel and well fit the lateral integration [9], [10], which is a promising road to fully exploit the merits of GaN material.

The Monolithic Microwave Integrated Circuit (MMIC) was proposed in the GaAs-age with the first MMIC in 1975 [11] and now is still the mainstream process for GaN-based RF and microwave applications [12], [13]. Based on single-chip air-bridge integration of HEMTs, thin film or epitaxy resistors, and metal-insulator-metal capacitors, MMIC process has supported the high frequency microwave electronics from MHz to GHz ranges [14], [15]. The critical dimensions of GaN MMIC process has been reduced from several microns to sub-micron scale of 0.5 μm [16], 0.25 μm [17], 0.15 μm [18], 0.1 μm [19], 0.04 μm and 0.02 μm [15]. Commercial GaN HEMT MMIC platforms include BAE Systems, Fujitsu, Fraunhofer, HRL, MACOM, Northrop Grumman Aerospace Systems and Electronic Systems, NXP, Oki, Qorvo, Raytheon, Wolfspeed and so on, together with many other foundries listing GaN on their

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roadmaps. The highly scaled GaN HEMTs have formed excellent MMIC power amplifiers for 5G mobile bands with superior power added efficiency (PAE) performance.

Besides the RF and microwave applications, MMIC process can also play an important role in power conversion applications [20]–[23]. Ultra-high-frequency (UHF) DC-DC converter for on-chip power supply in Envelope Tracking (ET) application is presented at 865 MHz [21]. A buck converter switching at 100 MHz can obtain 90 % efficiency at 9 W output [22]. Other works on resonant DC-DC converters are demonstrated at approximately 1 GHz [24]. However, due to the relative low length of drift region in highly scaled GaN HEMTs in MMIC platforms, the state-of-the-art breakdown voltage is mostly below 150 V. Also the threshold voltage of HEMTs is negative, which is not fault-safe and requires specially designed gate driver. These conditions restrain GaN MMIC processes from realizing high voltage and high power DC-DC converters [25].

GaN power HEMTs or Metal-Insulator-Semiconductor (MIS) HEMTs with normally-OFF operation are introduced by means of gate recess [26], fluorine-ion implantation [27], p-type cap layer [28] or cascode structure [29]. The GaN normally-OFF power devices has ushered a new age of high-frequency and high-efficiency power conversion. Major power semiconductor companies have launched their GaN product lines, such as Cree, Infineon, Panasonic, ON-semi, Texas Instruments and TSMC, while other start-up companies are growing to key players including Efficient Power Conversion (EPC), GaN System, Navitas, Transphorm, VisIC and Wolfspeed. With the increasing availability of commercial discrete devices, the constructed power converter with GaN normally-OFF transistors have surpassed the Si-based counterparts in both output efficiency and operation frequency. It has realized over 95 % efficiency at over 1 MHz and output power over 1 kW [30], [31]. In order to minimize the converter volume for high frequency and high efficiency power conversion, normally-OFF power integration platforms are proposed [6], [9], [10], [32]–[38].

Integration schemes in power converters start from normally-OFF HEMTs with diodes for boost converters using fluorine-ion implantation technique in 2008 [39], [40] and p-type cap-layer Gate-Injection-Transistor technique in 2012 [41]. Later integrated half-bridges, full-bridges are realized with pre-gate driver to reduce the inductance of gate drive loop and a 12 V-1.8 V converter exhibits peak efficiency of 86.6 % at 2 MHz [42]. In the meantime, functional circuits such as inverter [43], comparator [44], voltage reference generator [45] and pulse-width-modulation circuit [46] are fabricated and have successfully demonstrated the analog functions of GaN integrated circuits.

The tide of high-speed GaN revolution keeps rising in industries. The consumer electronics can benefit in power density, charging speed and cost reduction with high-frequency and high-efficiency GaN power integrated converters. Firstly Navitas and Dialog have launched their System on Chip (SoC) GaN power ICs NV6115 and DA8801, respectively. In the meantime, EPC, Infineon, Tagore Technology and Texas Instruments choose the System in Package (SiP) road. The close proximity of devices and components can greatly reduce parasitic inductance to boost the switching speed. Based on low-voltage transistors, functional subcircuits including gate driver, control and feedback circuits can be integrated as well.

In this paper, the GaN power integration for high frequency and high efficiency power applications is systematically reviewed. In the view of power ICs, the structure and property of GaN power devices are firstly discussed in section II, including the reasons why lateral integration is a choice. In section III the GaN MMIC processes are briefly presented in terms of critical dimensions and IC performance. The GaN smart power IC platforms are discussed in section IV with the development of device technology. Section V includes novel integration platforms and technologies to shed some light on future direction of the GaN integration road. Finally, Section VI summaries this review.

II. GAN DEVICES FOR LATERAL INTEGRATION

A. DEVICE PHYSICS AND STRUCTURE

The advantages of GaN over other solid state materials are so apparent that the GaN-based electronic devices should be the better choice for high power applications including RF, microwave and power conversion applications. The GaN material has a noncentrosymmetric wurtzite structure. Due to the difference between electronegativity of Ga and N atoms, the centers of the positive and negative charge in electron cloud do not coincide, thus GaN shows spontaneous polarization. In peseudomorphically grown epitaxial AlGaN/GaN structure, there will be strains due to the lattice mismatch and dislocations, which lead to the piezoelectric polarization. For Ga-face AlGaN/GaN heterostructures, the polarization induced charge density values can be calculated [47]. Fig. 1 shows the calculated polarization charge and 2DEG density values with various Al mole fraction with an inset of basic AlGaN/GaN heterostructure.

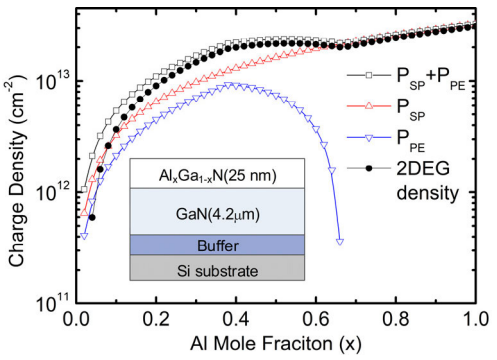


FIGURE 1. Calculated spontaneous polarization (P_{SP}), piezoelectric polarization (P_{PE}) and 2DEG density versus Al mole fraction in a typical AlGaN/GaN heterostructure shown in inset.

The 2DEG channel conduction is the key feature of lateral GaN devices, where the electron density can be around

1×10^{13} cm^{-2}. The source, gate and drain electrode configuration in AlGaN/GaN based devices further paves the way of integration in the same manner as Complimentary-Metal-Oxide-Semiconductor (CMOS) or Lateral-Diffusion-MOS (LDMOS) process. Fig. 2 show the SEM images of AlGaN/GaN HEMTs specially designed for MMIC [48] and power conversion application [28], respectively.

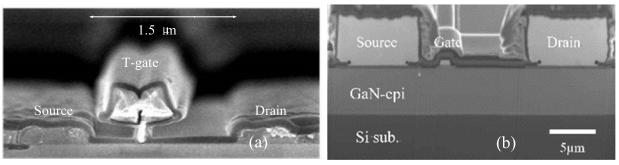


FIGURE 2. SEM images of AlGaN/GaN with (a) 0.1 μm gate length for MMIC application [48] and (b) 2 μm gate length for power conversion application [28].

In order to get high power-gain cutoff frequency f_{max}, the gate length can be designed as 100 nm, for example, in Fig. 2(a). While for GaN HEMTs in power applications, the gate length as well as gate-drain separation are designed to be larger, such as 2 μm and 7.5 μm, respectively, in Fig. 2(b). These lateral distance values, which are all larger than that of GaN HEMTs for MMIC application, can contribute to higher breakdown voltage for GaN power HEMTs. Despite the difference in in dimensions, the same heterostructure and electrode layout establish the common structure basis of lateral power integration schemes.

For a single device, the switching frequency is related with its structure. However when devices are applied with external circuits or ICs, the parasitic inductance in gate drive loop also significantly affects the maximum operation frequency [49]. The parasitic resistance and inductance in all the interconnections, through-vias, wires and pads can degenerate the high frequency switching performance of GaN ICs. This is a critical aspect that current GaN integration technology are trying to improve.

B. CO-INTEGRATION OF GAN HEMTS FOR MMIC AND POWER SWITCHING

Monolithic co-integration of the optimal GaN HEMTs for MMIC and power switching can be the promising solution of multi-function GaN ICs. In GaN devices, the drain-side access region with length of L_{GD} bears most breakdown voltage (BV). The L_{GD} of the power devices is relatively large to obtain a high breakdown voltage; however, the GaN HEMTs for MMIC have very high channel carrier concentration and shorter L_{GD} (typically less than 1 μm) to improve operation frequency with the sacrifice of BV. In order to realize the trade-off between high frequency and high breakdown voltage in the co-integration, specially designed and optimized field plates (FPs) can be introduced as one of the possible solutions.

The FPs connected with source and gate can modulate the distribution of surface electric field and alleviate the high electric filed at gate corner in drain side, which contributes to higher BV. The reported FP types in GaN HEMTs are summarized in Fig. 3. Other than the conventional source FP and gate FP, novel FP structures have been developed. Table 1 listed the reported characteristics of GaN HEMTs with several FP types. The FP techniques can offer efficient solutions to improve BV of GaN HEMTs.

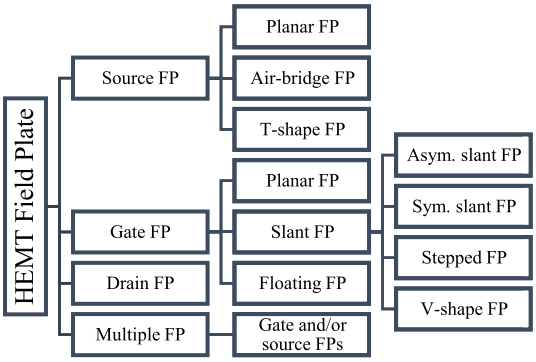


FIGURE 3. Field plate types in GaN HEMTs.

TABLE 1. Characteristics of GaN HMETs with various FP types.

FP type	$L_G/L_{GD}/L_{FP}$	f_t/f_{max}	BV	Authors
Multiple gate FPs	1/24/~1.4 μm	<1 GHz/-	850 V	UCSB [50]
Air-bridge recessed FP	0.2/1.3/0.85 μm	38.5/95 GHz	144 V	CAS [51]
Asymmetric slant FPs	0.2/2/1.2 μm	41/100 GHz	138 V	HRL [52]
Symmetric Slant FPs	1/15/0.25 μm	18.4/65GHz	1400 V	UCSB [53]

Although adding FPs could improve BV, it brings additional parasitic capacitance which limits the operation frequency of GaN HMETs. Especially for the co-integration of GaN HEMTs for MMIC and power switching, it is essential to realize high BV without increasing parasitic capacitance. As shown in Fig. 4(a) and (b), the recessed foot of FP reduce the distance between FP and 2DEG and the SiN dielectric

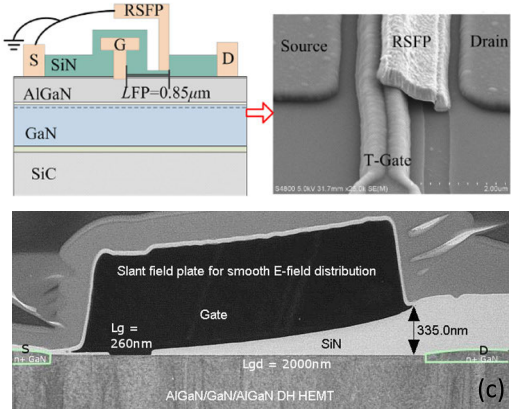


FIGURE 4. (a) The schematic of GaN HEMT with air-bridge recessed source FP; (b) SEM view of fabricated GaN HEMT in [51]; (c) The TEM cross-section of GaN HEMT with slant FP and slope of 6° at the drain-side gate corner.

is replaced by air-bridge with lower dielectric constant [51], which all contributing to less increase in gate capacitance. The slant FP structure in Fig. 4(c) can provide smoother electric field distribution without significant increase in gate capacitance [52].

As for commercial GaN HEMTs, Fig. 5 shows the cross-sectional SEM images of EPC 2045, Panasonic-PGA26E19BA and GaN Systems GS61004B GaN transistors, where the source and discrete FPs are adopted. The possible reason can be intention of limiting the introduction of additional gate capacitance and leaving gate intact for reliability concern in commercial GaN HEMTs.

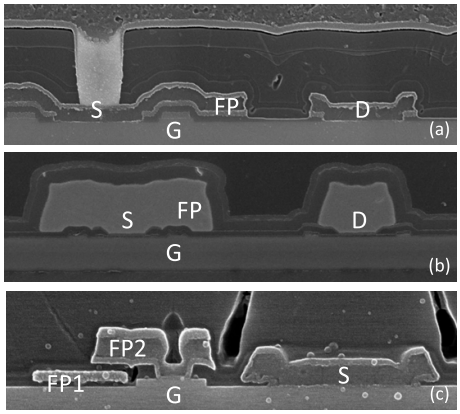


FIGURE 5. The cross-sectional images of (a) EPC2045 100V/16A GaN transistor, (b) Panasonic PGA26E19BA 600V/15A GaN transistor and (c) GaN Systems GS61004B 100V/45A GaN transistor. The contacts and field plates are labelled.

With the help of field plates, the GaN HEMTs for MMIC can have BV up to hundreds of volt with acceptable high frequency operation capability. The optimal GaN HEMTs for MMIC and power switching can probably be co-integrated.

III. GAN POWER INTEGRATION FOR MMICS

The GaN power integration processes for MMICs are the direct heritages of mature GaAs MMIC process. It features the monolithic integration of normally-ON Schottky gate AlGaN/GaN HEMTs, Schottky barrier diodes, thin-film resistors (TFRs), metal-insulator-metal (MIM) capacitors and inductors. Fig. 6 demonstrates the schematic cross-section of a typical 100 nm GaN-on-Si MMIC process from OMMIC [54].

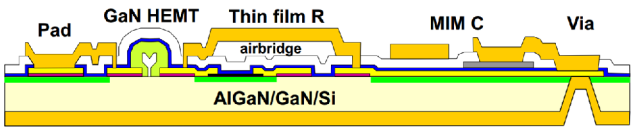


FIGURE 6. Schematic cross-section of an example 100nm GaN-on-Si process for MMICs [54].

Generally the GaN power integration platform can offer 0.5 μm and 0.25 μm HEMTs to replace high power LDMOS ($>$ 100W), or 0.1 μm and 0.06 μm HEMTs to replace GaAs devices in MMICs to offer high performance wide-band-gap (WBG) solutions up to 500 GHz for markets including mobile devices, communications infrastructure, and aerospace applications. The high frequency (operating frequency $>$50 GHz) power amplifiers (PAs) are the major category of GaN MMICs, while other categories include high linearity low noise amplifiers (LNAs), Voltage-Controlled-Oscillators (VCOs), transmitter/receiver and modulator components. In order to have a comprehensive review of the evolution of GaN MMIC process, the reported MMICs are reviewed in terms of critical gate length which represents the core technology parameter, fabrication institute, operation frequency and PAE of PAs, and other key performance.

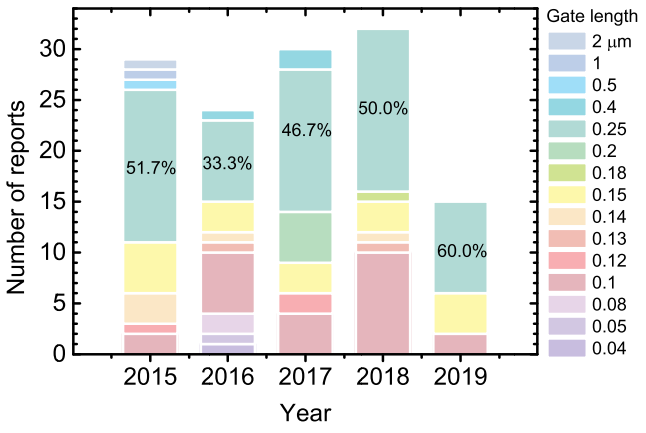
A. GATE LENGTH

The gate length is the determining factor for operation frequency of GaN HEMTs. Along with the scaling down of critical dimensions in IC industry, the gate length in MMIC platform has been scaled down to sub-micron level. Besides conventional optical lithography, electron-beam lithography (EBL) is used in aggressively scaled technologies. The device performance includes the maximum power-gain cutoff frequency f_{max} which is the maximum frequency at which there is still a power gain. It can be expressed as [55]

$$f_{\max} \approx \frac{f_T}{2\sqrt{\left(R_i + R_s + R_g\right)/R_{ds} + \left(2\pi f_T\right) R_g C_{gd}}}, \quad (1)$$

where f_T is the current-gain cutoff frequency; R_i, R_s, R_g, R_{ds} are respectively the gate-charging, source, gate and output resistance; C_{gd} is the gate-drain capacitance. All the denominator parameters need to be reduced to realize high f_{max}. The down-scaled gate length effectively decreases C_{gd} while shorter source-drain length can bring lower R_{ds}. The parasitic components in contacts and interconnects affect the R_s and R_g, which can be suppressed in optimized integration schemes.

Fig. 7 shows the annual number of reports on MMICs from 2015 to August 2019 in terms of gate length values. Although the data are non-exhaustive, the 0.25 μm gate



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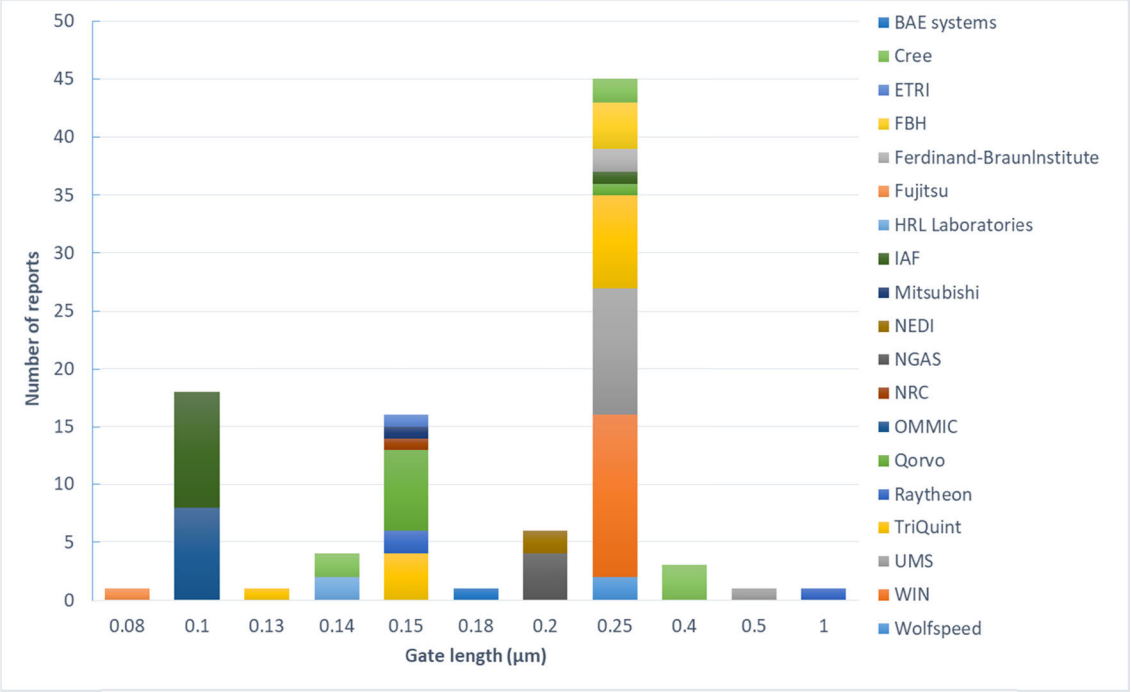

FIGURE 8. Number of reports on MMICs in term of fabrication locations. Data are retrieved from publications in IEEE Xplore and Web of Science.

length MMIC process has been the major choice among the total 130 reviewed reports in scientific research area. The percentage has been over 33.3 % throughout these years. This can be attributed to the acceptable balance between device performance and fabrication cost. Aggressively scaled process, i.e. gate length in tens of nanometers, has been demonstrated by HRL laboratory in 2016 [15]. In Fig. 7, the high proportion of the commercial 0.25 μm processes in cited papers can reflect its popularity, accessibility and maturity in industrial companies and research institutes. Fig. 8 shows the fabrication location of the reported works.

The reviewed companies or institutes are non-exhaustive and have not included the change of company names after capital acquisitions, such as TriQuint with Qorvo. Total 19 units are counted out of 97 publications from 2015 to August 2019. It is obvious that 0.25 μm process has drawn most attentions in companies and institutes. There are 9 units (47.4 % of total units) contributing 45 reported works (46.4 % of total reviewed publications) which adopt the 0.25 μm process. The companies using 0.25 μm process include WIN semi, UMS, Qorvo (with TriQuint), Wolfspeed and so on. For example, Fig. 9 demonstrates the Wolfspeed's 0.25 μm T-gate GaN HEMT MMIC technology with source field plate. The process platform includes low resistance TFRs, MIM capacitors and 18 GHz normally-ON HEMTs (gate length of 0.25 μm) on 4-mil SiC substrate.

B. PERFORMANCE OF GAN MMICS

The majority type of MMICs is the microwave power amplifiers (PAs). GaN MMIC PAs are specifically designed

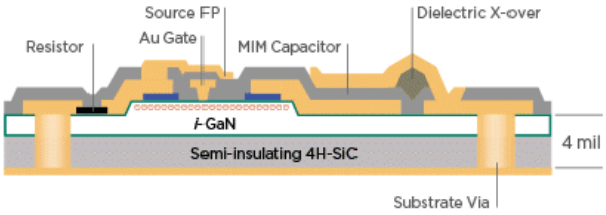

FIGURE 9. Schematic cross-section of Wolfspeed' 0.25 μm GaN MMIC technology.

for mainstream 3G/4G/5G base station architectures, which should meet requirements of massive antenna arrays in power density and efficiency, and they can surpass the performance of LDMOS technology. The parameters of the MMIC performance mainly include operation frequency, output power and power added efficiency (PAE). Here the performance of GaN MMICs with the state-of-the-art processes is discussed in terms of gate length, which is the critical dimension of fabrication process. Fig. 10 shows the output power of reported PAs from 2015 to August 2019.

As can be seen from Fig. 10, the range of output power of reported PAs with smaller gate length (<0.2 μm) is lower, while 0.25 μm PAs have output power ranging from 1 W to 75 W. Other than the different application background of PAs with various operation frequencies, the difference of output power capability can be related with the structures of HEMTs. GaN HEMTs with smaller gate length typically have smaller source-drain distance in order to obtain high device cut-off frequency. The device breakdown voltage as well as the power handling capability is limited. For example,

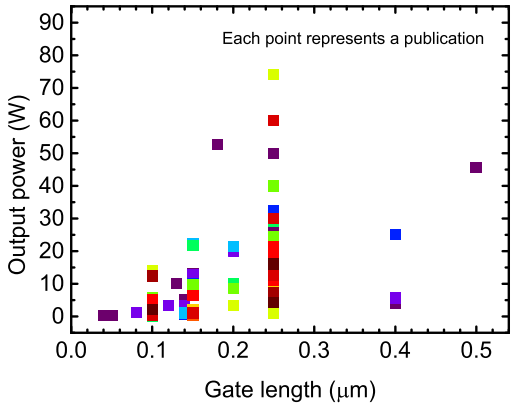

FIGURE 10. Output power of reported PAs in term of gate length in publication from 2015 to August 2019.

the GaN HEMTs fabricated by Wolfspeed's 0.25 μm process can operate under drain bias of 28-40 V with breakdown voltage larger than 120 V and power density over 6 W/mm. In comparison, GaN HEMTs using 0.15 μm process can be biased at only 28 V, the breakdown voltage is larger than 84 V and the power density is only 3.75 W/mm.

The operation frequency and efficiency of PAs are related with amplifier class. According to the operating mechanism, PAs are divided into conventional PAs (Class A, B AB and C) and switching mode PAs (Class D, E, F and so on). The Class A and AB PAs have relative higher linearity but lower efficiency, typically less than 60 %. The structure of Class AB in conventional PAs is simple and regarded as the trade-off between linearity and efficiency. However, its deterioration of linearity is large when operating at high efficiency. In comparison, switching mode PAs show high efficiency but less linearity than conventional PAs. The theoretical efficiency of Class D, E and F PAs can be 100 % while the typical value is 70 % to 90 %. For applications including wireless communication systems, phased array radars and active imagers, different demands in efficiency and linearity require different optimization of PAs. Fig. 11 shows the operation frequency and PAE of the reported PAs with different device gate length to provide an intuitive understanding of relationship between amplifier performance and device structure.

Fig. 11(a) shows that the operation frequency of PAs is obviously increasing with smaller device gate length, and can be up to several hundreds of GHz. Relatively high frequency (>100 GHz) can be achieved through process with gate length < 0.15 um. On the other hand, the PAE generally decreases with smaller gate length. Fig. 11(b) shows the decreasing trend of PAE in terms of frequency of 0.25/0.15/0.1 um processes. In early works on X-band and below, gate length is above 0.5 μm and the device f_T is 20-40 GHz. The PAs are working in deep A/B-class and the PAE are relatively higher. With the decrease of gate length and increase of frequency, PAE decreases together with gains. From Fig. 11, the choice of process for up to hundreds of GHz application can be the 0.1 μm and 0.15 μm process. They are expected to provide both better frequency and PAE at the same time compared with 0.25 μm process. Fig. 12 shows two typical optical images of fabricated PAs. Wu et al. realize a peak output power of 1.66 W with a peak PAE of 35% in a continuous-wave mode at 93 GHz using 0.1 μm process [48]. Youn et al. realize a peak output power of 9.03 W with a peak PAE of 35% under CW operation at 21.5 GHz using 0.15 μm process [56].

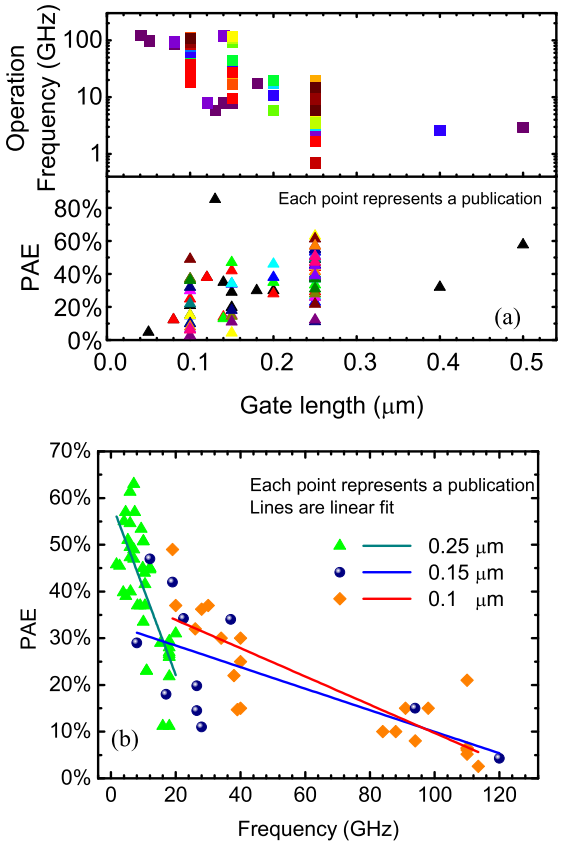

FIGURE 11. (a) Operation frequency and PAE of reported PAs in term of gate length; (b) relationship between PAE and frequency of 0.25/0.15/0.1 μm processes in publication from 2015 to August 2019.

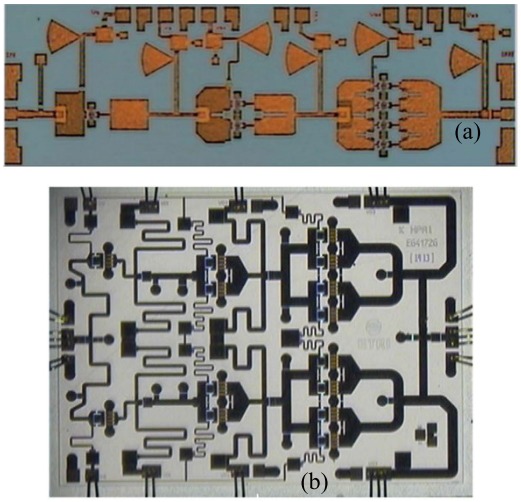

FIGURE 12. Optical images of the fabricated MMIC PAs from (a) [48] with 0.1 μm process and (b) [56] with 0.15 μm process.

IV. GAN POWER INTEGRATION FOR SMART POWER CONVERSION ICS

The GaN power integration for smart power conversion ICs is expected to improve the efficiency of DC power converters by replacing the switching transistors and Schottky diodes with GaN devices. The above mentioned MMIC process can form GaN integrated converters operating at very high frequencies [21], [22], [57]. However, the Schottky gate of AlGaN/GaN HEMTs restricts the input voltage swing, and the gate leakage current could cause deterioration in analog function of integrated circuit components. The negative normally-ON threshold voltage and Schottky gate require extra matching network or off-chip Field-Programmable Gate Array (FPGA) to obtain negative control signal with proper swing. So the integration with normally-OFF MIS-HEMTs is a promising solution for high frequency and high efficiency power conversion application.

A. INTEGRATED COMPONENTS

The smart power IC platforms can be categorized in terms of gate dielectric structure and normally-OFF technology. With the proposal of every normally-OFF technology, a novel platform can be formed based the integration of normally-ON and normally-OFF devices. Fig. 13 illustrates the schematic of smart power IC platforms using gate recess [58], fluorine-ion implantation [59] or p-type cap layer [60] technology.

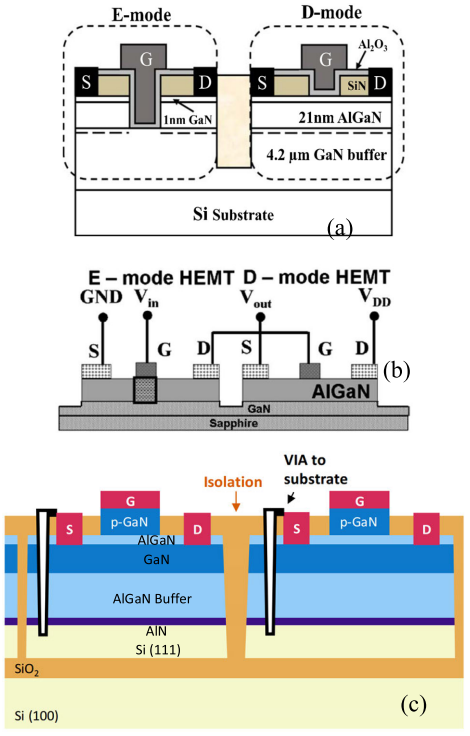

FIGURE 13. Schematic of smart power IC integration platforms using (a) gate recess [58], (b) fluorine-ion implantation [59] and (c) p-GaN cap layer [60] technology.

The isolation is formed by deep mesa or ion-implantation to remove the 2DEG channel between devices. Mesa depth values up to 500 nm are reported [61] to reduce leakage current among devices. However, deep trench makes interconnection more difficult and brings extra surface traps. Implantation isolation uses high energy ions (Ar, F, H, He, N, O) to destroy or deplete the 2DEG channel [62], [63], which can provide flat device surface and is beneficial for lateral metal interconnection. The GaN-on-SOI (Silicon-on-Insulator, SOI) approach has been reported in [38], [64]. The devices are isolated by trench etching until the buried SiO_2 layer and refilling deposition of SiO_2 passivation in the trenches as shown in Fig. 13(c). Especially Interuniversity Microelectronics Center (IMEC) has launched their 200-nm GaN-on-SOI platform and provides Multi-Project Wafer (MPW) runs for power devices and smart power ICs.

Diodes are essential devices to provide high voltage single direction blocking state in power ICs, and also can be used as voltage level shifter which takes advantage of its forward voltage drop. Most common is the Schottky barrier diode (SBD) which is formed by deposition Ni-based metal on AlGaN or GaN surface [65], [66] as shown in Fig. 14(a). Chen et al. [67] firstly introduces the Lateral Field Effect Rectifiers (L-FERs) which uses a Schottky-gate-controlled 2DEG channel between anode and cathode. The lateral device structure and process compatibility with AlGaN/GaN HEMT make the L-FER a well-qualified candidate in smart power IC platform [39], [68] as shown in Fig. 14(b). In Fig. 14(c) the tri-gate Schottky diodes are based on the tri-anode structure with Schottky contact to the multi-channels through the fin sidewalls to obtain lower turn-on voltage [69]. It also exhibits great potential in working with normally-OFF AlGaN/GaN

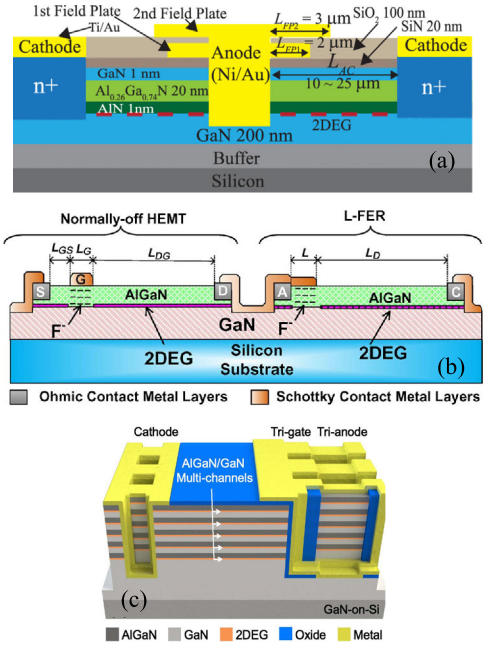

FIGURE 14. Schematic structure of (a) a typical Schottky barrier diode [66], (b) a L-FER with a normally-OFF HEMT [67] and (c) a tri-gated Schottky barrier diode [69].

Fin-FETs. Other reported vertical Schottky diodes are not feasible for lateral integration.

Passive components can be included in smart power IC platforms through the conventional MMIC IPD process. Thin film resistors include poly silicon, TaN and NiCr deposition. The 2DEG channel with controllable electron density can serve as a resistor but with larger temperature coefficient [29], [70]. MIM capacitors use the passivation layer (e.g. SiN_x) or gate dielectric layer (e.g. Al_2O_3, HfO_2) as insulator. The capacitance density is usually below 1 nF/mm^2 for MIM structure with single or multiple SiN_x passivation as insulator [71]. Generally the inductor is not preferred in ICs. However in high frequency GaN based power converters, inductance and volume can be reduced when operation frequency is at MHz range. On-chip spiral inductor which is formed by deposition of metal routes can be a practical solution. Fig. 15 illustrates the process flow of integrated passive devices in smart power IC platforms.

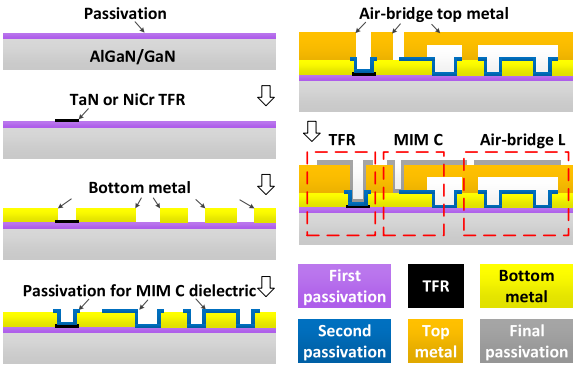

FIGURE 15. Schematic process flow of integrated passive devices in smart power IC platforms.

As the values of inductor required for DC-DC converters are typically in μH scale even for MHz power switching, on-chip integration of inductor in converter ICs is challenging. Several techniques have been reported to realize integrated inductor with inductance value from nH to μH range.

The conventional planar integrated spiral inductor is shown in Fig. 16(a). Low resistivity Cu layer with increased thickness is adopted to reduce inductor parasitic resistance. Additional thick isolation layer, such as low κ BCB material, is deposited to separate inductor from substrate to reduce the losses. This method is relatively simple but the realized inductance is low to several nH [72]. Fig. 16(b) shows the integrated inductors on Si interposer, which can provide small-size inductors with inductance up to 80 nH. The capacitors can be integrated on Si interposer as well. However, the thickness of inductor metal is limited due to the interposer volume [73].

Fig. 16(c) demonstrates the silicon-embedded coreless power inductor. The inductor can be fabricated in the substrate layer and connected to the front side through vias. Alternatively the coreless spiral inductors can be embedded in a silicon interposer and connected with other chips such as

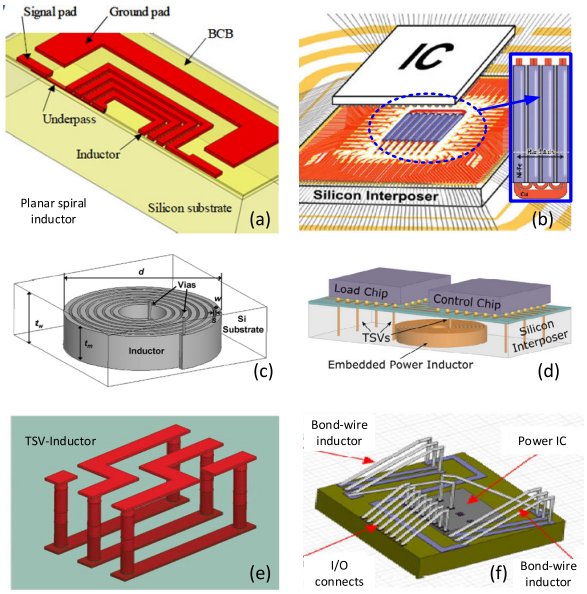

FIGURE 16. Schematics of (a) planar spiral inductor, (b) integrated inductor on Si interposer, (c) substrate embedded coreless power inductor, (d) Interposer embedded coreless inductor, (e) through silicon via (TSV) inductor and (f) bond-wire inductor.

GaN HEMTs through the front-side metal routing and vias as show in Fig. 16(d). The inductance can be up to several μH and the size of the system can be reduced by 5 times compared to the discrete counterparts [74]–[76].

Fig. 16(e) and (f) illustrate the reported through-silicon-via (TSV) inductor in a 3D integrated circuit and bond-wire inductor, respectively. The fabrication techniques are compatible with GaN HEMT process, however, the realized inductance is still small for DC-DC converters [77], [78].

TABLE 2. Integrated converters using normally-OFF HEMT technology.

Inductor type	inductance	frequency	Quality factor	author
Planar spiral inductor	0.5 nH	2.4 GHz	45	ASEI [72]
Integrated inductors on Si interposer	80 nH	36 MHz	-	Univ. of Tokyo [73]
Substrate embedded coreless power inductor	13.1 nH	100 MHz	3.9	HKUST [74]
	2-4 µH	2-5 MHz	18-23	HKUST [75]
Interposer - embedded coreless inductors	4.2 µH	10 MHz	-	HKUST [76]
TSV inductors	1.73 nH	200 MHz	6.1	Univ. of Notre Dame [79]
Bond-wire inductors	450 nH	5 MHz	-	UCF [78]

The reported performance of integrated inductors is summarized in Table 2. Inductance values are still in nH to μH range with Q factor below 50. Especially the embedded coreless power inductor technique can realize inductance in the range of μH, which is a promising solution for integration of large value inductors in power converter ICs.

B. INTEGRATED DC-DC CONVERTERS

Achieving higher operation efficiency to reduce losses during power conversion is one of the key concerns in power DC-DC converters. The research groups and industry leading companies have first time switched to GaN solution to pursue higher performance. The discrete approach using discrete GaN switches has shown great improvement in converter operation frequency and efficiency. The controller, protector and driver are dedicated Si-based ICs, which are mounted on the same PCB with GaN switches and passive components. Since 2007, converters with GaN normally-ON HEMT as high-side switch and SiC-SBD as low-side switch have demonstrated efficiency up to 97.8 % at MHz range [80]. With normally-OFF HEMT as high-side switch, Transphorm realizes a 3kW, 99 % converter at 100 kHz [81]. When using GaN SBD as low-side switch, the converter shows an efficiency of 98.5 % at 500 kHz and 500 W condition [82]. Lots of works adopt normally-OFF half-bridge structure, the high efficiency of 98.8 % is realized at 50 kHz by University of Southern Denmark [83] and high output power of 3.3 kW is realized at 300 kHz by Fudan University [84]. These cases have substantially shown the advantages of GaN based discrete DC-DC converters.

Further exploiting the properties of GaN devices, the road of integration starts. The integrated GaN converters are reviewed in terms of the fabrication technology of smart power IC platforms.

1) COMMERCIAL MMIC TECHNOLOGY

As stated in Section I and III, DC-DC converters for on-chip power supply of PAs, or for switching mode power amplification can be fabricated through the GaN MMIC technology. Table 3 lists the operation condition and performance of the reported converters using commercial MMIC process platforms.

TABLE 3. Integrated converters using commercial MMIC technology.

Converter topology	Technology	Max efficiency	Max freq.	Max power	Authors
Boost	0.25-μm GaN/SiC	34%	680 MHz	2.2 W	MIT [85]
Buck	0.15 μm	78%	246 MHz	-	Mitsubishi [86]
Synchronous buck	0.15 um GaN/SiC	90%	100 MHz	5 W	Univ. of Colorado [23]
Synchronous buck	0.15 μm GaN/SiC	90%	100 MHz	7 W	Univ. of Colorado [87]

In Table 3, the converters can operate at hundreds of MHz with high efficiency. Both buck and boost converters have been demonstrated. However the converters developed through this technology are mostly aimed at on-chip power supply for envelope tracking PAs. This limited application is related with the small gate length and relatively lower device breakdown voltage and power handling capability than

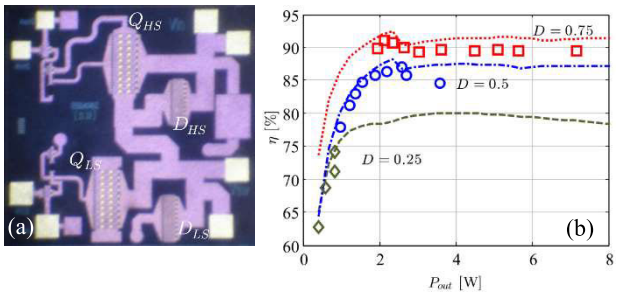

FIGURE 17. (a) Optical image of the integrated half-bridge with integrated gate driver; (b) efficiency versus output of the integrated buck converter [22].

AlGaN/GaN power MIS-HEMTs. Fig. 17 demonstrates the optical image and efficiency curves of an example integrated half-bridge converter by Zhang et al. [22]. The curvature of metal routes clearly indicates the transmission line in the MMIC process. The high efficiency over 90 % verifies the advantage of GaN based integrated converters. In order to accommodate the high power, high frequency and high efficiency power conversions, DC-DC power converter are switching to GaN smart power IC platforms with normally-OFF power devices.

2) NORMALLY-OFF HEMT TECHNOLOGY

The conventional normally-OFF technologies which are feasible for device integration have been discussed in Fig. 13. The normally-OFF devices provide fault-safe operation and ease the design of gate driver. Additionally the gate dielectric can be included in devices to form MIS-HEMTs, which can reduce the gate leakage and enlarge the gate voltage swing. Table 4 lists the publications with integrated converters using normally-OFF technologies.

TABLE 4. Integrated converters using normally-OFF HEMT technology.

Converter topology	Technology	Max efficiency	Max freq.	Max power	Authors
Boost	F-ion implantation	84%	1 MHz	-	HKUST [39]
Half-bridge with driver	P-AlGaN cap layer	86.6%	2 MHz	10.8 W	Panasonic [42]
Half-bridge with driver	P-AlGaN cap layer	84.9%	3 MHz	10.8 W	Panasonic [88]
Half-bridge with driver	P-GaN cap layer	-	500 KHz	0.1 W	IMEC [89]
Half-bridge with driver	Gate recess	95%	400 MHz	16 W	Univ. of Colorado [90]
Boost with driver	Gate recess	-	100 kHz	-	XJTLU [58]
Buck with driver	Gate recess	-	100 kHz	0.2 W	NUS [36, 91]

Normally-OFF technology is promising to assist GaN integrated converters to work at MHz range with efficiency up to nighty percent. The output power at current stage is less than

DC-DC converters with discrete GaN power switches, which could be due to the limited total gate width of integrated power stages. Larger power stages are integrated on 200-mm GaN IC platforms now. Ujita et al. has designed a fully integrated GaN-based power IC including gate drivers for high-efficiency DC-DC conversion [88]. The 12-1.8 V DC-DC converter IC demonstrates a maximum 3 MHz frequency, which is far beyond the limit of Si and can reduce 60% of system volume. Fraunhofer IAF has realized an integrated half-bridge converter as shown in Fig. 18, which can be switched at 3 MHz with a input/output of 400/200 V, and a current 1.15 A [92], [93].

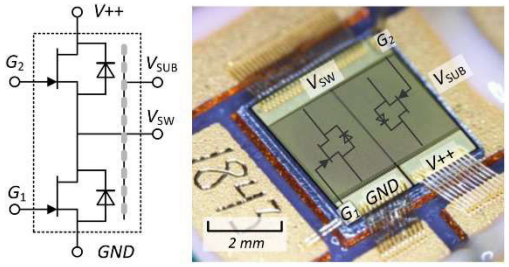

FIGURE 18. Schematic structure and optical image of the integrated half-bridge by Fraunhofer IAF [92], [93].

In the aspects of GaN integration in companies, Navitas and Dialog have lunched the GaN power IC products. Both of these two companies cooperated with TSMC on the practical fabrication. The high-frequency operation of GaN based circuit induces excessive parasitic from wire bonding, which has been reduced by TSMC's integration of peripheral circuits with low-voltage devices into CMOS-compatible 100/650 V enhancement GaN device platform. Functional blocks including control, clock, pre-gate driver, ESD protection circuits have been demonstrated using 12 V E/D-HEMTs, rectifiers. 2DEG resistors and capacitors [9]. Now Navitas' NV6115 can offer high-efficiency 650 V, 160 mΩ power switches with integrated gate drive and logic circuits, which can enable high switching speed, power efficiency and power density. Dialog's DA8801 can offer a half bridge of 650 V, 500 mΩ power switches with integrated analog, logic, and protection.

V. GAN POWER INTEGRATION ROAD AHEAD

GaN integration can take the power conversion to where silicon power cannot go [94]. More technologies in Si electronics have been applied on the GaN integration. The dedicated Si CMOS gate drivers can be packaged in the same case or directly bonded with GaN in 3-dimension. The heterogeneous integration of GaN and Bipolar-CMOS-DMOS (BCD) has been shown by GLOBALFOUNDRIES "GaN2BCD" technology in [95], [96]. The driver circuits can be dedicatedly designed and fabricated in BCD process, and then integrated with GaN power devices using the die-to-wafer transfer (D2W) as shown in the schematic in Fig. 19.

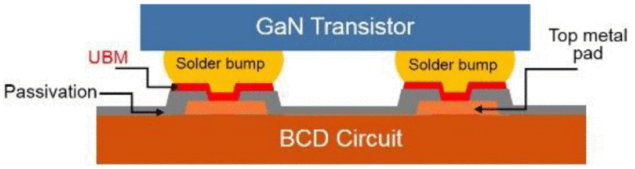

FIGURE 19. Schematic cross-section of the "GaN2BCD" developed by GLOBALFOUNDRIES [95]. The UBM is the abbreviation of under-bumper-metallization.

An open-loop 3.3-70 V boost converter is demonstrated. The 70.3 % efficiency is realized at 49.5 kHz and 1.68 W [95].

Another novel approach is the CMOS gate driver flip-chip assembled with GaN devices together on the IPD substrate, which minimizes the parasitic effects caused by bonding wires [97]. The PCB embedded inductor is also a solution to low parasitic IPDs [98].

Die bonding between CMOS and GaN ICs to form the integrated converter is one of the solutions provided by [99]. The half-bridge switches are AlGaN/GaN HEMTs, while the drivers and other functional circuits are implemented in a 0.18 μm CMOS platform. The GaN and CMOS dies are face-to-face bonded to reduce inductive parasitics. Fig. 20 shows the optical images of silicon die (top), GaN die (middle), and the face-to-face bonding illustration (bottom). The converter demonstrates the 8-to-1 V, 40 MHz and 76 % efficiency opeartion [99].

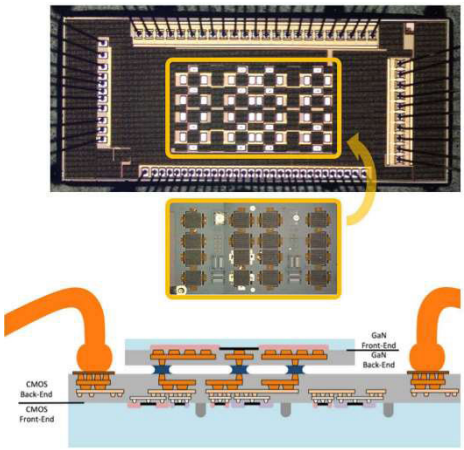

FIGURE 20. Optical images of silicon die, GaN die and face-to-face bonding illustration by Aklimi et al. [99].

The integration on Direct Bonded Copper (DBC) has the GaN power device bonded and other components soldered in the way as shown in Fig. 21 by Fraunhofer IAF in 2019 [100]. A prototype 200-to-100 V, 500 kHz, 100 W, 97% efficiency converter is designed and characterized.

More approaches are being proposed. However, the GaN integration firstly should be established on a stable platform with well calibrated and modelled active and passive components. So the performance of the GaN power ICs can be reliably predicted. The technology of discrete GaN devices

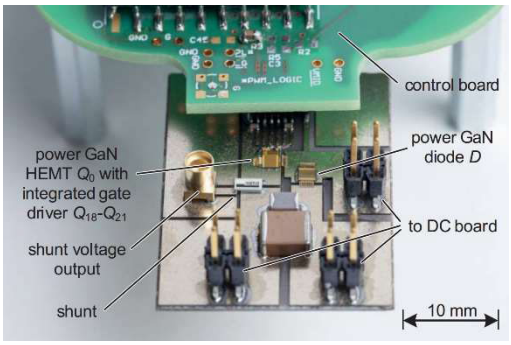

FIGURE 21. Optical image of the power module prototype with GaN power transistor, power diode and passive components mounted on the DBC substrate [100].

is improving fast and the GaN power integration should be updated simultaneously. In order to exploit the most of theoretical GaN performance, GaN power integration road follows the path of Si power IC, but on a fast lane.

VI. CONCLUSION

GaN power integration is the intuitive and effective solution for high frequency and high efficiency power applications including microwave and power conversion. The GaN integration road is reviewed in terms of the technology and application. With the rapid development of microwave communication, the GaN power integration technology based on MMIC platforms are significantly advanced. The 0.25/0.15/0.1 μm processes have been the major choices and highly scaled integration processes have been demonstrated. The state-of-the-art performance of the MMIC PAs is reviewed. The GaN power integration has supported the markets including mobile devices, communications infrastructure and aerospace applications.

On the other hand, smart GaN power IC platforms boost the high efficiency DC-DC power conversions. Numbers of platforms are constructed based on novel device technologies. Demonstrations of high frequency (>1 MHz) and high efficiency (>95 %) DC-DC converters with various kinds of topology have been summarized. Novel integration schemes and methods are introduced to stimulate new thoughts on GaN power integration.

The future of GaN power integration is exciting when considering the full potential of GaN electronics. However, the road is still tough. This review on GaN power integration in terms of high frequency and efficiency power applications could provide some up-to-date information and shed some light on the way.

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