IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 5, 2020, accepted January 10, 2020, date of publication January 15, 2020, date of current version January 24, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2966789

Coupled Thermo-Mechanical Analysis of 3D ICs Based on an Equivalent Modeling Methodology With Sub-Modeling

ZHIQIANG CHENG, YINGTAO DING, ZIYUE ZHANG, MINGRUI ZHOU, AND ZHIMING CHEN
School of Information and Electronics, Beijing Institute of Technology, Beijing 100081, China

Corresponding author: Zhiming Chen (czm@bit.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61774015 and Grant 61574016, in part by the 111 Project of China under Grant B14010, and in part by the Beijing Nova Program of Science and Technology under Grant Z191100001119078.

ABSTRACT The coupled thermo-mechanical field analysis of three-dimensional (3D) stacked integrated circuits (ICs) is evaluated by an efficient and accurate simulation strategy that combines equivalent homogenization modeling methodology and sub-modeling technique. The thermal field is first investigated using the proposed approach, and based on which the structural field is also examined through the calculation of warpage. The utilization of sub-modeling method reveals the local temperature and warpage distributions, which is lost or ignored by the conventional homogenization method. To validate the proposed method, the simulation results of a five-layer stacked integrated circuits are compared against true 3D results of the detailed model, where the maximum deviation for temperature and warpage is as low as 1.62% and 4.89%, respectively, which are greatly improved compared to 8.23% and 7.83% using traditional homogenization method. In addition, the total computation time is reduced by 76.7% in contrast to true 3D finite element analysis (FEA) simulation. Furthermore, the impacts of through-silicon-via (TSV) geometries, underfill and μ-bump parameters on the temperature and warpage distributions are also studied to guide the design of 3D ICs with high performance and reliability.

INDEX TERMS Three-dimensional integrated circuits, coupled thermo-mechanical analysis, equivalent homogenization modeling, sub-modeling technique, through-silicon-via.

I. INTRODUCTION

Recently, three-dimensional (3D) integration has been attracting considerable attention because it vertically stacks multifunction chips by a mass of through-silicon-vias (TSVs) to establish electrical interconnect among stacked chips, thereby overcoming the obstacle encountered during the shrinking of traditional planar integration and realizing complex 3D integrated circuits (3D ICs) with small form factor, high density, and excellent performance [1]–[5]. However, the local heat concentration [6], [7] caused by denser architecture, higher power density, and worse heat dissipation has become a serious challenge in thermal management of 3D ICs, which degrades the electrical performance and reduces the lifetime of devices [8]–[10]. Furthermore, the wafer or chip warpage as well as thermal stress are also inevitably induced inside 3D structure due to non-uniform temperature distribution and large coefficient of thermal expansion (CTE) mismatch among various materials, further undermining the thermo-mechanical reliability of 3D ICs [11]–[13].

So far, several studies were performed to evaluate the thermo-mechanical characteristics of 3D ICs. In terms of experimental approach, various methods were employed to measure the temperature profile and warpage distribution of 3D structure, including thermal test die [14], liquid crystals [15], infrared thermography [16], and shadow moiré method [13]. On the other hand, numerical simulation such as finite element analysis (FEA) was also widely used for thermo-mechanical analysis [17]–[21], including hot spot, process-induced stress/warpage, and even fatigue life. However, due to the multi-scale feature of 3D ICs, implementing a true 3D FEA simulation with all the structural details usually spends enormous computation resources and time, making it impractical. In order to reduce the simulation cost,

The associate editor coordinating the review of this manuscript and approving it for publication was Yu Liu.

several studies were reported, where the FEA simulation was simplified by utilizing an equivalent homogenized model and ignoring the internal details of 3D ICs. For instance, Lau and Yue [21], [22] investigated the equivalent thermal properties of TSV consisting of silicon substrate and copper plug only, and summarized a series of empirical formulas between the equivalent thermal conductivity (TC) and different TSV geometries. Afterwards, Xiao *et al.* [23] further illustrated this numerical method for thermal management of 3D stacked ICs, where the equivalent TC of TSV was obtained from a normalized two-dimensional (2D) model. Besides, the equivalent structural properties of TSV were studied by Che *et al.* [24], [25] for the wafer-level warpage and stress analysis by assuming a uniform temperature load, which usually does not reflect the real case. Similarly, Lee *et al.* [26], [27] investigated the equivalent structural properties of μ-bump surrounded by underfill, and applied it for the failure analysis of a chip stacking packaging. Thanks to the use of equivalent material properties, the numerical simulation of 3D ICs can be greatly simplified in terms of the modeling and solution process. However, after the chip containing TSVs or the interlayer with μ-bump is homogenized with the equivalent thermal and structural properties, its detailed information inside the equivalent block or black box is discarded, thereby resulting in a globally correct but locally inaccurate evaluation for the thermo-mechanical performance of 3D ICs. Therefore, it is highly desired to explore a method, which can accelerate the simulation without losing the detailed local information. What's more, previous studies mainly focus on either thermal or structural field analysis separately, missing a coupled thermo-mechanical evaluation of 3D ICs.

In this paper, in order to solve the above issues, the coupled thermo-mechanical analysis of 3D ICs is performed at the same time to further study the effect of the real non-uniform temperature distribution on its structural performance. Meanwhile, the sub-modeling technique is employed to overcome the inherent weakness of the equivalent homogenization method without increasing simulation costs significantly. To evaluate the accuracy and applicability of this simulation strategy, a 3D model with TSV array is built and analyzed, and the results agree well with the true 3D FEA simulation with much reduced simulation cost. Moreover, the accuracy of the numerical results is also improved compared to the traditional homogenization method. And the effects of material and geometric dimensions of TSV array, underfill, and μ-bump are explored to provide insights for the design of highly reliable 3D products.

II. MODELING METHODOLOGY AND SIMULATION STRATEGY

A. HOMOGENIZATION METHOD WITH SUB-MODELING TECHNIQUE

Typically, the TSV array is usually fabricated uniformly in a silicon substrate, so that it can be viewed as a unidirectional fiber reinforced composite [28], and a representative volume element (RVE) model [29] can be extracted to represent this TSV array, as shown in Fig. 1. And then, according to the micromechanics theory of composites as well as the heat transfer theory, the homogenization method can be applied to simplify the FEA simulation of 3D ICs with TSV array. Fig. 2 shows the homogenization method of TSV model together with the sub-modeling technique adopted in this work. First, the RVE model of a TSV consisting of central copper plug, SiO_2 sidewall liner, surface dielectrics and silicon substrate is replaced by a homogeneous material with some equivalent thermal and structural properties including TC (k), stiffness matrix (C), and CTE (α). It should be noted that this RVE model will be viewed as a black box after using the equivalent method, and its inner structural details will be ignored. Next, the equivalent model of 3D ICs is constructed utilizing the homogenized material above for following thermal and structural analyses, after which the global temperature and warpage distributions are obtained. And then, the sub-modeling technique [30] is further employed to retrieve the detailed thermal and structural fields within the black box considering the fact that it can obtain more accurate results in the region of interest. More precisely, a detailed local TSV model with fine mesh is constructed and simulated using the global results obtained from the previous simulation to reveal the temperature and warpage information inside the black box more accurately, as shown in Fig. 2.

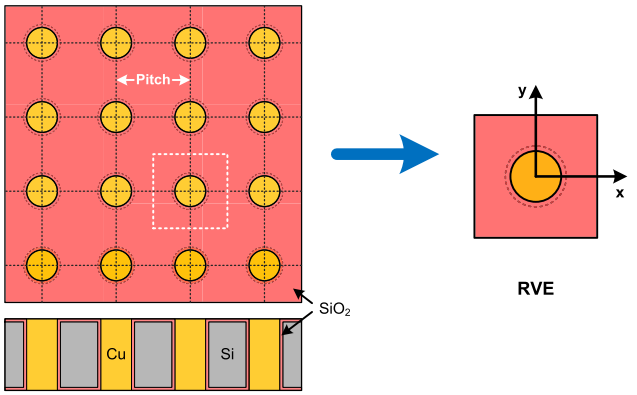


FIGURE 1. The TSV array and its RVE model.

B. EQUIVALENT THERMAL PROPERTIES

Fig. 3 shows the approach for extracting the equivalent TC from the RVE model along z and x directions, respectively, from which it can be seen that the equivalent TC along x direction should be the same as that along y direction, but different from that along z direction, indicating an orthotropic feature of the RVE model. In order to extract the equivalent TC along z direction, two different temperature boundary conditions, T_1 and T_2, are applied to the top and bottom surfaces of the RVE model, respectively, while the adiabatic boundary condition is imposed to other four sides, as illustrated by Fig. 3(a). And the similar boundary conditions are applied

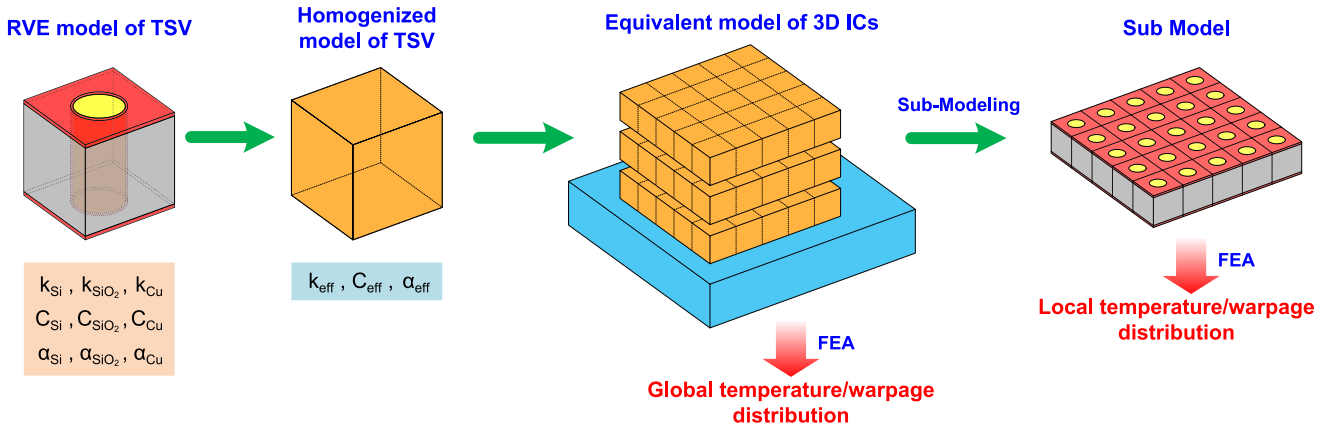


FIGURE 2. The FEA analysis flow: the equivalent homogenization method with the sub-modeling technique.

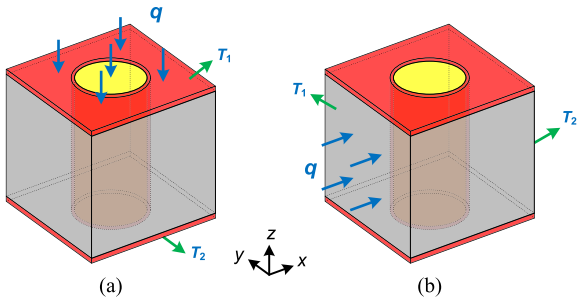


FIGURE 3. The schematic for extracting the equivalent TC (a) along z direction and (b) along x direction.

to extract the equivalent TC along x direction, as shown in Fig. 3(b). After the heat flux q along z or x direction is calculated using FEA software, the equivalent TC along the corresponding direction can be obtained by:

$$k_z = -q_z \frac{\mathrm{d}z}{\mathrm{d}T} = \left| \frac{q_z \cdot \Delta z}{\Delta T} \right| \tag{1}$$

$$k_{x,y} = -q_x \frac{\mathrm{d}x}{\mathrm{d}T} = \left| \frac{q_x \cdot \Delta x}{\Delta T} \right| \tag{2}$$

where $\Delta T = T_1 - T_2$, Δx and Δz represent the distance between the two surfaces where the temperature boundary conditions are applied.

C. EQUIVALENT STRUCTURAL PROPERTIES

Similar to the equivalent TC, the RVE model of TSV can also be treated as an orthotropic homogeneous material for structural analysis. Thus, six equivalent material properties need to be determined to form a stiffness matrix, including two Young's moduli ($E_{x,y}$ and E_z), two Shear moduli (G_{xy} and G_{xz}), and two Poisson's ratios (ν_{xy} and ν_{xz}). Besides, two equivalent CTEs ($\alpha_{x,y}$ and α_z) should be extracted as well.

1) STIFFNESS MATRIX

To obtain the equivalent Young's modulus and Poisson's ratio of the RVE model, a unidirectional tensile simulation is implemented. During this FEA simulation, a small displacement constraint U, which produces a uniform normal tensile strain ϵ along its traction direction, is applied to the top (or left) surface of the RVE model, while a fixed constraint is imposed to the opposite surface, where a normal reaction force F is induced, as shown in Fig. 4(a) and 4(b). And the equivalent Young's modulus (E) along z and x directions as well as the equivalent Poisson's ratio (ν) along xz and xy planes can be written as:

$$E_z = \frac{\sigma_z}{\epsilon_z} = \frac{F_z}{A_z \cdot \epsilon_z} \tag{3}$$

$$E_{x,y} = \frac{\sigma_x}{\epsilon_x} = \frac{F_x}{A_x \cdot \epsilon_x} \tag{4}$$

$$\nu_{xz} = \left| \frac{\epsilon_z'}{\epsilon_x} \right| \tag{5}$$

$$\nu_{xy} = \left| \frac{\epsilon_y'}{\epsilon_x} \right| \tag{6}$$

where σ_z and σ_x stand for the normal stress along z and x directions, respectively. And ϵ_z and ϵ_x represent the normal tensile strain when the tensile load is applied along z and x directions, respectively, while ϵ_z' and ϵ_y' are the normal shrinking strain along z and y directions due to the tensile load along x direction. A_x and A_z denote the cross-sectional area of the RVE model perpendicular to x and z directions, respectively.

Fig. 4(c) and 4(d) illustrate the method to obtain the equivalent shear modulus, where a displacement constraint U parallel to the surface of the model along z or y direction is applied to the left surface of the RVE model, thereby producing a shear strain γ on this surface. Meanwhile, a fixed constraint is applied to its opposite (right) surface, where a shear reaction force F is induced. And then, the equivalent shear modulus can be calculated as following:

$$G_{xz} = \frac{\tau_{xz}}{\gamma_{xz}} = \frac{F_{xz}}{A_x \cdot \gamma_{xz}} \tag{7}$$

$$G_{xy} = \frac{\tau_{xy}}{\gamma_{xy}} = \frac{F_{xy}}{A_x \cdot \gamma_{xy}} \tag{8}$$

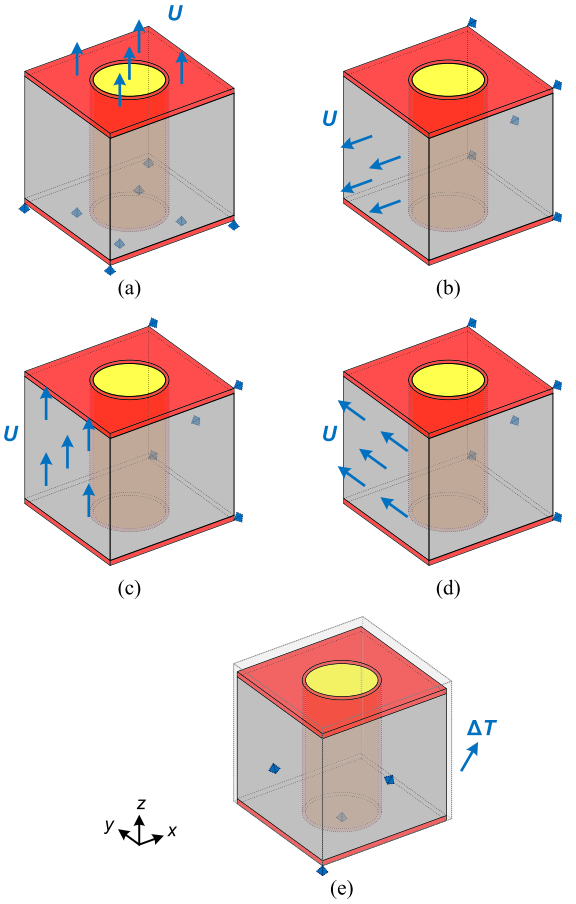


FIGURE 4. The schematic for extracting structural parameters: Young's modulus & Poisson's ratio along (a) z direction and (b) x direction, Shear modulus along (c) xz plane and (d) xy plane, and (e) CTE along x and z directions.

where τ_{xz} and τ_{xy} stand for the shear stress along xz and xy planes, respectively, while γ_{xz} and γ_{xy} are the shear strain along xz and xy planes due to the shear displacement. After calculating the six equivalent properties above, a stiffness matrix representing the fundamental structural property of the aforementioned homogeneous material can be obtained for subsequent numerical simulation.

2) CTE

Fig. 4(*e*) shows the method utilized to extract the equivalent CTE of the RVE model, where a temperature raise of ΔT is loaded onto this RVE model. As for the boundary condition, three adjacent surfaces are fixed to restrict the motion along their normal directions, while the other three surfaces are constrained to translate along their normal directions [31]. When the ambient temperature changes, the thermal strain ϵ^T is induced, and then can be calculated based on the thermal deformation of the model. Hence, the equivalent CTE along x and z directions can be expressed as:

$$\alpha_{x,y} = \frac{\epsilon_x^T}{\Delta T} \tag{9}$$

$$\alpha_z = \frac{\epsilon_z^T}{\Delta T} \tag{10}$$

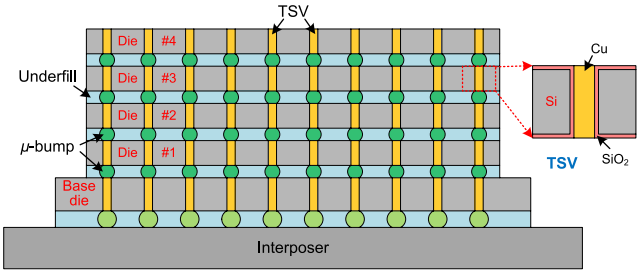


FIGURE 5. A 3D model consisting of five layers of stacked dies on top of a silicon interposer.

where ϵ_x^T and ϵ_z^T represent the induced thermal strain along x and z directions due to the temperature change, respectively.

III. VERIFICATION OF THE PROPOSED METHOD

To evaluate the accuracy and feasibility of the proposed method, a 3D model including five layers of stacked dies on top of a silicon interposer is constructed, and μ-bumps made of copper and surrounded by underfill are utilized for interlayer connection, as shown in Fig. 5. In this 3D model, the top four dies have the same geometric size (0.5 mm $\times$ 0.5 mm $\times$ 0.05 mm), while the base die has a slightly larger size (0.6 mm $\times$ 0.6 mm $\times$ 0.065 mm). Meanwhile, there are 100 (10 $\times$ 10) TSVs with a diameter of 10 μm and a pitch of 50 μm in each die. Table 1 lists all material properties used in the FEA simulation and all materials are assumed to be isotropic, while the temperature dependent material properties as well as the elastic-plastic characteristics of copper are considered [32]. Three kinds of modeling and simulation strategies are applied, including (1) simulation based on a detailed 3D finite element model (FEM); (2) simulation based on an equivalent homogenized FEM, where the stacked dies containing TSV array are modeled by a lumped homogeneous material with the orthotropic equivalent properties obtained in Section II-B and Section II-C; (3) simulation based on an equivalent homogenized FEM with the sub-modeling technique. In this coupled thermo-mechanical simulation, the commercially available software ANSYS 17.0 is employed to assess the computation resource and simulation accuracy among the above three modeling and simulation strategies, while all models are mesh by quadratic elements with 20 nodes (e.g. thermal SOLID90 and structural SOLID186 element type). During the thermal analysis, the top four dies and the base die are assumed as heat sources with power generation of 0.4 W and 0.8 W, respectively. Meanwhile, the heat sink is involved in the above models to provide an efficient heat diffusion path for 3D ICs [33], [34]. The ambient temperature is 25 °C, at which all materials are assumed to be stress-free. Afterwards, the temperature field obtained from the thermal analysis is employed as the thermal load to implement the structural analysis, while the vertical displacement at the bottom surface of the models is constrained to prevent from moving up and down.

To illustrate the difference of the above three simulation strategies clearly, a cross section is first selected along the

TABLE 1. The thermal and structural properties of materials.

Materials	Young's Modulus [GPa]	Poisson's ratio	Shear Modulus [GPa]	CTE [ppm/K]	Thermal conductivity [W/(m·K)]
Silicon	131	0.28	51.17	2.8	150
SiO_2	73	0.17	31.20	0.5	1.5
Copper	121-110 (27-260 °C)	0.3	46.54-42.31 (27-260 °C)	17.3	390
BCB	3.0	0.34	1.12	42.6-55.3 (25-125 °C)	0.29
Polyimide (Kapton MT+)	2.48-1.62 (23-200 °C)	0.34	0.93-0.6 (23-200 °C)	20-32 (25-200 °C)	0.8
Epoxy	5.5-0.1 (25-150 °C)	0.3-0.49 (25-150 °C)	2.12-0.03 (25-125 °C)	58-175 (25-150 °C)	0.23
Au	79	0.42	27.82	14	315
Sn	45	0.33	16.92	23.8	62.8-56.5 (0-200 °C)

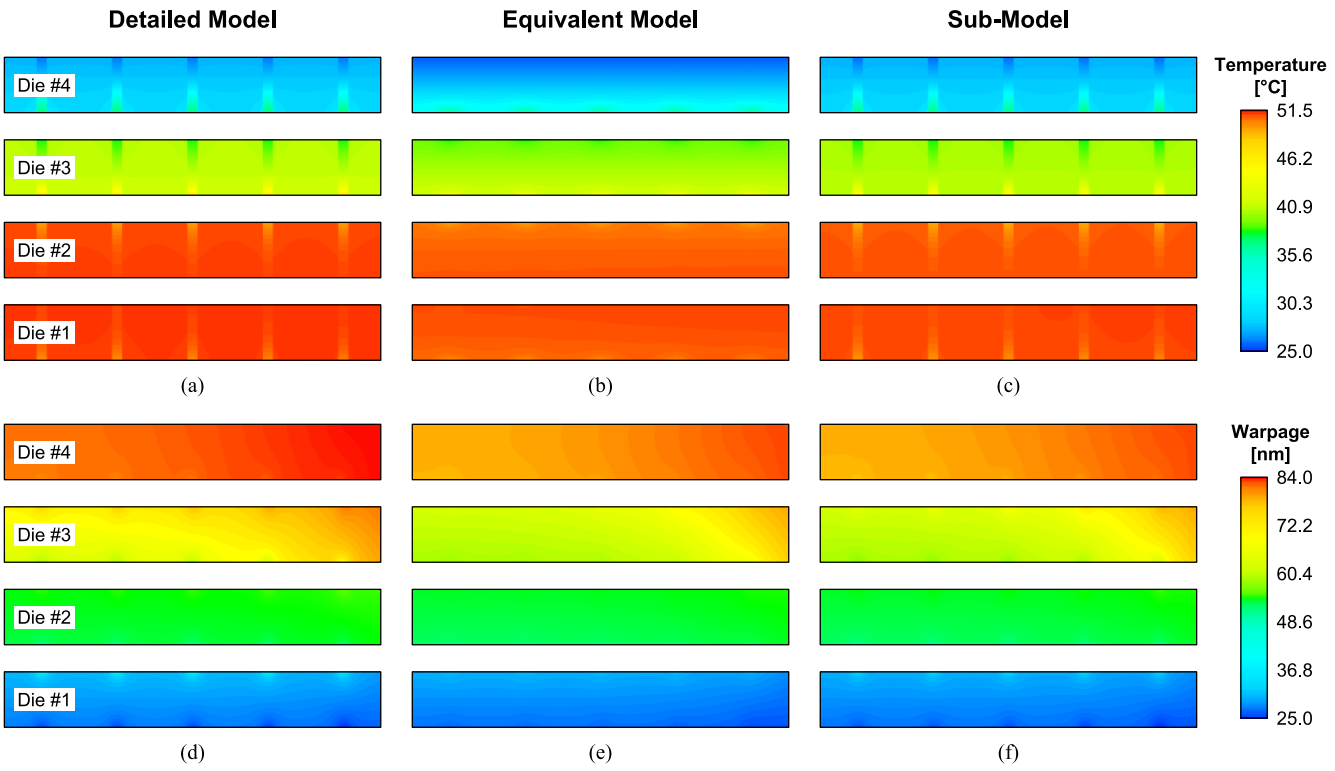


FIGURE 6. The temperature and warpage distributions of the section selected along the diagonal of the 3D model: (a) the temperature profile of the detailed model; (b) the temperature profile of the equivalent model; (c) the temperature profile of the sub-model; (d) the warpage distribution of the detailed model; (e) the warpage distribution of the equivalent model; (f) the warpage distribution of the sub-model.

diagonal of the 3D model from center to edge, and then the temperature and warpage distributions are plotted in this section. Fig. 6(*a*) and 6(*b*) show the temperature profiles obtained from the detailed model and the equivalent model. It can be seen from Fig. 6(*a*) and 6(*b*) that Die #1 exhibits maximum temperature of 50.14 °C and 49.56 °C for the detailed model and the equivalent model respectively, and the deviation of maximum temperature between both FEMs is about 1.2%, verifying the accuracy and capability of the equivalent method in terms of global thermal analysis. It should be noted that the maximum temperature locates in the interior of the 3D model rather than the top owing to an efficient heat diffusion path provided by the heat sink. Likewise, Fig. 6(*d*) and 6(*e*) show the warpage contours of the detailed model and the equivalent model respectively, where the maximum warpage occurs near the edge of Die #4 with the magnitude of 83.54 nm and 79.95 nm for the detailed model and the equivalent model, respectively. Therefore, the deviation in terms of maximum warpage is about 4.3%, further proving the applicability of the equivalent method for global structural analysis. The reason why the maximum warpage occurs in the top layer of the 3D model should be related to the choice of the reference plane for warpage calculation. In the structural analysis, the warpage value shown in Fig. 6 is referred to the bottom surface of the whole 3D model, thus the warpage of the i^{th} die will be accumulated on the warpage

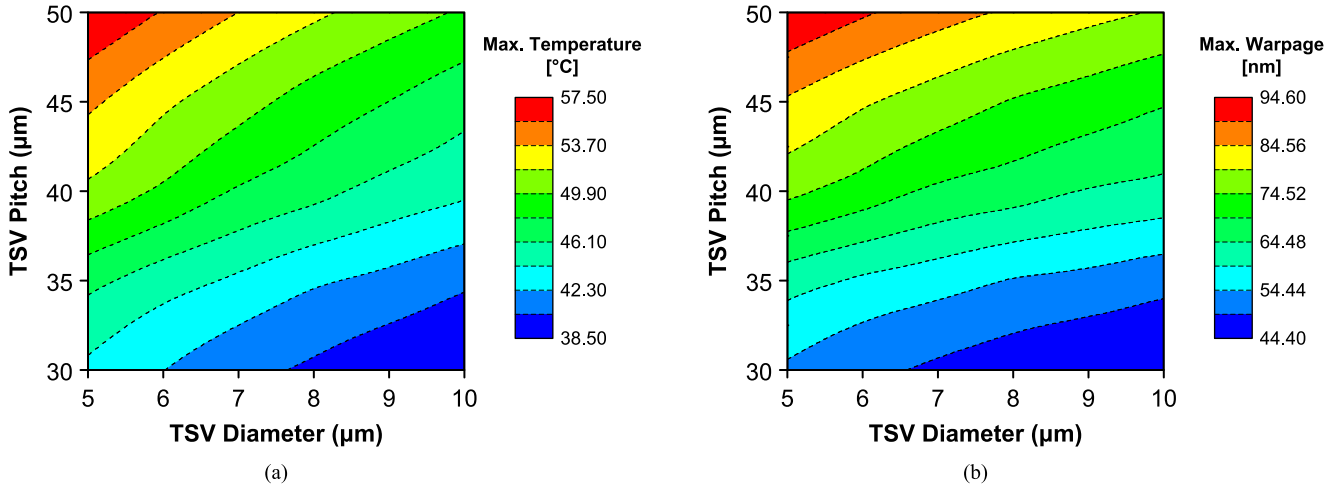


FIGURE 7. The impacts of TSV diameter and pitch on (a) the maximum temperature and (b) the maximum warpage.

of the $(i + 1)^{th}$ die located one layer above. In addition, it is worth mentioning that the detailed model is meshed with 4774345 nodes and 1177152 elements. In contrast, in the equivalent model, the node and element decrease by 51% and 55%, respectively. As a result, only 12.2 hours are taken during the simulation of the equivalent model using four *Intel Xeon E5-4627 V2* central processing units (CPUs) and 256 GB memory, while the total computation time is 53.9 hours for the detailed model.

TABLE 2. The maximum deviation of the equivalent model and the sub-model compared to the detailed model.

Deviation	Equivalent Model		Sub-Model	
(%)	Temperature	Warpage	Temperature	Warpage
Die #1	3.56	7.83	1.03	3.76
Die #2	4.00	6.82	1.22	4.69
Die #3	7.71	6.06	1.62	4.89
Die #4	8.23	4.84	1.08	4.70

Although the maximum temperature and warpage distributions from the equivalent model are similar to the detailed model in general, the considerable deviation occurs in the region around TSVs, which can be seen from Fig. 6(*a*) and 6(*b*). Table 2 presents the maximum deviations of temperature and warpage distributions between the detailed model and the equivalent model for each die, where maximum deviations are 8.23% and 7.83% for temperature and warpage, respectively, indicating the weakness of the equivalent method in terms of local thermal and structural field calculations. To overcome the aforementioned limitation of the equivalent method, the sub-modeling technique is employed to recover more accurate FEA results within the lumped homogeneous die. Utilizing the obtained FEA results from the equivalent model, a new model (referred as the sub-model) containing TSV array is constructed and simulated. Fig. 6(*c*) and 6(*f*) show the temperature and warpage distributions of the sub-model, from which it can be seen that the local thermal and structural fields around TSVs are recovered through an additional sub-modeling analysis. In order to prove the advantage of the sub-modeling technique, Table 2 lists the maximum deviation of each die obtained from the sub-model method as well. Compared to the results from the equivalent model, the sub-model method offers better accuracy for both temperature and warpage. Specifically, the maximum deviation for temperature reduces from 8.23% to only 1.62%, while the maximum deviation for warpage also decreases from 7.83% to 4.89%. What's more, although the sub-modeling analysis also consumes time, the total computation time is still reduced by 76.7% compared to the detailed model.

IV. PARAMETRIC ANALYSIS AND DISCUSSION

A. IMPACTS OF TSV DIAMETER AND PITCH

In order to explore the impacts of TSV diameter and pitch on the thermo-mechanical reliability of 3D ICs with TSV array, the maximum temperature and warpage contours are plotted for different TSV diameters and pitches, as shown in Fig. 7(*a*) and 7(*b*), respectively. It can be seen that TSV diameter and pitch have opposite effects on the maximum temperature and warpage of 3D ICs. This phenomenon can be attributed to the variation of the equivalent properties when TSV diameter and pitch change. As TSV diameter increases or TSV pitch decreases, the equivalent TC of homogenized die along its vertical direction increases due to the larger volume fraction of copper material, and hence enhancing the heat transfer capability of 3D structure. As for the warpage distribution, it follows the same trend as the temperature contour, since the temperature plays a key role in determining the mechanical warpage of 3D ICs. Overall, by employing the TSVs with large diameter and small pitch, the heat transfer capability of 3D ICs can be improved and the mechanical warpage can be reduced.

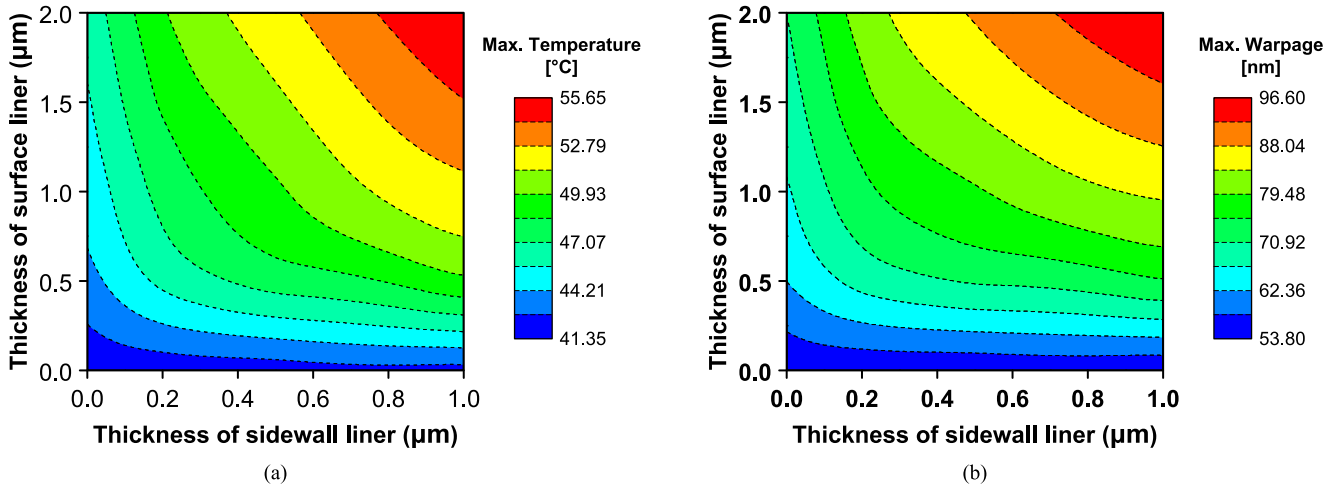


FIGURE 8. The impacts of surface and sidewall dielectric thickness on (a) the maximum temperature and (b) the maximum warpage.

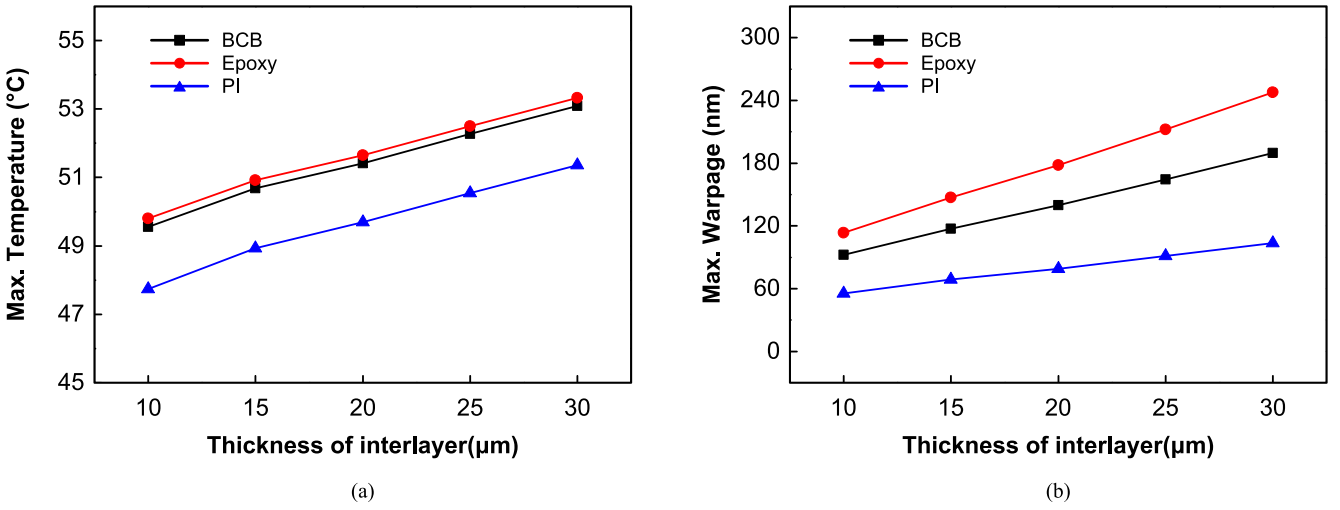


FIGURE 9. The impacts of underfill material and thickness on (a) the maximum temperature and (b) the maximum warpage.

B. IMPACTS OF SIDEWALL AND SURFACE LINER THICKNESS

Fig. 8 shows the relationship between the maximum temperature/warpage of 3D ICs and the thickness of sidewall and surface liner layers. And it can be concluded from Fig. 8 that when the thickness of sidewall or surface dielectric increases, the maximum temperature and warpage increase at the same time, which is related to the decreasing equivalent TC, since the TC of SiO_2 material is much smaller than that of silicon and copper, as shown in Table 1. With the increase of the thickness of sidewall or surface SiO_2 liner, the volume fraction of SiO_2 material increases accordingly, resulting in smaller equivalent TC. Therefore, it is desired to reduce the thickness of sidewall or surface liner for low temperature and small warpage of 3D ICs.

C. IMPACTS OF UNDERFILL MATERIAL AND THICKNESS

Furthermore, the impacts of the underfill with different materials and thicknesses on the thermal and structural fields are investigated. As shown in Fig. 9, the maximum temperature and warpage increase continuously with the increasing thickness of underfill for different materials including benzocyclobutene (BCB), polyimide (PI) and epoxy, since the polymer underfill has a low TC that makes the heat transfer between stacked dies worse. Besides, it can also be seen from Fig. 9 that 3D ICs with epoxy underfill has the highest value in terms of maximum temperature and warpage owing to its lowest TC and highest CTE. Thus, it is essential for the underfill to be with high TC and low CTE so as to reduce the heat resistance and warpage.

D. IMPACTS OF μ-BUMP MATERIAL AND DIAMETER

As the key unit of 3D structure, μ-bump can supply functions of electrical interconnect and thermal conduction among stacked chips. In this section, the dependence of maximum temperature and warpage on the diameter and material of μ-bump is further studied, as illustrated in Fig. 10. It can be seen clearly that the maximum temperature and warpage decrease for μ-bump with larger diameter as expected. It is supposed to be caused by the enhanced heat conduction path

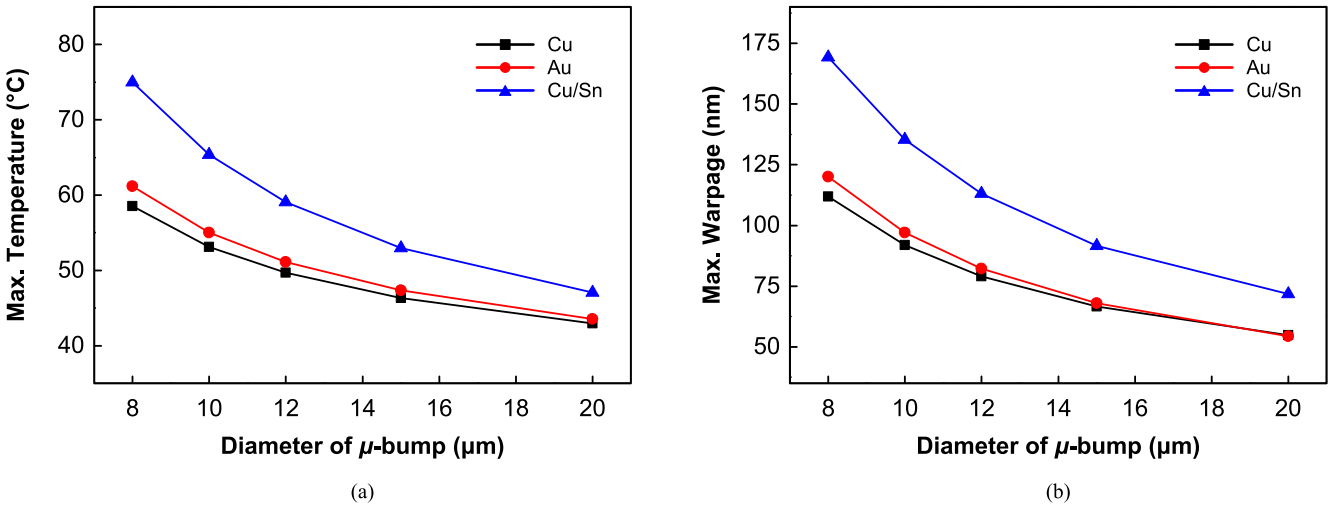


FIGURE 10. The impacts of μ-bump diameter and material on (a) the maximum temperature and (b) the maximum warpage.

between adjacent dies. Besides, 3D ICs with Cu/Sn μ-bump has the highest temperature and warpage values compared to Au or Cu μ-bump due to the poor TC and high CTE of Sn. Thus, it can be inferred from the above results that the μ-bump with large diameter, high TC and low CTE is recommended in the design of 3D products with high thermo-mechanical reliability.

V. CONCLUSION

This paper has presented a modeling and simulation strategy for implementing the coupled thermal and structural analyses of 3D ICs with TSVs. By combining the equivalent homogenization method with the advanced sub-modeling technique, the proposed method is able to reveal the detailed temperature and warpage information as true 3D FEA analysis based on the detailed model does, but the total computation time is reduced by 76.7%, thereby overcoming the inherent weakness of conventional equivalent method. The accuracy and practicability of this method are verified by comparing the simulation results of a five-layer stacked ICs using the detailed model and the sub-model, where the maximum discrepancy for temperature and warpage is only 1.62% and 4.89% respectively, proving the applicability for the coupled thermo-mechanical evaluation of 3D ICs.

In addition, the impacts of geometric dimensions of TSV array, as well as material and geometries of underfill and μ-bump on the thermo-mechanical reliability of 3D ICs are investigated. The simulation results show that the TSVs with large diameter, small pitch, thin sidewall and surface dielectrics are beneficial to the overall thermo-mechanical reliability. Furthermore, it is recommended for the underfill to be with high TC, low CTE, and small thickness and the μ-bump to be with high TC and large diameter.

REFERENCES

[1] S. J. Koester, A. M. Young, R. R. Yu, S. Purushothaman, K.-N. Chen, D. C. La Tulipe, N. Rana, L. Shi, M. R. Wordeman, and E. J. Sprogis, "Wafer-level 3D integration technology," *IBM J. Res. Develop.*, vol. 52, no. 6, pp. 583–597, Nov. 2008, doi: 10.1147/JRD.2008.5388565.

[2] J.-Q. Lu, "3-D hyperintegration and packaging technologies for micro-nano systems," *Proc. IEEE*, vol. 97, no. 1, pp. 18–30, Jan. 2009, doi: 10.1109/jproc.2008.2007458.

[3] J. H. Lau, "Overview and outlook of through-silicon via (TSV) and 3D integrations," *Microelectron. Int.*, vol. 28, no. 2, pp. 8–22, May 2011, doi: 10.1108/13565361111127304.

[4] M. Motoyoshi, "Through-silicon via (TSV)," *Proc. IEEE*, vol. 97, no. 1, pp. 43–48, Jan. 2009, doi: 10.1109/jproc.2008.2007462.

[5] Y. Deng and W. Maly, "2.5-dimensional VLSI system integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 668–677, Jun. 2005, doi: 10.1109/tvlsi.2005.848814.

[6] C. Torregiani, B. Vandevelde, H. Oprins, E. Beyne, and I. De Wolf, "Thermal analysis of hot spots in advanced 3D-stacked structures," in *Proc. 15th Int. Workshop Therm. Invest. ICs Syst. (THERMINIC)*, Leuven, Belgium, Oct. 2009, pp. 56–60.

[7] K. Puttaswamy and G. H. Loh, "Thermal herding: Microarchitecture techniques for controlling hotspots in high-performance 3D-integrated processors," in *Proc. IEEE 13th Int. Symp. High Perform. Comput. Archit.*, Scottsdale, AZ, USA, Feb. 2007, pp. 193–204.

[8] A. A. Keshavarz, P. Khare, and R. K. Sampson, "Comprehensive modeling of MOS transistors in a 0.35 μm technology for analog and digital applications," in *Proc. Int. Conf. MSM*, 2002.

[9] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*. Reading, MA, USA: Addison-Wesley, 1994.

[10] S. Das, "Design automation and analysis of three dimensional integrated circuits," Ph.D. dissertation, Massachusetts Inst. Technol., Cambridge, MA, USA, 2004.

[11] K. Tu, "Reliability challenges in 3D IC packaging technology," *Microelectron. Rel.*, vol. 51, no. 3, pp. 517–523, Mar. 2011, doi: 10.1016/j.microrel.2010.09.031.

[12] S. Kohara, K. Sueoka, A. Horibe, K. Matsumoto, F. Yamada, and Y. Orii, "Thermal stress and die-warpage analyses of 3D die stacks on organic substrates," in *Proc. 2nd IEEE CPMT Symp. Jpn.*, Dec. 2012, pp. 1–4.

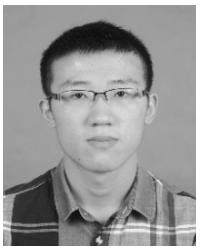
[13] C.-L. Lai, H.-Y. Li, S. Peng, T. Lu, and S. Chen, "Warpage study of large 2.5D IC chip module," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, May/Jun. 2017, pp. 1263–1268.

[14] H.-C. Cheng, T.-C. Huang, P.-W. Hwang, and W.-H. Chen, "Heat dissipation assessment of through silicon via (TSV)-based 3D IC packaging for CMOS image sensing," *Microelectron. Rel.*, vol. 59, pp. 84–94, Apr. 2016, doi: 10.1016/j.microrel.2015.12.028.

[15] K. Azar, J. R. Benson, and V. P. Manno, "Liquid crystal imaging for temperature measurement of electronic devices," in *Proc. 7th Annu. IEEE Semiconductor Therm. Meas. Manage. Symp. (SEMI-THERM)*, Feb. 1991, pp. 23–33.

[16] W.-H. Chen, H.-C. Cheng, and H.-A. Shen, "An effective methodology for thermal characterization of electronic packaging," *IEEE Trans. Compon., Packag. Technol.*, vol. 26, no. 1, pp. 222–232, Mar. 2003, doi: 10.1109/tcapt.2002.806180.

[17] C. Xue, Z. Cheng, Z. Chen, Y. Yan, Z. Cai, and Y. Ding, "Elimination of scallop-induced stress fluctuation on through-silicon-vias (TSVs) by employing polyimide liner," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 266–272, Jun. 2018, doi: 10.1109/tdmr.2018.2826557.
[18] Q. Zeng, Y. Guan, F. Su, J. Chen, and Y. Jin, "Influence of viscoelastic underfill on thermal mechanical reliability of a 3-D-TSV stack by simulation," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 2, pp. 340–348, Jun. 2017, doi: 10.1109/tdmr.2017.2682273.
[19] Z. Chen, B. Song, X. Wang, and S. Liu, "Thermo-mechanical reliability analysis of 3D stacked-die packaging with through silicon via," in *Proc. 11th Int. Conf. Electron. Packag. Technol. High Density Packag.*, Xi'an, China, Aug. 2010, pp. 102–107.
[20] F. Alfieri, S. Gianini, M. K. Tiwari, T. Brunschwiler, B. Michel, and D. Poulikakos, "Computational modeling of hot-spot identification and control in 3-D stacked chips with integrated cooling," *Numer. Heat Transf. A, Appl.*, vol. 65, no. 3, pp. 201–215, Feb. 2014, doi: 10.1080/10920277.2013.826480.
[21] J. H. Lau and T. G. Yue, "Thermal management of 3D IC integration with TSV (through silicon via)," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 635–640, doi: 10.1109/ectc.2009.5074080.
[22] J. H. Lau and T. G. Yue, "Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP)," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2660–2669, Nov. 2012, doi: 10.1016/j.microrel.2012.04.002.
[23] C. Xiao, H. He, J. Li, S. Cao, and W. Zhu, "An effective and efficient numerical method for thermal management in 3D stacked integrated circuits," *Appl. Thermal Eng.*, vol. 121, pp. 200–209, Jul. 2017, doi: 10.1016/j.applthermaleng.2017.04.080.
[24] F. X. Che, H. Y. Li, X. Zhang, S. Gao, and K. H. Teo, "Wafer level warpage modeling methodology and characterization of TSV wafers," in *Proc. IEEE 61th Electron. Compon. Technol. Conf. (ECTC)*, Lake Buena Vista, FL, USA, May/Jun. 2011, pp. 1196–1203.
[25] F. Che, H. Y. Li, X. Zhang, S. Gao, and K. H. Teo, "Development of wafer-level warpage and stress modeling methodology and its application in process optimization for TSV wafers," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 6, pp. 944–955, Jun. 2012, doi: 10.1109/tcpmt.2012.2192732.
[26] C.-C. Lee, T.-L. Tzeng, and P.-C. Huang, "Development of equivalent material properties of microbump for simulating chip stacking packaging," *Materials*, vol. 8, no. 8, pp. 5121–5137, Aug. 2015, doi: 10.3390/ma8085121.
[27] C.-C. Lee, P.-C. Huang, and B.-T. Chian, "Development and demonstration of equivalent material characteristics for microbump arrays utilized in failure estimation of chip-on-chip packaging," in *Proc. IEEE Intersociety Conf. Therm. Thermomech. Phenomena Electron. Syst. (ITherm)*, Las Vegas, NV, USA, May/Jun. 2016, pp. 262–267.
[28] Z. Hashin, "Analysis of properties of fiber composites with anisotropic constituents," *J. Appl. Mech.*, vol. 46, no. 3, pp. 543–550, Sep. 1979, doi: 10.1115/1.3424603.
[29] C. T. Sun and R. S. Vaidya, "Prediction of composite properties from a representative volume element," *Compos. Sci. Technol.*, vol. 56, no. 2, pp. 171–179, 1996, doi: 10.1016/0266-3538(95)00141-7.
[30] ANSYS. *ANSYS Mechanical APDL Advanced Analysis Guide: Sub-Modeling*. Accessed: Jan. 11, 2019. [Online]. Available: https://www.ansys.com
[31] Z. H. Karadeniz and D. Kumlutas, "A numerical study on the coefficients of thermal expansion of fiber reinforced composite materials," *Compos. Struct.*, vol. 78, no. 1, pp. 1–10, Mar. 2007, doi: 10.1016/j.compstruct.2005.11.034.
[32] R. Iannuzzelli, "Predicting plated-through-hole reliability in high temperature manufacturing processes," in *Proc. IEEE 41st Electron. Compon. Technol. Conf. (ECTC)*, Atlanta, GA, USA, May 1991, pp. 410–421.
[33] A. Jain, R. Jones, R. Chatterjee, and S. Pozder, "Analytical and numerical modeling of the thermal performance of three-dimensional integrated circuits," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 1, pp. 56–63, Mar. 2010, doi: 10.1109/tcapt.2009.2020916.
[34] X. Yin, Z. Zhu, Y. Yang, and R. Ding, "Metal proportion optimization of annular through-silicon via considering temperature and keep-out zone," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 5, no. 8, pp. 1093–1099, Aug. 2015, doi: 10.1109/tcpmt.2015.2446768.



ZHIQIANG CHENG received the B.E. degree from the Beijing Institute of Technology, Beijing, China, in 2015, where he is currently pursuing the Ph.D. degree with the School of Information and Electronics. His current research interests include advanced packaging, 3-D integration technology, and reliability evaluation of 3-D structures.

YINGTAO DING received the Ph.D. degree in mechanics from Tsinghua University. She was a Postdoctoral Research Fellow with the Institute of Microelectronics, Tsinghua University, from 2003 to 2005. She joined the Beijing Institute of Technology, in 2005. Her research interests include 3-D integration, and MEMS sensors and actuators.

ZIYUE ZHANG received the B.E. degree from the Beijing Institute of Technology, in 2015, where he is currently pursuing the Ph.D. degree with the School of Information and Electronics. His current research interests include 3-D integration technologies, MEMS, microfabrication technology, and advanced semiconductor devices.

MINGRUI ZHOU received the B.E. and M.S. degrees from the Beijing Institute of Technology, in 2016 and 2019, respectively. His current research interests include 3-D integration technologies and finite element analysis.

ZHIMING CHEN received the B.Eng. degree from Tsinghua University, and the Ph.D. degree from the University of California at Irvine, Irvine. In 2012, he joined the Beijing Institute of Technology, where he is currently an Associate Professor. His research interests include advanced packaging, 3-D integration technology, and RF/MMW system design.