IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received December 19, 2019, accepted January 9, 2020, date of publication January 14, 2020, date of current version January 27, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2966664

Simultaneous Wireless Power and Data Transmission Based on Unsymmetrical Current Waveforms With Duty Cycle Modulation

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This work was supported in part by the National Natural Science Foundation of China under Grant 51777098, in part by the Natural Science Foundation of Jiangsu Province under Grant BK20191383, and in part by the Jiangsu Province Graduate Research and Practice Innovation Plan under Grant SJCX19_0261.

ABSTRACT This paper proposes an active-clamped inverter (ACI) with duty cycle modulation for achieving simultaneous wireless power and data transmission (WPDT). The proposed method adjusts harmonic amplitudes by changing the duty cycle of the inverter, as a means to encode information alongside power using a shared wireless channel. This method generates a variable unsymmetrical current waveform corresponding with different duty cycles. By controlling the duty cycle, simultaneous power and data transfer can be achieved by using the fundamental and harmonic components respectively. The ACI is designed to operate in continuous current mode to reduce the variation of harmonic components, even under no load conditions. A simple ACI containing two switches is proposed to generate unsymmetrical current waveforms with a high efficiency and high circuit quality factor Q. Two communication methods are developed to balance the power transfer capability and signal-noise-ratio (SNR). Various separation distances and loads are tested, with experimental results showing the proposed system can achieve simultaneous power and data transfer across a shared channel in an inductive wireless power transfer.

INDEX TERMS Pulse width modulation inverters, inductive power transmission, data transfer.

I. INTRODUCTION

Wireless power and data transfer technologies are used in many special applications. For example, some medical implants, such as pacemakers and cochlear implants [1], [2], need to transfer power and data simultaneously. Since these electronic devices are desired to be as small as possible, the circuits used for these applications should be simple and cheap [3]–[9].

There are many methods to achieve simultaneous wireless power and data transmission (WPDT). One of the most popular solutions uses an independent RF chip to transfer data alongside a standalone WPT system. However, communication modules need to undergo an IP address matching process, which brings increased inconvenience. Building an additional pair of coils to transfer signals separately to power is another option, with the drawback of significantly increasing system size and cost. Furthermore, the interferences between separated power coils and signal coils are difficult to control [10]–[14]. Power transfer inverters using ON-OFF keying data modulation have been used for several years but suffer from greatly reduced power transfer efficiencies [15]–[21]. Based on a symmetrical waveform, novel WPDT methods using fundamental components to transfer power, and harmonics to transmit data have been previously proposed [22], [23]. Using harmonic components to transmit data can avoid to build the additional circuits of signal sources.

Equation (1) shows the maximum efficiencies of WPT system highly depend on the product of the magnetic coupling k and the Q [24]–[26].

$$\eta_{\max} \approx 1 - \frac{2}{k\sqrt{Q_T Q_R}} \tag{1}$$

The associate editor coordinating the review of this manuscript and approving it for publication was Yulong Zou.

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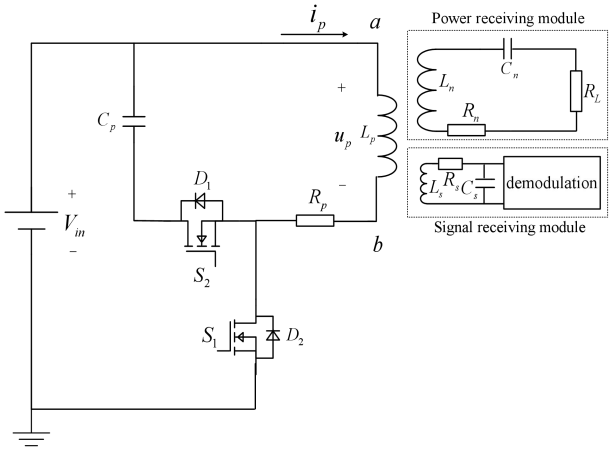

FIGURE 1. The proposed ACI system.

where Q_T and Q_R are the quality factors for the transmitter coil and receiver coil respectively. For the transmitter coil, $Q_T = wL_p/R_p$ and $R_p = R_{coil} + R_{switch}$. R_{coil} is the resistance of the coil, and R_{switch} is the equivalent resistance including the effects of on-resistances of switches and switching losses. A full-bridge converter can produce a symmetrical waveform to achieve WPDT, but it contains four switches. Less switches will reduce R_{switch} and enhance Q_T obviously, so the transmitting efficiency can be improved. A half-bridge converter contains two switches, but only half of the input voltage is added on the transmitter coil. A single-ended converter can use the input voltage fully with two switches, but the single-ended converter produces an unsymmetrical rectangular voltage waveform normally. The behaviors of the unsymmetrical waveform under different duty cycles have not been researched.

This paper proposes a single-ended active-clamped inverter (ACI) to produce an unsymmetrical waveform to achieve simultaneous wireless power and data transmission. In Section II, the characteristics of ACIs for achieving WPDT are discussed. The changing behavior of the waveforms fundamental component and harmonics with different duty cycles is analyzed in Section III. In Section IV, the hardware circuits of the communication block are introduced. The experimental results are shown in Section V, with the conclusions drawn in Section VI.

II. THE PROPOSED WPDT SYSTEM

A. STRUCTURE AND WORKING PRINCIPLES OF THE ACI

As shown in Fig. 1, the transmitting circuits consists of the ACI. Various unsymmetrical triangular current waveforms can be formed in L_p, corresponding to different duty cycles. The power and signal receiving circuits are made using individual LC resonant circuits which have different self-resonant frequencies (SRF). The fundamental frequency of the triangular current waveform equals the SRF of L_n and C_n in the power receiving circuit. The selected harmonic frequency equals the SRF of L_s and C_s in the signal receiving circuit. R_p, R_n and R_s are total equivalent resistances for the three circuits respectively.

The power transmitter coil L_p and power receiver coil L_n have the same planar structure. The signal receiver coil L_s uses a ferrite rod core to enhance the quality factor of circuits. The coupling coefficient M_{pn} between L_p and L_n or M_{ps} between L_p and L_s should keep high at the same time. A high M_{pn} can achieve a high power transfer efficiency, and a high M_{ps} can ensure a good communication quality. The coupling coefficient M_{ns} between L_n and L_s should be minimized to avoid the effect of interference signal from L_n on L_s. The geometry and positioning of the three coils coincide with [22].

A switching period is divided into two stages mainly based on the proposed ACI.

Stage 1[$t_0 \sim t_1$]: S_1 turns on and S_2 turns off at t_0. The current i_p passes through the V_{in}, L_p, R_p, S_1, as shown in Fig 2 (a). During this period, up equals V_{in} and i_p increases linearly until S_1 turns off at t_1.

Stage 2[$t_1 \sim t_2$]: S_2 turns on and S_1 turns off at t_1. The current passes through the L_p, R_p, S_2, C_p, as shown in Fig 2 (b). The clamp voltage V_c on C_p offers a reset voltage for L_p, the value of which will be explained later in the paper. During this period, u_p equals V_c and i_p decreases linearly until S_2 turns off at t_2. Actually, achieves ZVS easily if the dead time is set well.

Fig. 3 shows the key waveforms of the ACI. In order to simplify the analysis, the effects of dead time will be neglected. S_1 and S_2 conduct alternately in a switching period, D is the duty cycle of S_1, i_p is the triangular current flowing through L_p, u_p is the voltage on L_p, V_p is the input voltage, and V_c is the voltage on C_p.

A magnetizing inductor current i_p flows through C_p during Stage 2, and the electric charges $Q^+_{C_p}$ and $Q^-_{C_p}$ of C_p are balanced around zero. Since the clamped capacitor C_p has a relatively large value, V_c across C_p can be approximated as a constant value. According to the voltage-second balance law, V_{in} and V_c meet the relationship of (2) when the system works under a stable state condition.

$$V_{in}DT = V_c(1-D)T \Rightarrow V_c = \frac{D}{1-D}V_{in} \tag{2}$$

Unlike the symmetric waveforms in [22], [23], the ACI produces an unsymmetrical waveform during a switching period. u_p in Fig. 3 can be expressed in FFT form, with the calculating process is given in the Appendix

$$u_p(t) = \frac{2V_{in}}{(1-D)\pi}\sum_{k=1}^{+\infty}\frac{\sin kD\pi}{k}\cos k\omega t \tag{3}$$

where k is a positive integer, $\omega = 2\pi f$ and f is the switching frequency.

Based on (3), the harmonics of the peak voltage under different duty cycles $U_{pk}(D)$ are defined as

$$U_{pk}(D) = \frac{2V_{in}}{k(1-D)\pi}\sin kD\pi \tag{4}$$

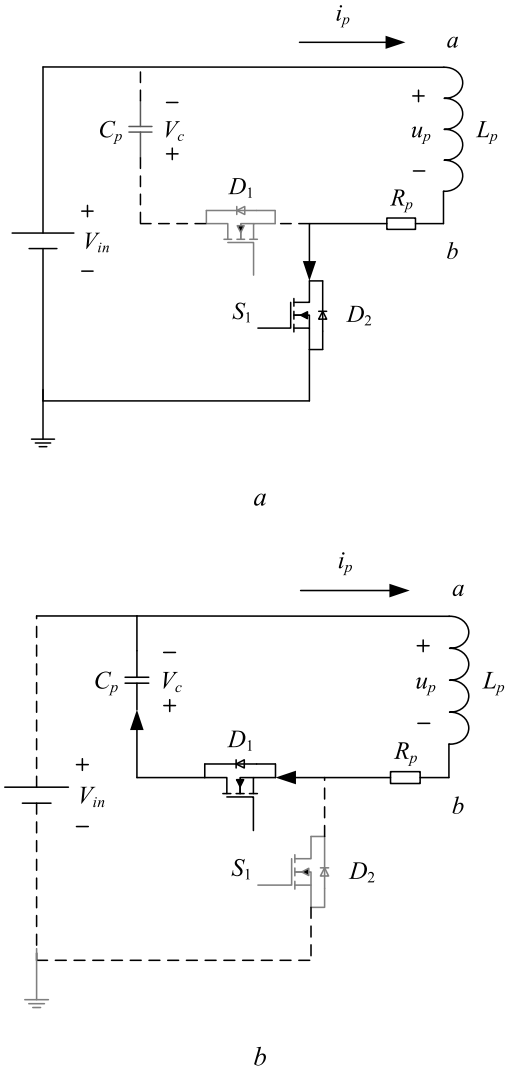

FIGURE 2. Stages of the ACI circuits in a switching period.

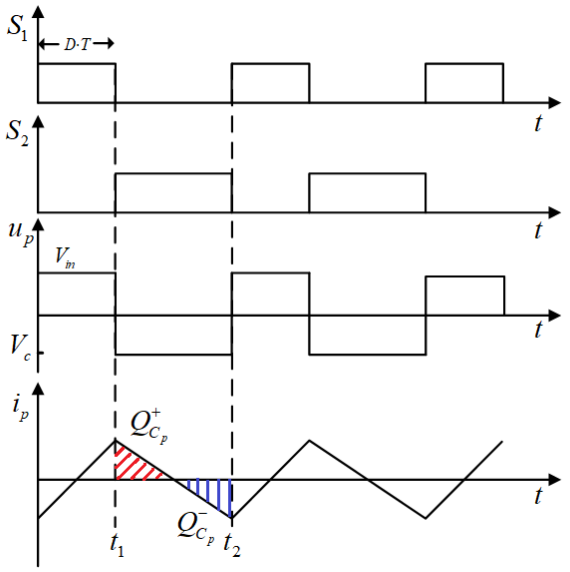

FIGURE 3. Key waveforms of the ACI.

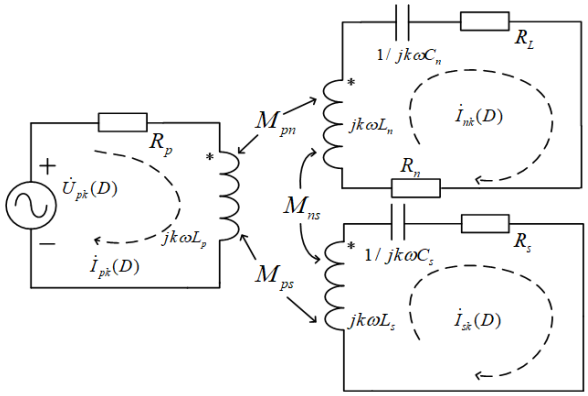

FIGURE 4. Equivalent circuits under the $I_{pk}(D)$ excitations.

The FFT forms of the triangular current i_p in Fig. 3 are

$$i_p(t) = \frac{2V_{in}}{L(1-D)\omega\pi} \sum_{k=1}^{+\infty} \frac{\sin kD\pi}{k^2} \sin k\omega t \tag{5}$$

Based on (5), the harmonics of peak current at different duty cycles $I_{pk}(D)$ can be expressed as

$$I_{pk}(D) = \frac{2V_{in}}{k^2L(1-D)\omega\pi} \sin kD\pi \tag{6}$$

Since the discontinuous current mode for an ACI does not exist, the values of the harmonics in (6) remain constant even under no load conditions.

B. EQUIVALENT CIRCUITS OF THE PROPOSED SYSTEM

As shown in Fig. 4, the excitations of $I_{\mathrm{pk}}(D)$ at different duty cycles, generate the induced currents $I_{\mathrm{nk}}(D)$ and $I_{\mathrm{sk}}(D)$ in the power coil and signal coil respectively.

The state space equation of the ACI is

$$\begin{bmatrix} \dot{U}_{pk}(D) \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{pk} & -jk\omega M_{pn} & -jk\omega M_{ps} \\ -jk\omega M_{pn} & Z_{nk} & jk\omega M_{ns} \\ -jk\omega M_{ps} & jk\omega M_{ns} & Z_{sk} \end{bmatrix} \times \begin{bmatrix} \dot{I}_{pk}(D) \\ \dot{I}_{nk}(D) \\ \dot{I}_{sk}(D) \end{bmatrix} \tag{7}$$

where Z_{pk}, Z_{nk} and Z_{sk} are the equivalent impedances.

$$\begin{cases} Z_{pk} = R_p + jk\omega L_p \\ Z_{nk} = R_L + R_n + jk\omega L_n + 1/jk\omega C_n \\ Z_{sk} = R_s + jk\omega L_s + 1/jk\omega C_s \end{cases} \tag{8}$$

For the sake of simplicity, the impact of harmonics on the fundamental component will be neglected in here. According

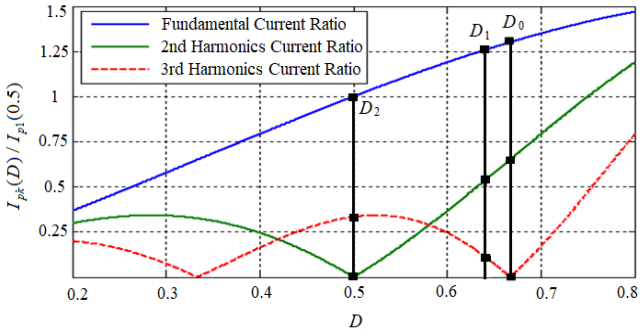

FIGURE 5. Changed trends of $I_{pk}(D)/I_{p1}(0.5)$ under different duty cycles.

to (4), (6) and (7), $I_{p1}(D)$ and $I_{n1}(D)$ can be expressed as

$$\dot{I}_{p1}(D) = \frac{\dot{U}_{p1}(D)}{j\omega L_p + R_p + \frac{\omega^2 M_{pn}^2}{j\omega L_n + 1/j\omega C_n + R_L + R_n}} \tag{9}$$

$$\dot{I}_{n1}(D) = \frac{j\omega M_{pn}\,\dot{I}_{p1}(D)}{j\omega L_n + 1/j\omega C_n + R_L + R_n} \tag{10}$$

When the power receiving circuit works under resonant conditions, the efficiency of the proposed system can be simplified as

$$\eta(\omega_0) = \frac{R_L(\omega_0 M_{pn})^2}{(R_L + R_n)[R_p(R_L + R_n) + (\omega_0 M_{pn})^2]} \tag{11}$$

III. WIRELESS DATA TRANSFER BASED ON UNSYMMETRICAL OPERATION OF ACI

A. RELATIONSHIP BETWEEN HARMONIC COMPONENTS AND DUTY CYCLE

Compared to symmetrical waveforms, the asymmetric current waveform contains the harmonics of odd components and even components at the same time. As can be seen in (6), D plays an important role and influences the values of the fundamental and harmonic components. Therefore, it is important to first analyse the effect of changing duty cycle for each harmonic.

As shown in Fig. 5, the current fundamental component $I_{\mathrm{p1}}(0.5)$ is taken as a reference. The blue line is the changes in $I_{\mathrm{p1}}(D)$ versus different duty cycles. This curve shows that the proposed system with a higher D can improve the capability of WPT for increasing values of I_{p1}. The green line and the red line show the changes in the 2nd harmonic $I_{\mathrm{p2}}(D)$ and the 3rd harmonic $I_{\mathrm{p3}}(D)$ respectively for different duty cycles. Obviously, adjusting the duty cycle can be used as a strategy to modulate the values of harmonics for transferring data signals.

Since the interval frequencies between the fundamental component and 2nd harmonic is relatively narrow, using other higher order harmonics can reduce noise interferences caused by the strong fundamental component.

TABLE 1. Theoretical results of harmonics under typical duty cycles.

Harmonic Ratio (%)	D_0=0.66	D_1=0.624	D_2=0.5
$I_{p1}(D)/I_{p1}(0.66)$	1	95%	75%
$I_{p2}(D)/I_{p2}(0.66)$	1	75%	0%
$I_{p3}(D)/I_{p3}(0.66)$	1	500%	1000%

Taking the 3rd harmonic as an example, it is shown that the 3rd harmonic can effectively be suppressed when $D_0 = 0.33$ or $D_0 = 0.66$. The value of I_{p1} decreases dramatically when $D_0 = 0.33$. Under $D_0 = 0.66$, a higher power transfer operation of the WPT system can occur when the communication function is not required or is transmitting a '0' data bit. Fig. 5 shows that duty cycles between 0.5 and 0.67 can be selected to represent the opposite data bit '1'.

B. TRADE-OFF BETWEEN CAPABILITIES OF WIRELESS POWER TRANSFER AND HIGH SNR OF COMMUNICATION

As mentioned earlier, the values of the fundamental component decrease dramatically when duty cycles are low. Depending on the priorities of different applications, two communication modes are proposed for determining duty cycles to best meet the specific requirements.

Mode I (between D_0 and D_1): At the point of $D_1 = 0.624$ in this setup, the 3rd harmonic can achieve a stable envelope curve in the communication circuit. This mode can be used for achieving a good balance between the power transfer and communications functionality of a WPT system.

Mode II (between D_0 and D_2): At the point of $D_2 = 0.5$, the 2nd harmonic is eliminated totally and the 3rd harmonic reaches an approximately maximum value. This mode suits applications which require a high signal-to-noise ratio (SNR) for communications.

In order to investigate the capabilities of the proposed system, the induced voltages on the power receiving coil are tested at different duty cycles and separation distances. The induced voltage at the power receiving coil with a duty cycle $D_0 = 0.66$ is taken as the reference. Based on (6), Fig. 6 shows that the predicted values and experimental results at three typical duty cycles fit very well under different separation distances. These experiments show that duty cycles will affect the capabilities of the wireless power transfer significantly, agreeing with Fig. 5. The induced receiver voltage decreases by nearly 25% when $D_2 = 0.5$, and only shows a 5% decrease at $D_1 = 0.624$.

In order to investigate the characteristics of harmonic frequencies and values at the typical duty cycles, frequency domain analysis for current waveforms in the transmitter coil is performed and experimentally verified. Table 1 shows the ideal theoretical results based on (6), but in practical

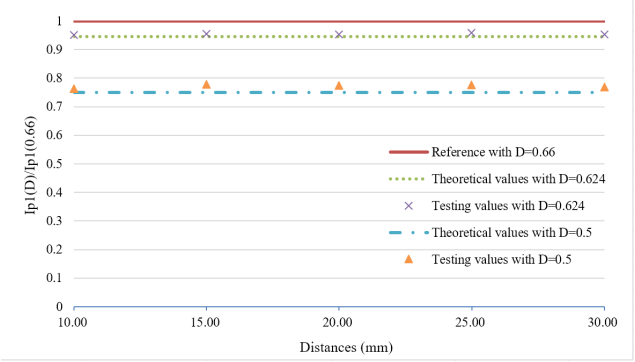

FIGURE 6. Induced voltages on the power receiving coil at typical duty cycles under different distances.

engineering harmonic ratio is limited by the controlled accuracy of duty cycles and lower than the expected values.

The MDO3024 oscilloscope has a spectral analysis function, and harmonics of current waveforms can be demonstrated in a straightforward way. As shown in Fig. 7, the frequencies of harmonics will not be affected when duty cycles are adjusted for data modulation. Compared with Fig. 7 (a) and Fig. 7 (b), it is shown that the value of the 3rd harmonic at state D_1 is 10dB higher than at state D_0. This follows the conclusions of (7) very well. Since I_{p1} only decreases by 5% at state D_1, this mode is suitable when good balance between data transfer and capability is required in a WPT system.

If the WPDT system requires a high SNR in the communications, Mode II can be used to transmit bit '1'. As shown in Fig. 7 (c), the values of the 3rd harmonic rise by 20dB from state D_0. Since the values of the 2nd harmonics fall by 50dB at this point, a high SNR for communications is achieved easily. However, the capability of WPT is limited at this point since I_{p1} also decreases remarkably.

C. DESIGN OF MODULATION AND DEMODULATION CIRCUITS

Fig. 8 (a) shows the block diagram of the major components for the hardware setup, and the diagram of the modem circuits is shown in Fig. 8 (b). D_0 is selected as the default duty cycle value. According to the requirements of the system function, different modes can be selected corresponding to different duty cycles. The signal receiving circuits extract the induced voltage envelope waveforms of the 3rd harmonic and give the judgments of the baseband signal.

The demodulation circuits are shown in Fig. 9. The voltage-follower and amplifier enlarge the differences of induced voltages between bit '0'and bit '1'. High frequency noise on the envelopes of 3rd harmonic can be removed by a low-pass RC filter. Finally, the comparator and transistor recover the baseband signal.

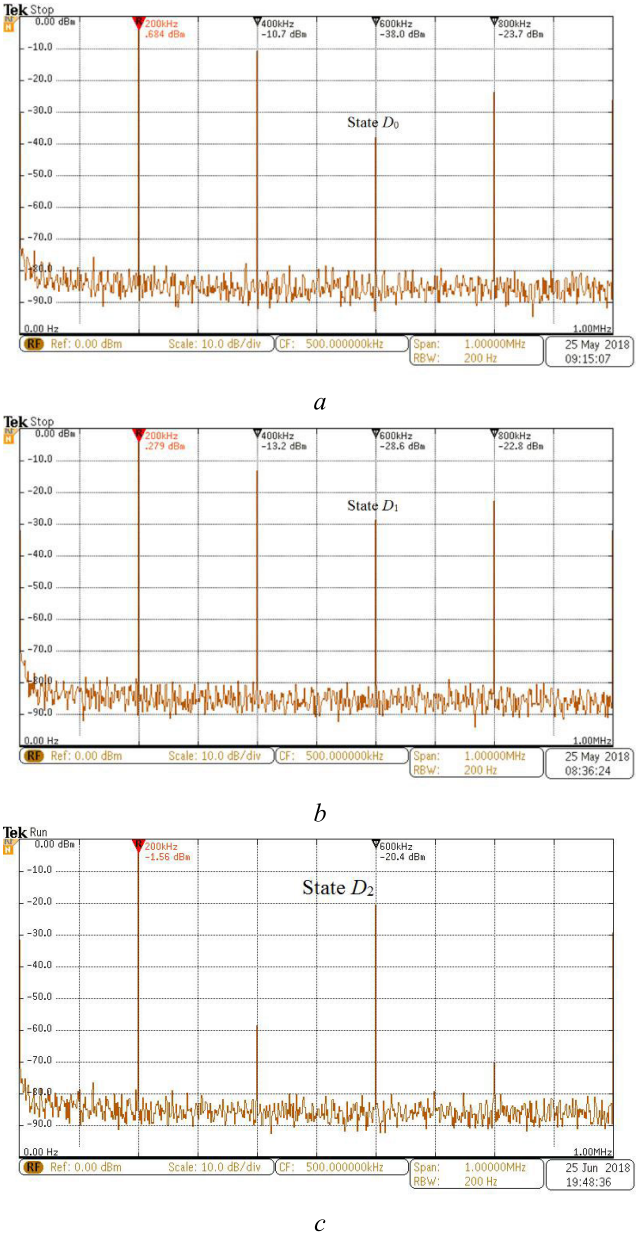

FIGURE 7. Experimental results of harmonic components $aD_0 = 0.66, bD_1 = 0.624, cD_2 = 0.5$.

IV. EXPERIMENTAL RESULTS

In order to verify the different characteristics at various duty cycles, a test platform is constructed, as shown in Fig. 10. The key parameters of the proposed WPDT system are listed in Table 2.

The key waveforms of the circuits at D_0 are shown in Fig. 11. Starting with the top trace, the traces are the U_{ab} voltage waveform, the i_p current waveform and the induced voltage waveforms at the power receiving coil and signal receiving coil respectively. Fig. 11 (a) shows the key waveforms with no load, and Fig. 11 (b) shows the waveforms when $R_L = 2.5\Omega$. Obviously, the current waveforms in

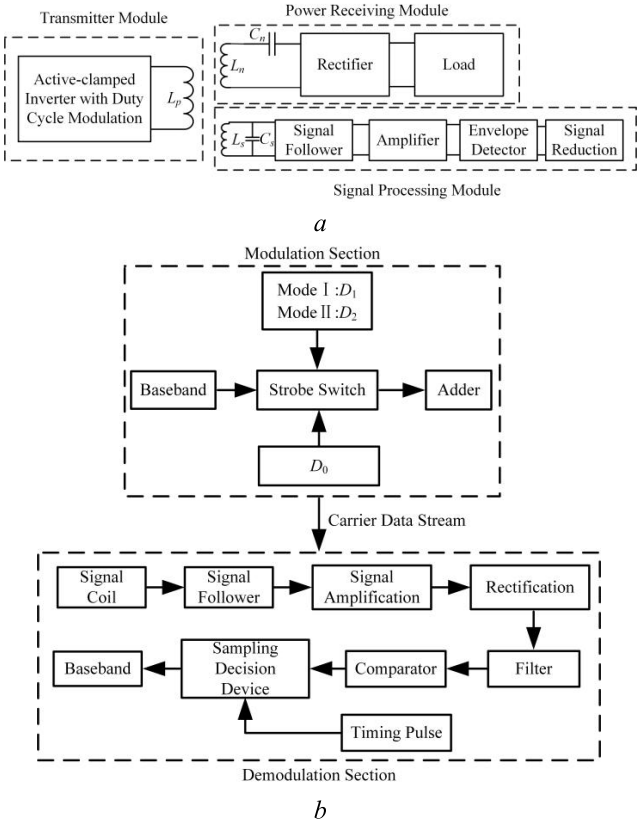

FIGURE 8. Diagram of the modem circuit.

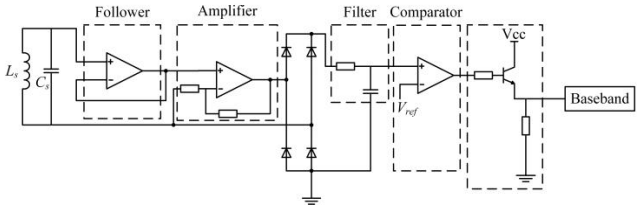

FIGURE 9. The demodulation circuits.

TABLE 2. Key parameters of the circuit.

Power Transmitting Module	$V_{in}=24V$, $L_p=11.78\mu H$, $R_p=0.3\Omega$, $r_1=44mm$, $r_2=60mm$, $N=8$ FPGA: EP4CE6E22C8N, MosFET: PSMN013
Power Receiving Module	$C_n=55nF$, $L_n=11.78\mu H$, $r_1=44mm$, $r_2=60mm$, $N=8$, $R_L=2.5\Omega$, $R_n=0.43\Omega$
Signal Receiving Module	$C_s=1.08nF$, $L_s=66\mu H$, $R_s=12.4\Omega$ *and* $Q=20$ @$600kHz$, $N=47$, Wire diameter=0.5mm, Rod Core (ROD6/30-3B1), MCU: STC12C5201D
Testing Equipment	Oscilloscope: MDO3024, Power Analyzer: YOKO WT1800, Current probe: TEK-P6021, Differential voltage probe: TEK-P5205A

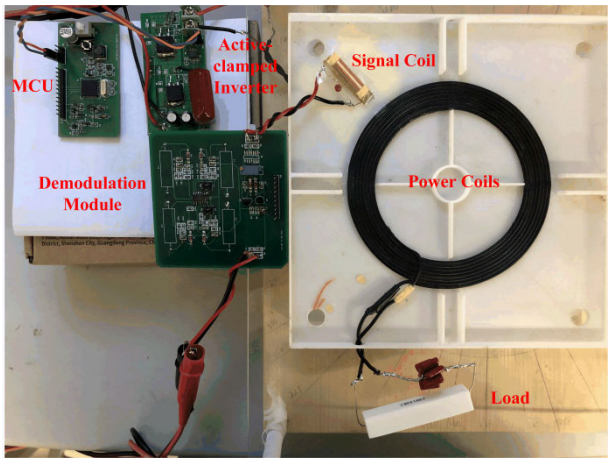

FIGURE 10. The test platform.

the primary side show different shapes under various load conditions. The most interesting observation is that the waveforms of the 3rd harmonic will not change, since the reflected currents caused by a changing load will only affect the fundamental component.

As mentioned before, two modes can be used to achieve the proposed WPDT functionality. $D_1 = 0.624$ is selected as a modulation point to achieve the maximum power transfer capability of the WPT system, and $D_2 = 0.5$ can be used to meet a requirement for high SNR in the communications. In order to simplify the analysis, the testing experiments are modulated with a typical '0101' digital message signal.

Fig. 12(a) and Fig. 12(b) show the characteristics of the system under Modes I and II with $R_L = 2.5\Omega$ respectively. The upper traces are the extracted signal waveform and the lower trace is the induced voltage waveform on power receiving coil. Fig. 12(a) shows that the induced voltage waveforms in the power receiving coil remain constant when data is transferred, meaning the power transfer capability of the system will not be affected by communications. On the contrary, the data transfer process shows a significant reduction in the induced voltage waveforms for the power receiving coil under Mode II operation. Therefore, the power transfer ability of the WPDT system will be limited in Mode II. However, a higher SNR in Fig. 12 (b) is achieved compared with the theoretical analysis shown in Fig. 12 (a).

Fig. 13 shows the curves for system efficiency under the two modes respectively. We use 2.5-ohm resistor as loads and can achieve 30W level power transfer at a 10mm air gap. Based on the proposed method, the signal can be transmitted by using the same coil of the power transfer. So the system can achieve WPDT without using any

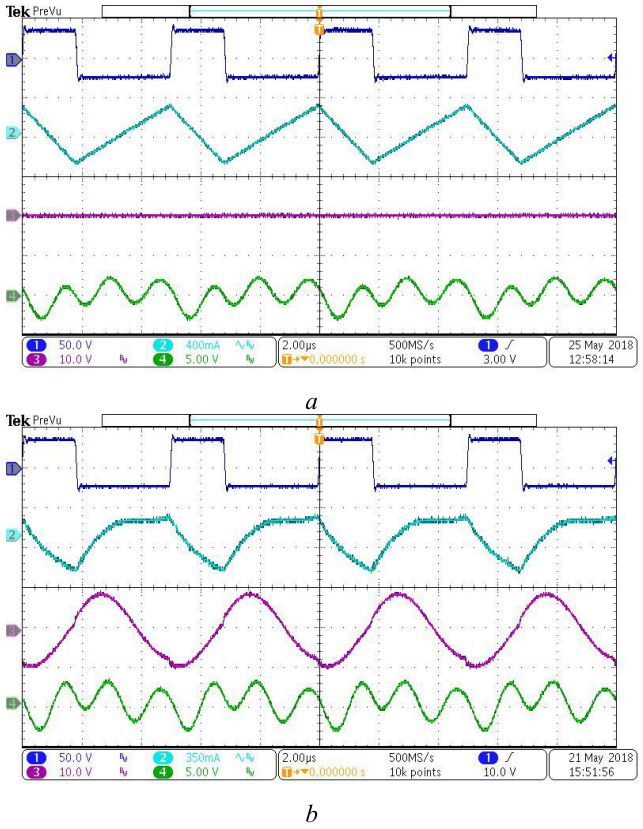

FIGURE 11. Induced voltage waveforms in signal coil are insensitive to load conditions *a* No load, *b* $R_L = 2.5\Omega$.

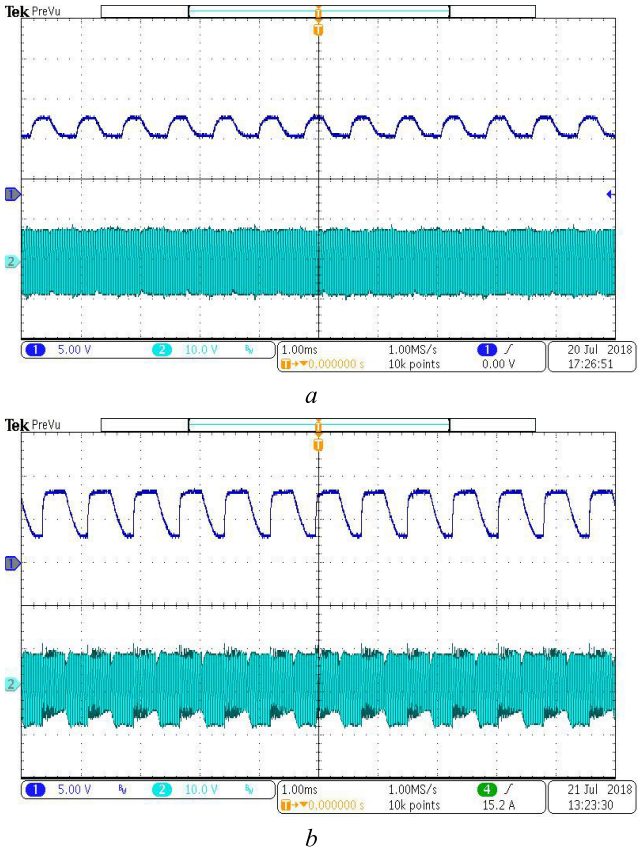

FIGURE 12. Induced voltage waveforms on the power receiving coil and the envelope curve on the signal receiving coil under two different Modes *a* Mode I, *b* Mode II.

extra data transmission devices. When the distance between power coils is 30mm, the transmitted powers are 16.62W, 15.79W and 11.946W and the received powers are 14.05W, 13.34W and 10.5W when the system works under $D = 0.66$, Mode I and Mode II respectively. The capability of the power transfer is limited under Mode II as expected since I_{p1} decreases dramatically from D_0 to D_1 as shown in Fig. 5. Fig. 13 gives an intuitive impression that the proposed method can achieve a quasi-decoupling relationship between communication and efficiency.

Similar efficiencies in both of these modes is unsurprising since the efficiency is defined by (11). Benefitting from a single-ended converter design with higher Q coil values and ZVS conditions in S_2, the ACI shows an efficiency improvement of nearly 7% compared with full-bridge converters operating under the same conditions [22], [23].

Taking the received power $P_{rec}(D)$ with $D = 0.66$ as a reference, Fig. 14 shows the ratio curves of the received power under Mode I and Mode II. Consistent with the previous analysis in (9) and Fig. 6, the capabilities of the WPT obviously decrease since the fundamental current I_{p1} goes down in Mode II.

Fig. 15 shows that the input baseband signal, shown as the upper trace can be accurately identified, and the demodulation baseband signal, shown as the lower trace, can be recovered in both in Mode I and Mode II.

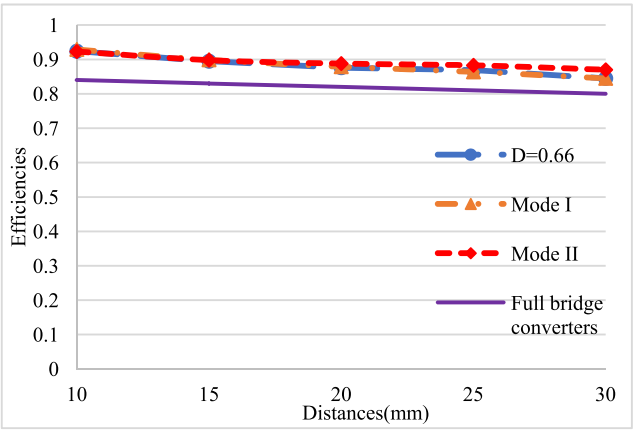

FIGURE 13. Curves of efficiencies in the ACI under two modes.

Table 3 shows the comparison results between the proposed method and typical published literature. We use three levels to compare their performances from different aspects, such as data transmitting speed, the effect of data transmission on power transfer and the complexity of circuits, and "H, M and L" are the abbreviation for "High, Middle and Low". We can observe that the proposed method shows a good balance among typical performances in table 3.

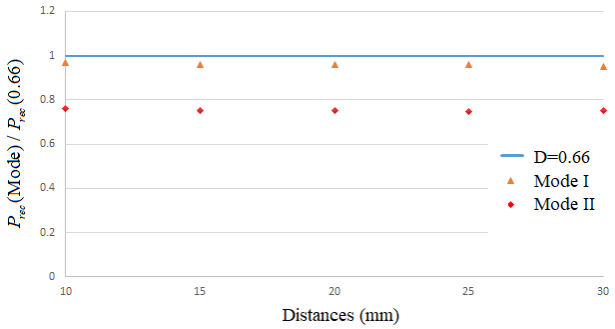

FIGURE 14. Ratio curves of received powers under two modes.

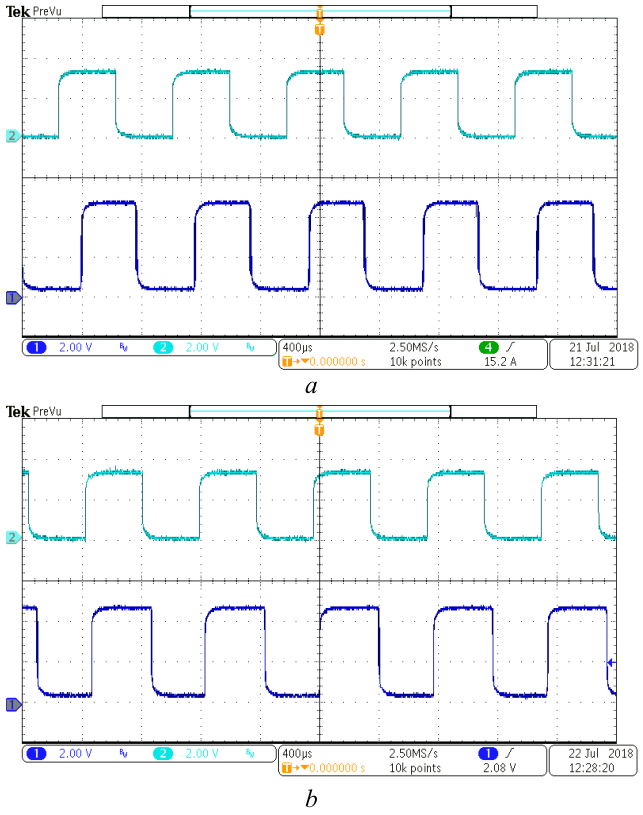

FIGURE 15. Baseband signals and output signals under two different communication modes *a* Mode I, *b* Mode II.

TABLE 3. The performances of typical solutions.

Ref.	Speed	Effect on Efficiency	Circuit Complexity
[5]	H	-	H
[7]	H	M	M
[15]	L	H	L
RF chips	H	-	H
This paper	M	L	L

V. CONCLUSION

A wireless power and data transmission system based on the modulation of duty cycles is proposed and developed in this paper. In order to enhance the system efficiency by improving the parameter Q, a single-ended active-clamped inverter containing two switches is used. Compared with the traditional full-bridge converter configuration, the efficiency in the proposed system is improved by nearly 7%. The proposed method uses unsymmetrical current waveforms with duty cycle control, and a good balance has been achieved between system power efficiency, cost and complexity.

Benefitting from using duty cycle modulation, the effect of communications on the system power efficiency is relatively small. Furthermore, the transmitter coil is designed to operate in the continuous current mode to reduce the variation of harmonic components, even under no load conditions.

Duty cycles are modulated to achieve the communication functionality, and two modes offer the capability of prioritizing power transfer or high communications SNR. The behaviour of system has been verified by simulation and experimental results, and the constructed prototype has shown the feasibility of the proposed WPDT system.

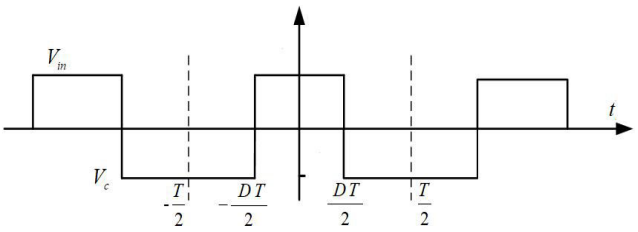

FIGURE 16. The waveform of the $u_p(t)$.

APPENDIX

In this Appendix, the calculation process shows the fast Fourier transforms (FFT) of $u_p(t)$ and $i_p(t)$ in the proposed system.

From Fig. 16, $u_p(t)$ in a switching period is:

$$u_p(t)=\begin{cases} V_{in} & \text{if } -\dfrac{DT}{2}\le t\le\dfrac{DT}{2} \\ -\dfrac{DV_{in}}{1-D} & \text{if } \dfrac{T}{2}\le t<-\dfrac{DT}{2} \text{ or } \dfrac{DT}{2}<t\le\dfrac{T}{2} \end{cases} \tag{a.1}$$

According to FFT, $u_p(t)$ can be expressed as:

$$u_p(t)=a_0+\sum_{k=1}^{+\infty}(a_k\cos k\omega t+b_k\sin k\omega t) \tag{a.2}$$

Since $u_p(t)$ can be treated as an even function and does not contain a DC bias, a_0, b_k can be easily gotten as:

$$a_0=0 \tag{a.3}$$

$$b_k=0 \tag{a.4}$$

Based on (1), the cosine terms a_k is:

$$a_k=\frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}}f(t)\cdot\cos k\omega t\cdot dt=\frac{4}{T}\int_0^{\frac{T}{2}}f(t)\cdot\cos k\omega t\cdot dt$$

$$=\frac{4}{T}\int_0^{\frac{DT}{2}}V_{in}\cos k\omega t dt+\frac{4}{T}\int_{\frac{DT}{2}}^{\frac{T}{2}}\frac{D}{D-1}V_{in}\cos k\omega t dt$$

$$= \frac{4V_{in}}{Tn\omega}\sin k\omega t\Big|_{0}^{\frac{DT}{2}} + \frac{4V_{in}}{Tn\omega}\frac{D}{D-1}\sin k\omega t\Big|_{\frac{DT}{2}}^{\frac{T}{2}}$$

$$= \frac{2V_{in}}{n\pi(1-D)}\sin kD\pi \tag{a.5}$$

So $u_p(t)$ can be summarized mathematically as follows:

$$u_p(t) = \frac{2V_{in}}{(1-D)\pi}\sum_{k=1}^{+\infty}\frac{\sin kD\pi}{k}\cos k\omega t \tag{a.6}$$

The relationships between $u_p(t)$ and $i_p(t)$ are:

$$u_p(t) = L\frac{di_p(t)}{dt} \tag{a.7}$$

Based on (a.6) and (a.7), the $i_p(t)$ can be written as:

$$i_p(t) = \frac{2V_{in}}{L(1-D)\omega\pi}\sum_{k=1}^{+\infty}\frac{\sin kD\pi}{k^2}\sin k\omega t \tag{a.8}$$

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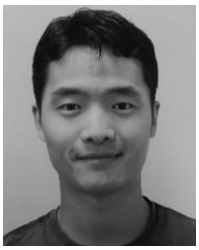

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