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Alteration of Gate-Oxide Trap Capture/Emission Time Constants by Channel Hot-Carrier Effect in the Metal-Oxide-Semiconductor Field-Effect Transistor

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ABSTRACT Electrical-stress-invariant gate-oxide traps' capture and emission time constants have been the basis of aging models as well as applications that leverage the stochastic nature of the capture and emission processes, such as the true random number generator. In this work, we show that this presumption is only valid for about two-thirds of the oxide-trap population studied. For the remaining one-third, the traps' capture and/or emission time constants could be changed by the channel hot-carrier (CHC) effect. Such a behavior is found in both polysilicon/silicon oxynitride gated and TiN/HfO_2 gated transistors. A reversion of the altered trap time constant to the value before the CHC-stress is also observed, but the period varies significantly for different traps (from several hours to months). Since the CHC stress effect is present in all scaled transistors, the findings would have important implications for models/applications that presume oxide-trap properties to be stress-invariant.

INDEX TERMS Gate dielectric defects, random telegraphic noise, channel hot carriers.

I. INTRODUCTION

Electronic traps in the gate oxide of the metal-oxide-semiconductor (MOS) field-effect transistor are known to have a profound influence on the transistor operation and they have been studied as a reliability issue, as well as a possible avenue for novel applications by exploiting the randomness of charge trapping and detrapping. Random telegraphic drain-current (I_d) noise [1]–[3] and threshold-voltage (V_t) instability [4]–[9] that arise from charge capture/emission by oxide traps have been intensively studied due to their potential impact on timing-sensitive circuits, e.g. causing timing jitter in the static random-access memory [10]–[12]. Some studies have leveraged the stochastic nature of the capture/emission processes for realizing physically unclonable functions, such as a true random number generator (TRNG) [13]–[15], a key primitive for future data and communication secured applications in the internet of things era. Others have explored the possibility of using a charge-trap memory transistor as an artificial synapse [16]–[20] that emulates the plasticity behavior of biological synapses in response to neuron spikes, due to the capability of continuously modulating the population of filled traps and hence the channel conductance of the MOS structure.

Parametric variations due to charge capture and emission by oxide traps are usually expressed in terms of probability functions characterized by the traps' capture and emission time constants (τ_c and τ_e, respectively). Although τ_c and τ_e are dependent on temperature and applied voltage, the general presumption is that these parameters are invariant under a given operating condition. Invariant and stabilized trap properties are crucial to the validity of physically unclonable functions (PUFs), endurance of artificial synapses and the accuracy of predictive aging models. In this work, we found that this presumption is valid for less than two-third of the oxide traps studied. For about 40% of the traps, their τ_c and τ_e may be changed persistently after subjecting the transistor to a brief channel hot-carrier (CHC) stress, a ubiquitous effect that arises from drain voltage (V_d) induced carrier heating in scaled transistors. A plausible physical explanation for the observed changes is provided.

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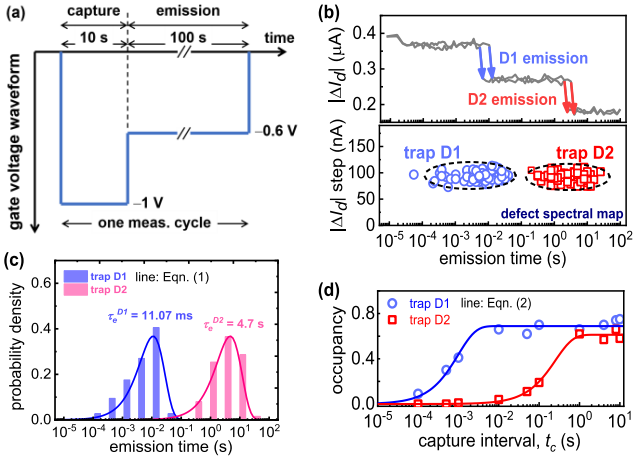

FIGURE 1. (a) Gate voltage waveform within one measurement cycle, applied during the testing of a p-channel transistor. Drain voltage was fixed at −0.1 V. Statistics on the capture and emission characteristics of oxide traps can be collected by repeating the gate-voltage cycles. (b) Recovery of degraded drain current ($|\Delta I_d|$) due to discharging of pre-charged oxide traps during the emission interval (upper). Plot of $|\Delta I_d|$ recovery step versus emission time yields clusters of data points which identify traps that are active (i.e. repeatedly capture and emit) under the recurring measurement cycles. (c) Emission time distributions of active traps fitted according to Eq. (1). (d) Occupancy versus capture interval characteristics of active traps, fitted according to Eq. (2).

II. EXPERIMENTAL DETAILS

Test devices are small-area Si-channel transistors ($\sim 5\times10^{-3}\mu m^2$) with a gate stack comprising either polysilicon/SiO_xN_y (1.7 nm) or TiN/HfO_2(3.5 nm). The electrical testing sequence applied to a p-channel transistor is illustrated in Fig. 1(a). The pristine device is first subjected to 100 pulsed gate-voltage (V_g) cycles for determining the τ_c and τ_e of oxide traps active under the measurement conditions. In each cycle, V_g is first pulsed to −1 V for a duration t_c (capture interval), during which the capture of holes by the traps result in I_d degradation. A −1 V bias is chosen since it is close to the operating voltage. Then, V_g is switched to −0.6 V for 100 s (relaxation interval) during which emissions of the trapped holes result in the recovery of the degraded I_d ($|\Delta I_d|$), manifested as "downward" steps in the $|\Delta I_d|$ versus time curve (Fig. 1(b)). A plot of $|\Delta I_d|$ recovery step heights versus the corresponding emission times (t_e) gives a defect spectral map comprising clusters of data points corresponding to oxide traps which are active under the measurement conditions. For a given active trap, the statistical variation in t_e may be fitted according to [21], [22]

$$p = \frac{t_e}{\tau_e} \cdot \exp\left(-\frac{t_e}{\tau_e}\right) \tag{1}$$

from which the τ_e (@ $V_g = -0.6$ V) may be determined (e.g. Fig. 1(c)); p is probability density function. Since an emission observed during relaxation indicates that the trap involved must be previously charged during t_c, the number of data points in a cluster expressed as a percentage of the total measurement cycles gives the trap's occupancy rate or probability P that a net capture of a hole would occur during t_c. By varying t_c, a trap's τ_c (@ $V_g = -1$ V) may be

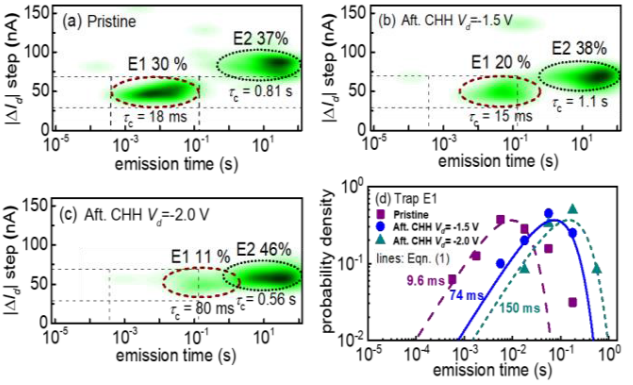

FIGURE 2. Defect spectral maps, represented as kernel plots of $|\Delta I_d|$ recovery step versus emission time of two active hole traps in a SiO_xN_y-gated p-channel transistor. (a) Pristine device; (b) and (c) After stressing the device under channel hot-hole condition at $V_d = -1.5$ V and −2.0 V, respectively with V_g fixed at −1 V. The capture time constant τ_c for the traps, extracted based on Eq. (2), are indicated below the respective clusters. (d) Emission time distributions for trap E1 which is affected by the CHH stress. The extracted emission time constant are as indicated.

extracted from its P versus t_c curve (Fig. 1(d)) according to the following expression: [22], [23]

$$P = \frac{\tau_e}{\tau_e + \tau_c} \cdot \left[1 - \exp\left(-\frac{t_c}{\tau_c}\right)\right] \tag{2}$$

where τ_e is corresponding emission time constant at $V_g = -1$ V. After the above measurement phase, the device is subjected to a channel hot-hole (CHH) stress phase for 100 s. During CHH stress, the applied V_d reduces the oxide field along the channel and this affects the traps' τ_c and τ_e [24], [25]. Thus, trapping characteristics during the CHH stress are not studied. However, it should be noted such τ_c and τ_e changes which arise out of a change in the oxide field are temporary. If the CHC stress did not affect the trap properties, then reapplying the measurement phase after the CHC stress should reveal similar trap behaviors. However, this is not the case for some traps.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows an example of CHH-induced persistent changes in τ_e and τ_c of an oxide trap (E1) in a SiO_xN_y-gated p-channel transistor (similar observations apply to the TiN/HfO_2-gated counterpart). After a 100-s CHH stress at $V_g = -1$ V, $V_d = -1.5$ V, a re-run of the measurement phase clearly reveals a shift of the emission cluster for trap E1 towards a longer time relative to the pristine case (Figs. 2(a), 2(b)). A further 100-s CHH stress at $V_d = -2$ V (with V_g fixed at −1 V) yielded more shift (Fig. 2(c)). To quantify the observed changes, the τ_e (@ $V_g = -0.6$ V) was extracted by fitting the respective te emission time distributions according to Eq. (1) (Fig. 2(d)). τ_e is increased from 9.6 ms (pristine) to 74 ms after the $V_d = -1.5$ V CHH stress and is further increased to 150 ms after the $V_d = -2$ V stress. In addition to the τ_e increase, a decrease of E1's occupancy rate is also seen after the CHH stress. To understand this, E1's τ_c was extracted based on Eq. (2). Interestingly, τ_c is also increased after CHH stress, which translates to a decrease of capture probability

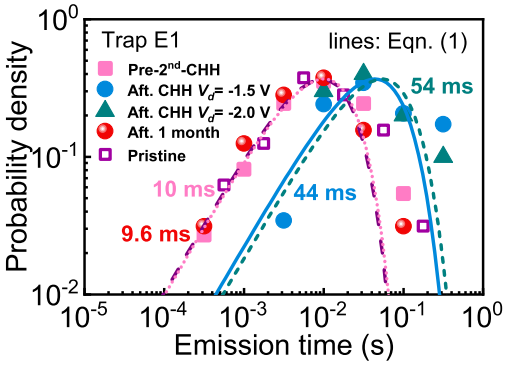

FIGURE 3. Emission time distributions of the same trap E1 as in Fig. 2, before and after the second round of CHH stresses. "Pre-2nd-CHH" denotes the curve measured after a three-day rest period following the first round of CHH stresses.

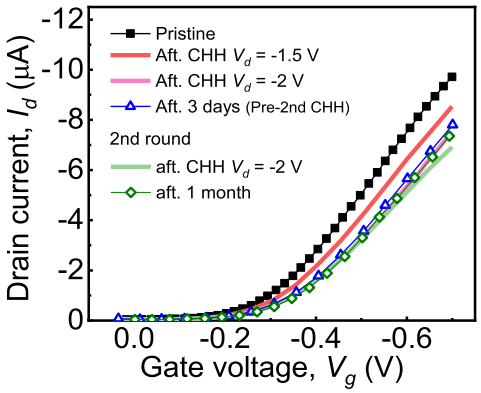

FIGURE 4. Current-voltage transfer characteristic curves of the SiO_xN_y-gated p-channel transistor.

and hence the occupancy rate for a given t_c. In this example, it can be seen that the CHH stress could make an oxide trap less likely to capture a hole but upon a successful capture, the trapped hole would be retained for a longer time.

A recovery of the altered E1's characteristics back to those of the pristine state can be seen after some period of rest. As shown in Fig. 3, the t_e distribution remeasured after leaving the device unbiased for three days (filled square) can be seen to have shifted back and almost coincides with that of the pristine state (open square). This is also accompanied by a restoration of the trap's occupancy rate, indicating that τ_c has also recovered. Applying the CHH stress a second time again shifts E1's t_e distribution towards a longer time and decreases the occupancy rate. A similar restoration back to the pristine state can be seen after the device was left unbiased for one month.

It has been shown that CHH stress generates additional SiO_xN_y/Si interface states [21], [22], [26] which increase V_t and degrade I_d (Fig. 4). To check whether these changes have affected E1's τ_c and τ_e, we compare the changes in the time constants to in the transfer curves. After the first and second round of CHH stress, a near-complete restoration of E1's τ_c and τ_e is seen after three days and one month, respectively as noted above. However, there is no noticeable recovery in the transfer curve for both cases. From these observations,

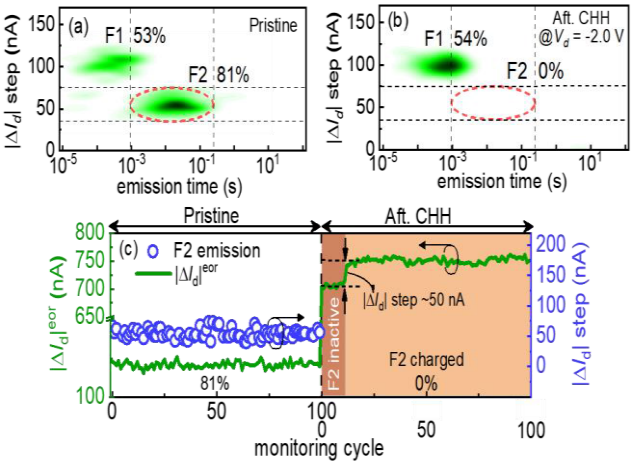

FIGURE 5. Defect spectral map of (a) a pristine SiO_xN_y-gated p-channel transistor and (b) the same device after a $V_d = -2$ V CHH stress. (c) $|\Delta I_d|$ recovery step due to trap F2 emission (circle) and remnant I_d degradation at the end of relaxation, $|\Delta I_d|^{eor}$ (line) as a function of the cycle number. Superscript "eor" denotes end of the relaxation interval in each measurement cycle.

it would be reasonable to exclude the role of V_t and I_d shifts on E1's τ_c and τ_e.

It should be noted that a gradual increase of τ_e after CHH stress, such as the example depicted in Fig. 2, is not always observed. In some cases, the increase is so significant that the emission cluster is shifted entirely out of the measurement "window". Fig. 5 shows an example for another SiO_xN_y-gated p-channel transistor. After the CHH stress at $V_d = -2$ V, $V_g = -1.5$ V, the cluster for trap F2 (Fig. 5(a)) disappears from the spectral map obtained from the re-run of the measurement phase (Fig. 5(b)). To understand this disappearance, we track F2's emission in every measurement cycle (circle in Fig. 5(c)) relative to changes in $|\Delta I_d|^{eor}$, both before and after the CHH stress. $|\Delta I_d|^{eor}$ denotes remnant I_d degradation at the end of relaxation (eor) in each cycle; an increase in $|\Delta I_d|^{eor}$ relative to the previous cycle may imply 1) generation of additional interface states leading to a further I_d degradation and/or 2) one or more oxide traps charged in the present cycle failed to emit during relaxation. An interesting behavior in $|\Delta I_d|^{eor}$ provides a clue for F2's change after the CHH stress. As can be seen, F2 is very "active" before the CHH stress (left panel); emissions, each with a $|\Delta I_d|$ recovery step of ~50 nA, are seen in 81 out of the 100 cycles (circles). Since $|\Delta I_d|^{eor}$ remains constant throughout (line), no additional interface state or oxide trap is generated during the measurement phase and F2 emits in every cycle it is charged. In the remaining 19 cycles where no emission is observed, F2 is not charged. After the CHH stress, a re-run of the measurement phase yielded a higher $|\Delta I_d|^{eor}$ right at the 1st cycle (right panel). This change is ascribed to the additional interface states generated by the CHH stress since the measurement phase itself would not cause any interface or oxide trap generation. After this increase, $|\Delta I_d|^{eor}$ stays constant until the 11th cycle with no emission of F2 observed, implying that F2 is not charged in

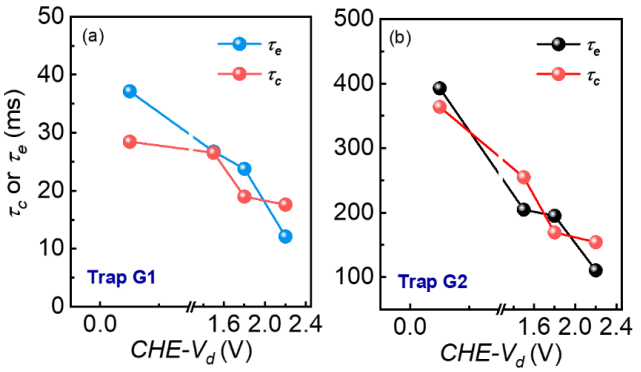

FIGURE 6. Capture and emission time constants τ_c and τ_e, respectively for two active electron traps extracted from the measurement phase performed after each channel hot-electron (CHE) stress. The test device is a TiN/HfO_2-gated n-channel transistor.

the first 11 cycles. At the 12th cycle, an increase of $|\Delta I_d|^{eor}$ by ∼50 nA is observed. This increase is similar to the Id degradation caused by the charging of F2, indicating that F2 is charged at the 12th cycle. After this increase, $|\Delta I_d|^{eor}$ stays at the new level throughout with no emission of F2 observed, implying that F2 remains charged in the remaining 88 cycles. This prolonged trapping of a hole by F2 for at least 8900 s is a huge contrast to the much faster emission time (<0.1 s) before the CHH stress. Due to this significant increase in F2's emission time, both τ_e and τ_c could not be extracted within reasonable experimental timeframe. After a two-month relaxation, F2's capture and emission are restored to the pre-CHH stress behaviors (not shown), like in the case of E1 (Fig. 3).

It should be mentioned that an oxide trap's time constants are not always increased following a CHC stress. In some cases, a decrease is observed. Fig. 6 shows the example of a TiN/HfO_2-gated small-area n-channel transistor studied by a measurement-stress-measurement sequence similar to the p-channel device. After channel hot-electron (CHE) stress, a persistent decrease of trap G1's and G2's τ_c and τ_e (@ $V_g = 1.8$ V)) can be observed, with the decrease becoming more significant after a more severe CHE stress at a higher V_d. The decrease of τ_c and τ_e would mean that the traps can now capture and emit charges more frequently, increasing the frequency of I_d fluctuations in a given time period. For this device, the decrease in τ_c and τ_e persisted for a couple of days before recovering back to the pristine values, similar to the earlier example in Fig. 3.

In our study, we examined a total of 21 oxide traps and changes in the capture/emission characteristics after CHC stress are found in ∼40% of the traps studied. The remaining 60% are relatively immune to CHC stress, even after a severe stress at a high $|V_d|$. Examples include E2 (Fig. 2) and F1 (Fig. 5) in the SiO_xN_y-gated p-channel transistors. As can be seen from the respective spectral maps, there is no apparent change in the trap's occupancy rate and te distribution after a severe CHH stress at $V_d = -2$ V. Similar cases have been noted for the TiN/HfO_2-gated devices.

A relevant question at this point would be the nature of the underlying physical mechanisms that govern the τ_c and τ_e changes observed after CHC stress. Due to the lack of experimental capability in deciphering the atomic origin of the affected oxide traps, the exact details would likely remain elusive for some time. Nonetheless, the importance of interface and oxide traps has prompted many studies aimed at understanding the nature of the defects and thus it would be useful to hypothesize possible mechanisms based on popular theories. Detailed studies on CHC stress have consistently pointed to the dissociation of interfacial Si-H bonds by energetic carriers as the underlying cause for interface state generation [27], with the rate of trap generation dependent on the rate of hydrogen migration away from the dissociated bond sites. This proposed mechanism is supported by an experimentally observed dependence of interface trap generation rate on hydrogen isotopes [28]. On the other hand, there is also a general consensus that a major source of electron/hole traps in gate oxides such as SiO_xN_y and HfO_2 is oxygen vacancies (V_O's) [29], [30]. It has been reported by numerous ab-initio simulation studies that migrating hydrogen in the oxide network could change the properties of V_O's through the formation of hydrogenated E' centers, hydrogen bridges and other complexes, thus affecting the trap levels [31]–[35]. Hydrogen when positive tends to bind to an oxygen; to a silicon when negative [35]. This strong tendency of rebonding could cause large shift in the trap level and change the traps' capture/emission behavior [31]. With the above considerations, we propose a plausible explanation for the changes in τ_c and τ_e observed after CHC stress. During CHC stress, hydrogen released from hot-carrier induced dissociation of interfacial Si-H bonds migrate through the oxide, changing the local lattice environment of the V_O defects via bonding with the oxygen/silicon. This in turn affects the energy levels of the electron/hole traps and the corresponding time constants. W. Goes *et al*. [33] showed that when a hydrogen atom is attached to a V_O defect in SiO_2, the hole trap level of the resultant defect could become deeper. A deep hole trap has a longer emission time than a shallow one. In SiO_xN_y, it was found that a nitrogenated V_O defect (i.e. NO_2Si Si ≡ O_3), where one of the oxygen atoms is substituted by a nitrogen atom, gives rise to a shallow hole trap when the nitrogen binds to a hydrogen atom to achieve the usual three-fold coordination [34]. However, the shallow hole trap could be changed into a deeper one when the hydrogen atom is detached, via for instance interaction with another nearby hydrogen released from the CHC stress. The affected traps may revert to the state before CHC stress when further changes to the local environment arise from phononic perturbations in the oxide network. More studies are needed to validate the hypothesis as well as to understand the different lengths of recovery time of affected traps and why certain traps are immune to the CHC stress.

IV. CONCLUSION

In summary, this study reveals that the τ_c and τ_e of more than a third of the gate-oxide traps in SiO_xN_y- and HfO_2-gated Si transistors are changed by the ubiquitous CHC effect. Follow-

ing varying recovery periods, the affected traps would revert to their pre-CHC stress behaviors and similar changes could be induced by subsequent CHC stresses. It is proposed that hydrogen species released from the CHC effect may bond to the trap sites and thus change the trap levels and the resultant τ_c and τ_e. Such variations may be potentially disruptive to aging models and applications that rely on the presumption that trap properties are invariant. For example, a recent study has proposed the use CHC stress to generate oxide traps as a means for TRNG implementation [14]. Therefore, further studies are required to access the impact of the observed CHC-induced changes in τ_c and τ_e as well as to understand the underlying physical mechanisms.

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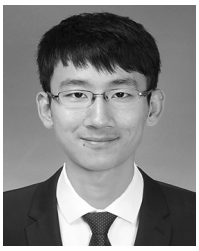

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