IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 6, 2019, accepted January 2, 2020, date of publication January 13, 2020, date of current version January 22, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2966437

Simple and Effective Digital Control of a Variable-Speed Low Inductance BLDC Motor Drive

RODOLFO L. VALLE[1], PEDRO M. DE ALMEIDA[2], GABRIEL A. FOGLI[3], ANDRÉ A. FERREIRA[2], AND PEDRO G. BARBOSA[2]

[1]Electronics Department, Centro Federal de Educação Tecnológica de Minas Gerais, Leopoldina 36700-000, Brazil
[2]Electric Engineering Graduate Program, Universidade Federal de Juiz de Fora, Juiz de Fora 36036-900, Brazil
[3]Department of Electronic Engineering, Universidade Federal de Minas Gerais, Belo Horizonte 31270-901, Brazil

Corresponding author: Pedro M. de Almeida (pedro.machado@ufjf.edu.br)

This work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) under Grant 001, in part by the Conselho Nacional de Desenvolvimento Científico e Tecnológico - Brasil (CNPq), in part by the Instituto Nacional de Energia Elétrica (INERGE), in part by the Fundação de Amparoà Pesquisa no Estado de Minas Gerais (FAPEMIG), in part by the Universidade Federal de Juiz de Fora, in part by the Universidade Federal de Minas Gerais, and in part by the Centro Federal de Educação Tecnológica de Minas Gerais.

ABSTRACT This paper presents a simple digital control applied to a low inductance 5 kW/48 V three-phase brushless DC motor. Controlling the VSI as a full-bridge converter allowed the use of unipolar switching strategy, increasing the output equivalent frequency up to 100 kHz. The aforementioned strategy has made it possible to control the three-phase currents using a single deadbeat controller without a back-EMF feed-forward compensation. Stability analysis is performed to show that the proposed current control presents good transient response under reasonable parametric variations, as well as zero steady-state error. Precise regulation with no overshoot was obtained using an IP controller to regulate the motor speed. Experimental results are presented to validate the theoretical analysis and to compare with a conventional PI compensator and a predictive controller.

INDEX TERMS BLDC motor drive, digital control, deadbeat controller, IP controller.

I. INTRODUCTION

Owing to its advantages as high efficiency, long lifetime, low noise and good speed-torque characteristics, Brush less DC motors (BLDC) holds a great share in applications such as household equipment, industries, aerospace and automotive [1]. In relation to the latter category, when BLDC motors are used to drive electric vehicles (EV), they present a good technical superiority when compared with DC, induction and switched reluctance motors [1], [2].

Regardless their lower volume and weight, which are interesting features for embedded applications, they present low inductance values, resulting in large current and torque ripples [3], [4] which may cause heating, vibration and irreversible demagnetization in the permanent magnets [5]. In order to overcome the aforementioned issues, different converter topologies have been investigated in literature, usually switched at high frequencies, including series inductors or cascaded converters [4], [6]–[9].

Another challenge, which arises due to the motor's low inductance, is the design of current controllers. To ensure precise tracking over a wide range of the motor speed, the controller must present the highest achievable bandwidth, shortening the transient. Concerning the control, there are in the literature a large number of techniques applied to BLDC. It goes from classical linear controller to non-linear approaches. Hysteresis [10], [11] and proportional-integral-derivative (PID) type controllers [12]–[14] are largely employed due its implementation simplicity. However, some issues as variable switching frequency and slow transient response, respectively, limit their application. In order to achieve better performance, more complex control strategies, as well as, modulation techniques [15] has been developed. It can be cited for instance, non-linear controllers as variable structure control [16], fuzzy [17], artificial neural network [18], feedback linearization [19] and backstepping

The associate editor coordinating the review of this manuscript and approving it for publication was Dwarkadas Pralhaddas Kothari.

control [20]. Recently, digital predictive controllers applied to power electronics has draw a lot of attention due its fast transient response, precise current control and full compatibility with digital signal controllers [21]–[24].

Among the predictive controllers there is the deadbeat controller [25]. This controller consists on placing all the poles of the compensated system at the origin of the z-plane, resulting in the fastest achievable response. In order to reach this performance a precise model of the motor and power converter is required. On the other hand, if there are parameters mismatches in the model, significant differences in the time response, steady-state error, oscillations or overdamped transients may occur [7], [26]. Besides that, nonlinearities compensation is very difficult when dealing with deadbeat controller [27].

In sense to reduce the steady-state current error due inaccuracies and non-ideal inverter behavior, a modified predictive current controller including an integrator is proposed in [26]. Despite the fact that integral action eliminates the steady-state error, its time constant drastically affects the currents dynamics, slowing the transient response. Furthermore, if small time constants are used, the system's stability margins may become unreasonable. In [28] this idea applied to a BLDC motor. The slower transient behavior due to the integrator can be clearly observed.

In [7] a predictive current controller with driver parameters compensation is proposed. In spite of the fast response and reduced tracking error, the control law depends on the experimental measurement of parameters as blanking time, pulse drive delay time, semiconductor switches voltage drop and sampling delay. Mismatches in these parameters may affect the current error.

Based on the previous analysis this paper proposes a deadbeat current controller to achieve the highest bandwidth ensuring precise tracking over a wide range of the motor speed. It will be shown that due to the integral action and controller's robustness, the time response presents a good transient behavior and zero steady-state error, even under parametric variations.

The contributions of this paper are the following: *i)* The design of an effective, with reduced number of loops, digital control of a variable-speed low inductance BLDC motor drive. A deadbeat current controller with integral action taking into account only the computational delay is used to this end. This controller ensures robustness under model mismatches without the need of driver's parameters knowledge. Moreover, it is shown that a feed-forward compensation of the back-EMF is not needed, simplifying even more the implementation. *ii)* Reduce the current ripple, without the need to connect any additional series inductance or converter stages. *iii)* The design of digital integral-proportional (IP) controller to regulate the motor speed guaranteeing a good transient behavior without overshoot.

In this way, this work is organized as follows. In Section II the BLDC motor drive and the simplified "pseudo" current are presented. As will be seen, the current flows only

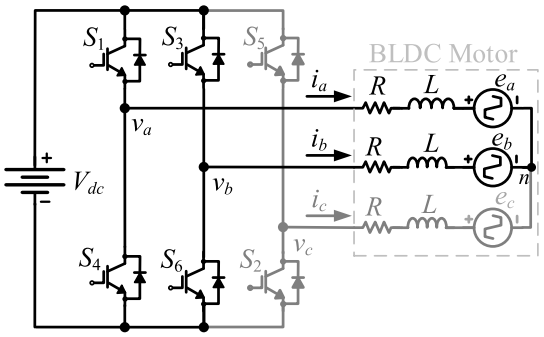

FIGURE 1. Simplified drive schematic.

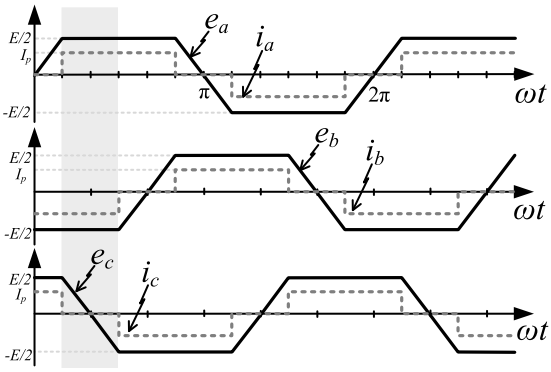

FIGURE 2. Back EMF (continuous lines) and currents (dashed lines) waveforms.

through two phases of the motor at each regular interval of 60°. This feature simplifies the current controller and allows the use of the unipolar PWM pattern increasing the output equivalent switching frequency. Section III presents the modeling of the BLDC motor. Section IV addresses the design of the deadbeat current controller. The system stability is analyzed under uncertainties on the motor's parameters. The laboratory prototype is presented and the experimental results are used to validate the theoretical analysis. In Section V the speed response is approximated by a first order system and an IP controller is used to regulate the speed. Section VI presents some final considerations.

II. BLDC MOTOR DRIVE

Figure 1 shows the schematic diagram of the BLDC motor drive based on a three–phase, two level voltage source inverter (VSI). The back electro-motive force (back-EMF) are represented by the voltage sources e_{an}, e_{bn} and e_{cn}, while R and L are the resistance and inductance of the BLDC phase winding, respectively.

The ideal back-EMF and current in each phase are depicted in Figure 2. Notice that the back-EMFs are trapezoidal shaped while the currents have rectangular like waveform. This combination increases the power density and torque in about 15% for the same current level, avoiding pulsating torques

on the shaft. This feature not only makes the BLDC suitable for small scale EV, but also simplifies the position sensors placement in the machine stator [3]. The last advantage is due the fact that only six different rotor positions must be identified.

As a result of the current shape, only two phases conduct simultaneously as highlighted in Figure 2. Considering that during each $\pi/3$ rad the current flows only by two phases of the motor, it is not necessary to design three but only one current controller. That is, only the following current should be controlled.

$$i_p(t) = \frac{1}{2}\left(|i_a(t)| + |i_b(t)| + |i_c(t)|\right), \tag{1}$$

where i_p is the magnitude of the ''pseudo'' current which flows through the VSI [7], [29]–[31].

Moreover, thanks to the aforementioned characteristic, it is possible to control the VSI as a full-bridge converter, allowing the use of unipolar PWM pattern. The great advantage of this strategy is that the output voltage is switched with a frequency two times higher than the switching frequency of each transistor [32].

III. MODELING

Based on Figure 1 and applying the Kirchhoff's law, the following dynamics can be written for the VSI output ''pseudo'' current

$$\frac{d}{dt}i_p(t) = -\left(\frac{R}{L}\right)i_p(t) + \left(\frac{1}{2L}\right)\left(v_L(t) - e_L(t)\right), \tag{2}$$

where $v_L \in \{v_{ab}, v_{bc}, v_{ca}\}$ and $e_L \in \{e_{ab}, e_{bc}, e_{ca}\}$ are the inverter's output and back-EMF line-to-line voltages, respectively.

Applying the zero-order hold (ZOH) [33] to discretize (2), the following representation is obtained,

$$i_p[k+1] = \Phi i_p[k] + \Gamma\left(v_L[k] - e_L[k]\right), \tag{3}$$

where

$$\Phi = e^{AT_s} = e^{-\frac{R}{L}T_s}, \tag{4}$$

$$\Gamma = \int_{t_k}^{t_{k+1}} e^{A(t_{k+1}-\tau)}Bd\tau = \frac{1 - e^{-\frac{R}{L}T_s}}{2R}, \tag{5}$$

and T_s is the sampling period.

Assuming that the time delay between the sampling and the PWM update is equal to the sampling period, the augmented state-space model of the system is given by

$$\begin{aligned} x(k+1) &= \Phi_d x(k) + \Gamma_d v_L(k) + \Gamma_w e_L(k) \\ y(k) &= Cx(k), \end{aligned} \tag{6}$$

where

$$x(k) = \begin{bmatrix} I_p(k) \\ v_L(k-1) \end{bmatrix}, \quad \Phi_d = \begin{bmatrix} \Phi & \Gamma \\ 0 & 0 \end{bmatrix}, \quad \Gamma_d = \begin{bmatrix} 0 \\ 1 \end{bmatrix},$$
$$\Gamma_w = \begin{bmatrix} \Gamma \\ 0 \end{bmatrix}, \quad C = \begin{bmatrix} 1 & 0 \end{bmatrix}. \tag{7}$$

Based on (6) and (7) it is possible to obtain the following output/input and output/disturbance transfer functions, respectively

$$P(z) = \frac{I_p(z)}{V_L(z)} = C\left(zI - \Phi_d\right)^{-1}\Gamma_d = \frac{\Gamma}{z(z-\Phi)}, \tag{8}$$

$$D(z) = \frac{I_p(z)}{E_L(z)} = C\left(zI - \Phi_d\right)^{-1}\Gamma_w = \frac{-\Gamma}{(z-\Phi)}. \tag{9}$$

The output/input transfer function will be used in the next section to design the digital controller. On the other hand, the output/disturbance transfer function will be used to further evaluate the influence of the disturbance on the current regulation.

IV. DEADBEAT CONTROL DESIGN

In contrast to continuous-time exponential convergence, discrete-time controllers can be designed to track the reference signal without steady-state error after a finite time and follow it exactly thereafter. In deadbeat control, an effort is made to reach the set-point as quickly as possible and stay there, reducing the error to zero in a few samples. However, the minimum time required to reach the set-point, is the dead-time of the system, that is, the intrinsic delay of the system which cannot be compensated [34]. According to the previous features, the deadbeat controller is the fastest achievable digital control, which makes it a suitable strategy for high performance variable speed drives.

Figure 3 depicts the control block diagram, where the inverter is modeled by the V_{dc} gain. A delay z^{-1} is introduced to model the intrinsic computational processing period. $C_{db}(z)$ is the deadbeat controller to be designed. The back-EMF E_L represents a disturbance which can be compensated using a feed-forward action. The control signal V_L is normalized using the voltage at the DC-side to obtain the modulation index m. Moreover, the normalization also reduces the effect of V_{dc} fluctuations in the output current.

Based on Figure 3, the following closed-loop output/reference, sensitivity and output/disturbance transfer functions can be written, respectively

$$C_l(z) = \frac{C_{db}(z)P(z)}{1 + C_{db}(z)P(z)}, \tag{10}$$

$$S(z) = \frac{1}{1 + C_{db}(z)P(z)}, \tag{11}$$

$$C_d(z) = \frac{D(z)}{1 + C_{db}(z)P(z)}. \tag{12}$$

Solving (10) for C_{db} yields

$$C_{db}(z) = \frac{C_l(z)}{[1 - C_l(z)]P(z)}. \tag{13}$$

If the closed-loop transfer function $C_l(z)$ is chosen as z^{-k}, where k depends on the system, the controller is called deadbeat. As a consequence, it can be designed as

$$C_{db}(z) = \frac{1}{[z^k - 1]P(z)}. \tag{14}$$

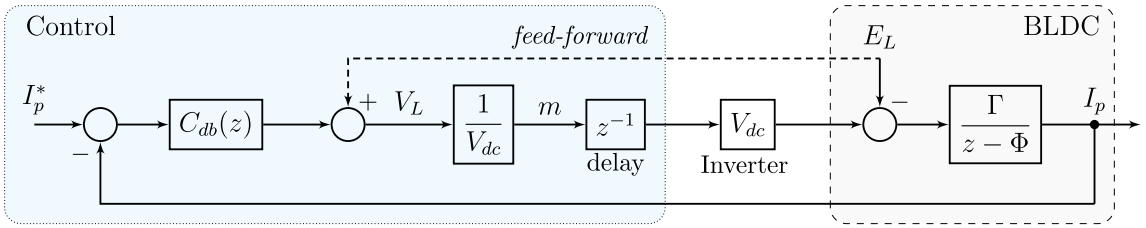

FIGURE 3. BLDC current control block diagram.

According to the transfer function $P(z)$ given in (8), the minimum value of k is 2. Therefore, substituting $k = 2$ into (14), the controller reduces to

$$C_{db}(z) = \left(\frac{1}{z^2-1}\right)\left(\frac{z^2-\Phi z}{\Gamma}\right). \tag{15}$$

Notice that the controller includes a pole at $z = 1$, which presents a practical advantage. This integral action will asymptotically drive the error to zero even if there is parametric uncertainty. It is also worth noting that the deadbeat controller includes the inverted plant model. Therefore, an extra care should be taken if the plant has not minimum phase or slightly damped zeros. This is due the fact that the zeros will become the controller poles, leading to instability or high oscillatory response [33]. For the specific case under study, as the plant does not have zeros, the methodology can be directly applied, resulting in the fasted possible controller without hidden oscillations. The influence of parametric uncertainty is addressed in the next section.

A. STABILITY ANALYSIS UNDER PARAMETRIC UNCERTAINTY

The main concerns when dealing with deadbeat controller are stability and performance under parametric variation. This is due the fact that the controller design is highly dependent on the exact knowledge of the plant's parameters.

The stability analysis may be performed based on the close-loop transfer function given in (10) and the deadbeat controller (15). If the motor's inductance and resistance are exactly known, $C_l(z)$ reduces to z^{-2} (deadbeat, as designed) presenting a Gain Margin (Gm) equal to 6.02 dB, a Phase Margin (Pm) of 60° and a maximum value of the sensitivity transfer function of $\|S(e^{j\omega T_s})\|_\infty = 1.99$. Those stability margins are usually considered reasonable [33], [35]. However, the assumption that the parameters are exactly known or that it will not vary, is an unrealistic assumption. Therefore, an analysis under parametric uncertainty should be performed to set stability boundaries.

Consider for instance that the inductance L_c and the resistance R_c used to design the deadbeat controller differ from the real values L and R. Consequently, the closed-loop transfer function becomes

$$C_l'(z) = \frac{\left(\frac{\Gamma}{\Gamma_c}\right)z - \left(\frac{\Gamma\Phi_c}{\Gamma_c}\right)}{z^3 - \Phi z^2 + \left(\frac{\Gamma-\Gamma_c}{\Gamma_c}\right)z + \left(\frac{\Gamma_c\Phi-\Gamma\Phi_c}{\Gamma_c}\right)}, \tag{16}$$

where Φ_c and Γ_c are the values obtained from (4) and (5) respectively, using L_c and R_c instead of L and R, respectively.

The conditions for stability of (16) can be found using the Jury's Stability Criterion [33]. Applying the aforementioned criterion, results in three complicated inequalities in L, R, L_c, R_c and T_s. This complexity makes it quite difficult to find a reasonable relation among the real values and the ones picked for the controller. Still, if the resistance is neglected, which does not leads to poor approximation (as will be shown later on), a simple relation can be found. Neglecting the resistance, means to take the limit of the inequalities when $R \to 0$ and $R_c \to 0$ resulting in the following single inequality

$$\frac{L_c\,(2L - L_c)}{L^2} > 0, \tag{17}$$

which means that if $0 < L_c < 2L$ the stability is ensured. Since the transfer functions $C_l(z)$ and $C_d(z)$ have the same poles, if the condition (17) is satisfied, the system will be stable as long as the disturbance E_L is bounded.

According to previous analysis, the system will only become unstable if $L_c > 2L$. Fact which does not occur because the uncertainty will not be this large. For this reason, it is important to check whether the time response will be acceptable when there are reasonable parametric errors. This may be performed evaluating the closed-loop poles behavior, as depicted in Figures 4 and 5. Notice that the variation of the resistance value does not have a significant influence on the poles locations as shown in Figure 4. Consequently, it can be neglected when dealing with stability analysis as done before. On the other hand, variations on the inductance leads to a noteworthy change on the poles locus, as can be clearly seen in Figure 5. Take into consideration that when $L < L_c$, the poles moves away from the origin becoming less and less damped until the stability limit $L = L_c/2$ is reached, where there is no damping. The root locus confirms the analysis performed before using Jury's stability criterion.

It is also important to check the stability margins for reasonable parametric uncertainty. Therefore, in Table 1 the stability margins for $L_c = [0.5L, L, 1.5L]$ are shown. Notice that when $L_c < L$ the stability margins are enhanced. As a

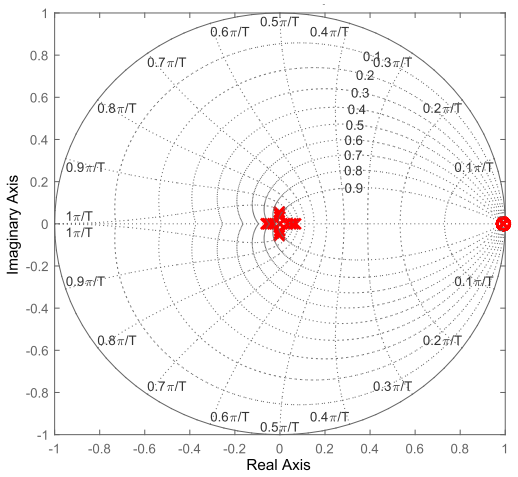

FIGURE 4. Compensated system poles locus under parametric variation: Assuming $L_c = L$ and varying R.

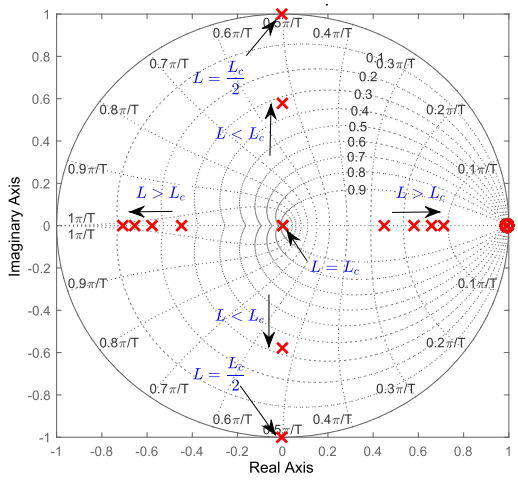

FIGURE 5. Compensated system poles locus under parametric variation: Assuming $R = 0$ and varying L.

TABLE 1. Stability margins under parametric variations.

	Gain margin	Phase margin	$\|S(e^{j\omega T_s})\|_\infty$
$L_c = 0.5L$	12 dB	$[-75.6°, 73.6°]$	1.33
$L_c = L$	6 dB	$[-60°, 60°]$	1.99
$L_c = 1.5L$	2.5 dB	$[-41.6°, 41.6°]$	3.97

consequence, since $\|S(e^{j\omega T_s})\|_\infty$ decreases, the system damping increases resulting in a more damped response. On the other hand for $L_c > L$, $\|S(e^{j\omega T_s})\|_\infty$ increases and the system becomes less damped. This is in accordance with the poles locus analysis.

Based on the previous analysis it can be concluded that even if there are mismatches between the parameters used to design the controller and the real ones, the time response will not drastically change and the stability is ensured as well as good stability margins.

To validate the theoretical analysis, preliminary experimental results are shown in the next section.

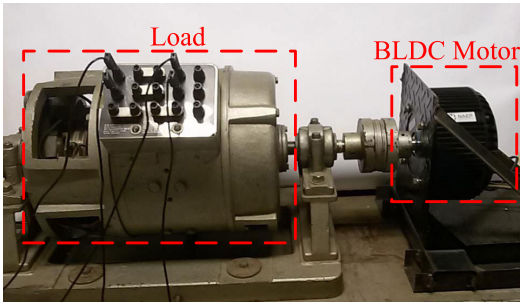

FIGURE 6. Picture of the BLDC motor and load (dc generator).

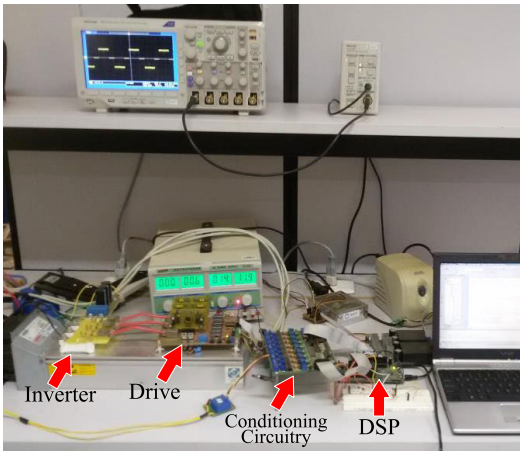

FIGURE 7. Picture of the three-phase inverter and auxiliary circuitry.

TABLE 2. BLDC motor characteristics.

Description	Value
Rated power	5 kW
Rated voltage	48 V
Rated current	100 A
Maximum Efficiency	89.1 %
Resistance per phase	6.2 mΩ
Inductance per phase	14.8 μH
K_{rpm}	0.0125 V/rpm
Number of poles	8
Weight	11 kg
Maximum torque	13.92 Nm
Rated speed	3532 rpm

B. EXPERIMENTAL VERIFICATION

In order to evaluate the time response of designed current controller a prototype was built. The BLDC motor is depicted in Figure 6, whose main parameters are detailed in Table 2. The experimental setup uses DC generator to emulate a variable load. The inverter and the auxiliary circuitry used to control the motor are shown in Figure 7.

Substituting the inductance and resistance values given in Table 2 into (4) and (5), and afterwards into (8) and (9) yields

$$P(z) = \frac{0.6729}{z(z - 0.9917)}, \tag{18}$$

$$D(z) = \frac{-0.6729}{(z - 0.9917)}, \tag{19}$$

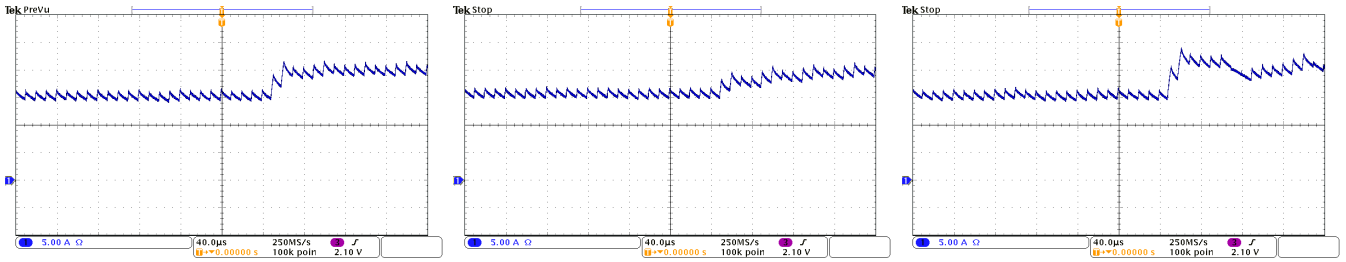

FIGURE 8. Behavior of the i_p current for a step change on the reference signal from 15 A to 20 A. (a) $L_c = L$, (b) $L_c = 0.5L$ and (c) $L_c = 1.5L$.

where the sampling frequency f_s is 50 kHz. The deadbeat controller given in (15) can be rewritten as

$$C_{db}(z) = \left(\frac{1}{z^2 - 1}\right)\left(\frac{z^2 - 0.9917z}{0.6729}\right). \tag{20}$$

Once the controller is designed, the control law depicted in Figure 3 is implemented using a DSP TMS320F28335. The behavior of the $i_p(t)$ current for a step change on the reference signal from 15 to 20 A under three different conditions is shown in Figure 8. It can be clearly seen in Figure 8 (a) that when the inductance used to design the controller is equal to the motor's one, the time response is deadbeat as designed.

On the other hand, when $L_c < L$ the response is overdamped as shown in Figure 8 (b). In the case in which $L_c > L$ (Figure 8 (c)) the system becomes underdamped. This experimental results are in accordance with the theoretical analysis performed in section IV-A.

The three-phase currents in steady state are depicted in Figure 9. Notice that the currents present the same shape of the ideal currents shown in Figure 2. Moreover, this result proves that it is possible to control the three-phase current through the pseudo current, using a single controller. Another important feature is that the waveforms present low switching ripple due to the chosen switching strategy. The unipolar PWM leads to a inverter's output voltage switched with twice the switching frequency of each IGBT. That is, while the switching frequency of each transistor is 50 kHz, the frequency of the output voltage is 100 kHz. This advantage is really important when dealing with low inductance BLDC motors.

It is also important to check whether it is necessary to compensate the back-EMF. Figure 3 presents how a feedforward action can be used to mitigate the effects of E_L. In practice, due to the fringing effect, the back-EMF has the rounded corners differently of the Figure 2 [36]. Thus the voltage amplitude E_L is not flat, but a function of the speed and position rotor. The back-EMF can be compensated by measuring and storing the points of the back-EMF waveform. Afterward, the waveform of the voltage E_L can be obtained by the position and speed of the rotor.

The current step response with and without back-EMF compensation are shown in Figure 10 and 11, respectively.

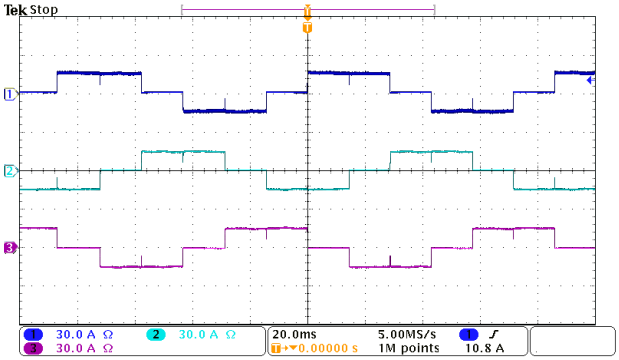

FIGURE 9. Three-phase currents.

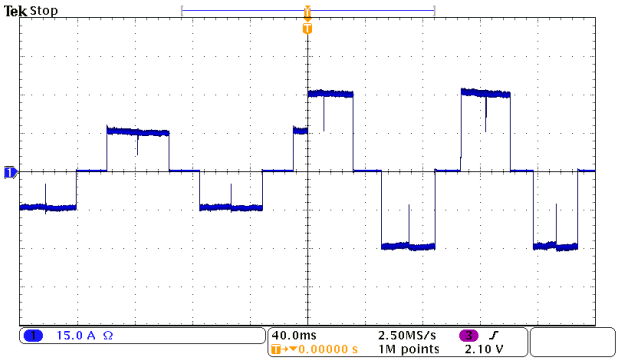

FIGURE 10. Current step response without back-EMF compensation.

Notice that there is no significant improvement on the time response. This can be explained by the fact that the controller's integrator rejects the back-EMF as a disturbance.

Take for instance the closed-loop transfer function between the current I_p and the back-EMF given in (12), rewritten in (21) using the experimental parameters.

$$C_d(z) = \frac{I_p}{E_L} = -\frac{0.6729(z-1)(z+1)}{z^2(z-0.9917)}. \tag{21}$$

Observe that there is one pole of (21) which is not at the origin, meaning that the response related to the disturbance is not deadbeat. As a consequence the plant's pole $z = 0.9917$ dominates the response. The time constant of the dominant

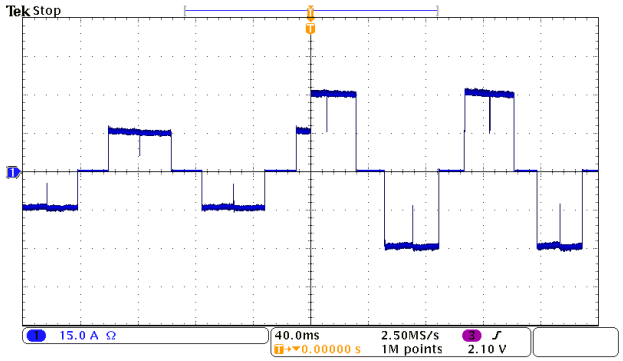

FIGURE 11. Current step response with back-EMF compensation.

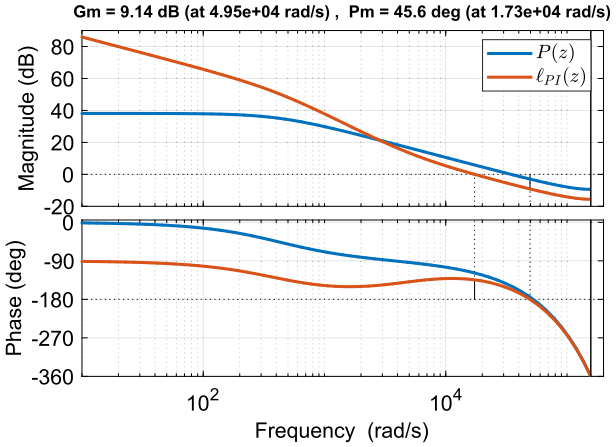

FIGURE 12. Frequency response of the plant and the open-loop with the PI controller.

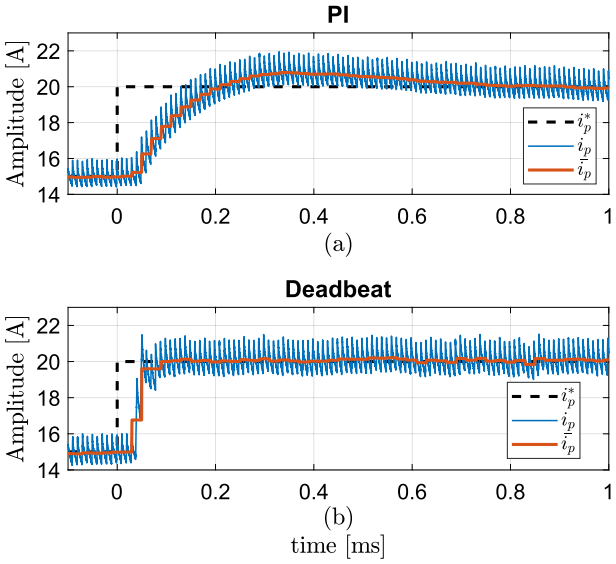

FIGURE 13. Time response under a reference step from 15 to 20 A. (a) PI controller; (b) Deadbeat controller.

pole is approximately 2.4 ms. Therefore in about five time constant the disturbance is completely rejected due the zero at $z = 1$. That explains why the response with and without back-EMF compensation are almost the same. Based on the previous analysis, there is no need to compensate the back-EMF. This fact makes the implementation even simpler.

In order to contrast the performance and features of the proposed controller, its time and frequency responses can be compared with other control strategies. Take for instance a discrete-time PI controller

$$C_{PI}(z) = k_{p,i} + \frac{k_{i,i}z}{z-1}. \tag{22}$$

As a PI controller cannot boost the system's phase, only reduce it, the maximum bandwidth (consequently the minimum settling time) is limited by the plant's open-loop characteristic. Therefore, one of the fastest achievable closed-loop response can be obtained by choosing $k_{p,i} = 0.4647$ and $k_{i,i} = 0.0492$. Those gains were designed to ensure fast response with reasonable stability margins of Gm = 9.14 dB, Pm = 45.6° and $\|S(e^{j\omega T_s})\|_\infty = 1.72$. Figure 12 depicts the frequency response of the plant and the open-loop compensated system with the PI controller. As can be seen, if the crossover frequency is increased, aiming to accelerate the response, the stability margins are reduced resulting in a system with poor robustness characteristics.

For comparison purposes, Figure 13 shows the time response for a reference step from 15 to 20 A. In order to better analyze the figures of merit of the output behavior, the experimental data was collected and plotted in Matlab. A moving average filter with a period equal to T_s was applied to visualize the average values of the switched i_p current, where $\bar{i_p}$ is the filter output. Notice that the settling time for the PI controller is around 0.8 ms. This response is around 10 times slower than the deadbeat one, as can be clearly seen in Figure 13. Furthermore, it presents an overshoot of around 16%, while when the deadbeat is used the system settles without overshoot.

Based on the previous analysis, the comparison between the deadbeat and a PI controller is unfair and we will not make further comparisons. On the other hand, the predictive control can settle the system as fast as the deadbeat, making it a good candidate for comparison purpose. Therefore, the predictive controller designed in [7] was also implemented.

According to [7], the converter's output line voltage, taking into account the delay, is given by

$$v_L(k+1) = 2Lf_s(i_p^* - i_p(k)) - v_L(k) + 2e_L(k). \tag{23}$$

where $v_L(k) = m(k)V_{dc}$.

Substituting (23) into (6), the steady-state value would present a theoretical error of 0.83% since the resistance was neglected. This error is really small, and in fact can be ignored. Moreover, the transfer function of the current $I_p(z)$ regarding the reference $I_p^*(z)$ is equal to z^{-2}. The same as the deadbeat controller. This means that the predictive controller can settle the system as fast as the deadbeat.

However, on the other hand, if the feed-forward action used to compensate the effects of the back-EMF e_L is not used, the transfer function that relates the output current and the

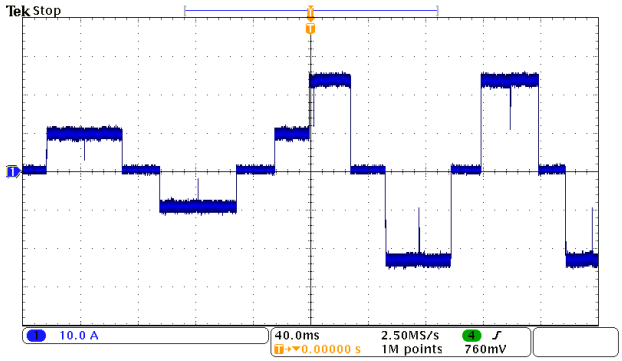

FIGURE 14. Current behavior under a reference step from 15 to 30 A using predictive control law (23) without nonidealities compensation.

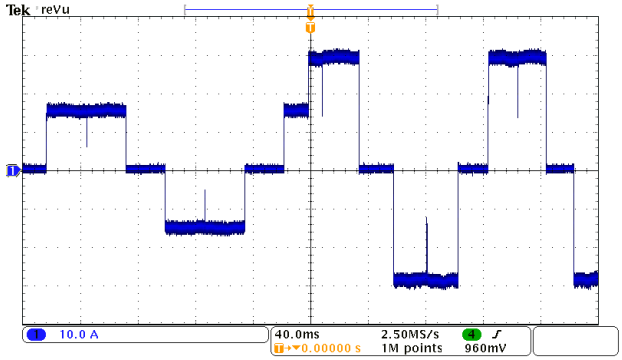

FIGURE 15. Current behavior under a reference step from 15 to 30 A using predictive control law (25) with nonidealities compensation.

disturbance becomes

$$\frac{I_p(z)}{E_L(z)} = \frac{-\Gamma z(z+1)}{z^3 + (1-\Phi)z^2 - \Phi z + 2Lf_s\Gamma}. \tag{24}$$

The transfer function (24) was obtained substituting (23) into (6).

Notice that due the absence of a zero at $z = 1$, the closed-loop system is not able to completely reject the disturbance. Therefore, there will be a steady-state error. As a consequence, the predictive controller cannot be implemented without feed-forward action. Fact that does not happen when the proposed controller is used, as proved by Figure 10.

Figure 14 depicts the time response under a step in the reference from 15 A to 30 A, using the control law given by (23). It is clear that there is a steady-state error of around 5 A. This is due to the nonlinear effects such as blanking-time, voltage drops on the semiconductor switches and delay time of pulse driver [7]. As the predictive controller does not present an integral action, the way to eliminate the steady-state error is to compensate for this these effects, resulting in the following modified control action

$$v_L(k+1) = 2Lf_s(i_p^* - i_p(k)) - v_L(k) + 2e_L(k) + \frac{4T_{BT}V_{dc}}{T_s} + E_L(T_{DD} + T_{SD})f_s + 4V_G, \tag{25}$$

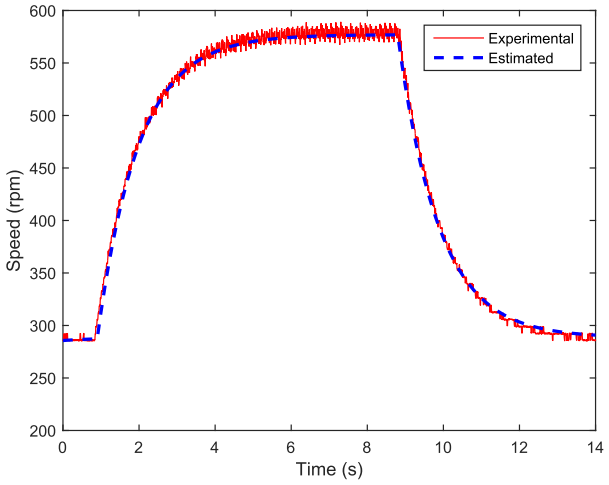

FIGURE 16. Speed behavior under a current step: experimental result and speed response estimated by the approximated model.

where T_{BT}, T_{DD}, T_{SD} and V_G are the blanking time, pulse drive delay, sample delay and voltage drop on the switches, respectively.

Applying the control law (25), the current response to a step in the reference can be seen in Figure 15. Notice that the steady-state error is eliminated. However, the great disadvantage of this technique is that the parameters T_{BT}, T_{DD}, T_{SD} and V_G must be obtained experimentally. Moreover, the back-EMF must be compensated through a feed-forward action in order to achieve zero steady-state error. On the other hand, none of the aforementioned compensations are needed when the proposed controller is used, as shown in Figure 10, simplifying considerably the design and implementation.

V. SPEED CONTROL

The main goal of the drive is to control the EV speed. In this way, an outer speed control loop must be designed. The first step toward this end is to obtain the transfer function which relates the current i_p and the speed w. The transfer function parameters can be estimated based on experimental data. Figure 16 shows the speed response for a current step. The current is reference is changed from 15 A to 30 A. Owing to its fast convergence, the inner current loop dynamics can be neglected. Therefore, the speed dynamics can approximated by the following first order system

$$G(z) = \frac{w(z)}{I_p(z)} = \frac{b}{z-a}. \tag{26}$$

The parameters a and b can be obtained using an estimation method, least-square for instance [33], [34]. For the motor under study, those parameters are found to be $a = 0.99997$ and $b = 3.33715 \times 10^{-4}$. The comparison between the experimental result and the estimated plant is depicted in Figure 16. It can be clearly seen that the dynamics are close related. Consequently, the model is accurate enough to the purpose under study.

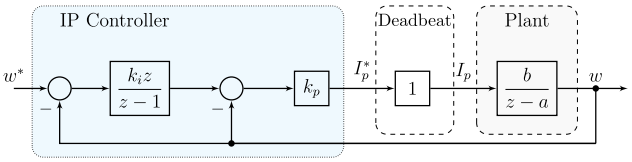

FIGURE 17. Speed control block diagram.

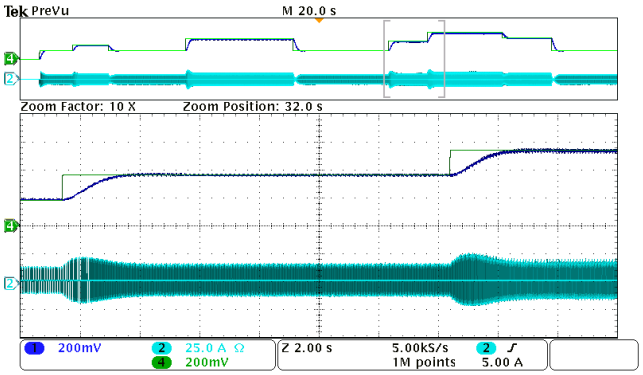

FIGURE 18. Speed behavior under positive step changes in the reference (upper curves) *(vert. scale: 500 rpm/div)*, phase "a" BLDC current (bottom curve).

Once the plant's model is obtained, the outer loop can be designed. Figure 17 depicts the proposed speed control. As mentioned before, due to the fast response of the inner deadbeat current controller, its transfer function is considered ideally equal to one.

In most applications, the speed regulation is performed using a Proportional-Integral (PI) compensator [37]. Although this controller eliminates the steady-state error, the time response presents an overshoot, even if both poles are choosing with unitary damping. The overshoot is caused by the relatively low frequency zero added by the controller. This issue can be avoided using a modified version of the PI, called Integral-Proportional (IP) compensator.

The block diagram of an IP controller is highlighted in Figure 17. The main difference between the PI and IP controllers is that the proportional gain does not directly process the reference. Therefore, if there is a step change in the reference, it is not straight transmitted to the output. Consequently, the overshoot is reduced and the actuator does not saturate, which may occur when PI controllers are employed, depending on the reference value.

Based on Figure 17 the following speed closed-loop transfer function can be written

$$\frac{w}{w^*} = \frac{k_p b k_i z}{z^2 + z(k_p b k_i + k_p b - 1 - a) + a - k_p b}. \quad (27)$$

It must be pointed out that the only zero at the origin does not contribute to the overshoot. As a consequence, if the poles damping are chosen equal to unit, the time response will not present an overshoot.

Comparing the poles of (27) with a canonical second order transfer function represented by the polynomial

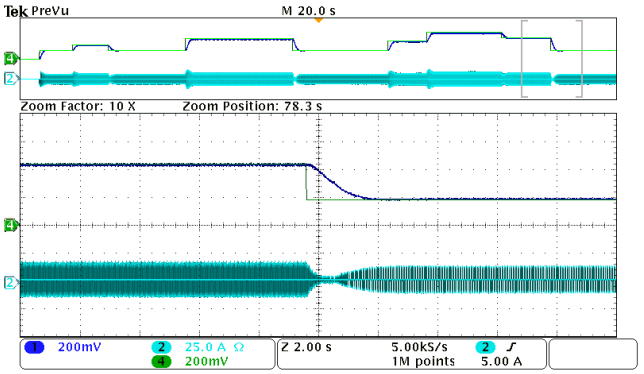

FIGURE 19. Speed behavior under negative step changes in the reference (upper curves) *(vert. scale: 500 rpm/div)*, phase "a" BLDC current (bottom curve).

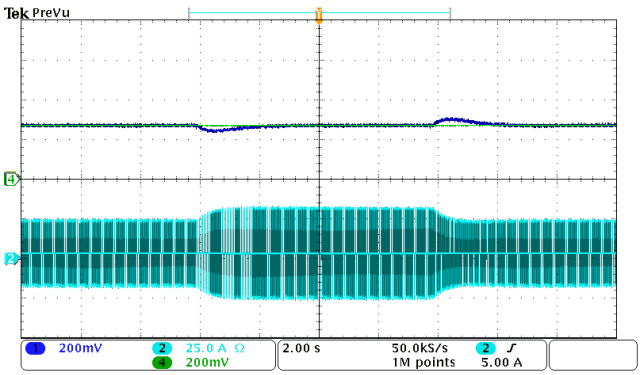

FIGURE 20. Speed behavior subjected to load step. *(vert. scale: 500 rpm/div)*, phase "a" BLDC current (bottom curve).

$z^2 + d_1 z + d_2$ [33], where

$$d_1 = -2e^{-\xi\omega_n T_s} \cos\left(\omega_n T_s \sqrt{1-\xi^2}\right), \quad (28)$$

$$d_2 = e^{-\xi\omega_n T_s}, \quad (29)$$

it is possible to calculate the IP controller's gains based on the damping ratio ξ and the natural frequency ω_n as

$$k_p = \frac{a - d_2}{b}, \quad (30)$$

$$k_i = \frac{d_1 + 1 + a - k_p b}{k_p b}. \quad (31)$$

Choosing $\xi = 1$ and $\omega_n = 2.3$ rad/s the gains are found to be $k_p = 0.2113$ and $k_i = 2.9994 \times 10^{-5}$. The previous gains results in a settling time of around 2 s.

A. EXPERIMENTAL VERIFICATION

In order to evaluate the effectiveness of the designed speed control, the outer loop shown in Figure 17 is implemented. The speed behavior under step changes in the reference is depicted in Figure 18 and 19. Notice in the details, that the system responds exactly as designed. That is, there is no overshoot and it settles in about 2 s.

To complete the analysis, the systems is tested under load steps. Figure 20 shows the speed response for load variation.

It is clear the systems rejects the disturbance in 2 s, presenting maximum/minimum over/undershoot of about 100 rpm.

VI. CONCLUSION

This paper has presented a simple digital control applied to a low inductance 5 kW/48 V three-phase brushless DC motor. Controlling the VSI as a full-bridge converter allowed the use of unipolar switching strategy, increasing the output equivalent frequency up to 100 kHz. Furthermore, it was possible to employ a single deadbeat controller to control the three-phase currents. Due to the integrator on the deadbeat transfer function a zero steady-state error without the need of back-EMF feed-forward compensation was achieved. Moreover, it was shown that the system presents a good robustness level against model uncertainty. The performed analysis have shown that current control presents good response under reasonable parametric variations. Precise regulation with no overshoot was obtained using an IP controller to regulate the speed. Experimental results were presented to validate the theoretical analysis and have shown the advantages of the proposed controller over the PI and predictive control laws.

ACKNOWLEDGMENT

The authors would like to thank UFJF, UFMG, CEFET/MG for the infrastructure, used in the development of this research.

REFERENCES

[1] C. L. Xia, *Permanent Magnet Brushless DC Motor Drives Controls*. Hoboken, NJ, USA: Wiley, 2012.

[2] K. T. Chau, *Electric Vehicle Machines Drives: Design, Anal. Application*. Hoboken, NJ, USA: Wiley, 2015.

[3] R. Krishnan, *Permanent Magnet Synchronous Brushless DC Motor Drives*. Boca Raton, FL, USA: CRC Press, 2010.

[4] J.-O. Krah and J. Holtz, "High-performance current regulation and efficient PWM implementation for low-inductance servo motors," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1039–1049, Sep./Oct. 1999.

[5] M.-K. Seo, T.-Y. Lee, Y.-Y. Ko, Y.-J. Kim, and S.-Y. Jung, "Irreversible demagnetization analysis with respect to winding connection and current ripple in brushless DC motor," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 3, pp. 1–4, Apr. 2018.

[6] B. Singh, V. Bist, A. Chandra, and K. Al-Haddad, "Power factor correction in bridgeless-Luo converter-fed BLDC motor drive," *IEEE Trans. Ind Appl.*, vol. 51, no. 2, pp. 1179–1188, Mar. 2015.

[7] R. L. Valle, P. M. De Almeida, A. A. Ferreira, and P. G. Barbosa, "Unipolar PWM predictive current-mode control of a variable-speed low inductance BLDC motor drive," *IET Electr. Power Appl.*, vol. 11, no. 5, pp. 688–696, May 2017.

[8] V. Viswanathan and J. Seenithangom, "Commutation torque ripple reduction in the BLDC motor using modified SEPIC and three-level NPC inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 535–546, Jan. 2018.

[9] J. Feng, K. Liu, and Q. Wang, "Scheme based on buck-converter with three-phase H-bridge combinations for high-speed BLDC motors in aerospace applications," *IET Electr. Power Appl.*, vol. 12, no. 3, pp. 405–414, Mar. 2018.

[10] F. Rodriguez and A. Emadi, "A novel digital control technique for brushless DC motor drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2365–2373, Oct. 2007.

[11] N. Milivojevic, M. Krishnamurthy, A. Emadi, and I. Stamenkovic, "Theory and implementation of a simple digital control strategy for brushless DC generators," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3345–3356, Nov. 2011.

[12] H.-X. Wu, S.-K. Cheng, and S.-M. Cui, "A controller of brushless DC motor for electric vehicle," *IEEE Trans. Magn.*, vol. 41, no. 1, pp. 509–513, Jan. 2005.

[13] C. S. Joice, S. R. Paranjothi, and V. J. S. Kumar, "Digital control strategy for four quadrant operation of three phase BLDC motor with load variations," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 974–982, May 2013.

[14] G. Buja, M. Bertoluzzo, and R. K. Keshri, "Torque ripple-free operation of PM BLDC drives with petal-wave current supply," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4034–4043, Jul. 2015.

[15] C. Cui, G. Liu, and K. Wang, "A novel drive method for high-speed brushless DC motor operating in a wide range," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4998–5008, Sep. 2015.

[16] N. Milivojevic, M. Krishnamurthy, Y. Gurkaynak, A. Sathyan, Y.-J. Lee, and A. Emadi, "Stability analysis of FPGA-based control of brushless DC motors and generators using digital PWM technique," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 343–351, Jan. 2012.

[17] R. Shanmugasundram, K. M. Zakariah, and N. Yadaiah, "Implementation and performance analysis of digital controllers for brushless DC motor drives," *IEEE/ASME Trans. Mechatronics*, vol. 19, no. 1, pp. 213–224, Feb. 2014.

[18] F. Naseri, E. Farjah, and T. Ghanbari, "An efficient regenerative braking system based on battery/supercapacitor for electric, hybrid, and plug-in hybrid electric vehicles with BLDC motor," *IEEE Trans. Veh. Technol.*, vol. 66, no. 5, pp. 3724–3738, May 2017.

[19] M. S. Boroujeni, G. A. Markadeh, and J. Soltani, "Torque ripple reduction of brushless DC motor based on adaptive input-output feedback linearization," *ISA Trans.*, vol. 70, pp. 502–511, Sep. 2017.

[20] D. X. Ba, H. Yeom, J. Kim, and J. Bae, "Gain-adaptive robust backstepping position control of a BLDC motor system," *IEEE/ASME Trans. Mechatronics*, vol. 23, no. 5, pp. 2470–2481, Oct. 2018.

[21] Y. A.-R. I. Mohamed and E. F. El-Saadany, "An improved deadbeat current control scheme with a novel adaptive self-tuning load model for a three-phase PWM voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 747–759, Apr. 2007.

[22] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*, vol. 40. Hoboken, NJ, USA: Wiley, 2012.

[23] A. Darba, F. De Belie, P. D'Haese, and J. A. Melkebeek, "Improved dynamic behavior in BLDC drives using model predictive speed and current control," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 728–740, Feb. 2016.

[24] A. G. De Castro, W. C. A. Pereira, T. E. P. De Almeida, C. M. R. De Oliveira, J. R. B. De Almeida Monteiro, and A. A. De Oliveira, "Improved finite control-set model-based direct power control of BLDC motor with reduced torque ripple," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4476–4484, Sep. 2018.

[25] W. Jiang, X. Ding, Y. Ni, J. Wang, L. Wang, and W. Ma, "An improved deadbeat control for a three-phase three-line active power filter with current-tracking error compensation," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2061–2072, Mar. 2018.

[26] P. Wipasuramonton, Z. Zhu, and D. Howe, "Predictive current control with current error correction for PM brushless AC drives," in *Proc. IEEE Int. Conf. Electr. Mach. Drives*, May 2005, pp. 558–564.

[27] P. Cortés, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodríguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4312–4324, Dec. 2008.

[28] W. Na, T. Park, T. Kim, and S. Kwak, "Light fuel-cell hybrid electric vehicles based on predictive controllers," *IEEE Trans. Veh. Technol.*, vol. 60, no. 1, pp. 89–97, Jan. 2011.

[29] H. Fakham, M. Djemai, and K. Busawon, "Design and practical implementation of a back-EMF sliding-mode observer for a brushless DC motor," *IET Electr. Power Appl.*, vol. 2, no. 6, pp. 353–361, Nov. 2008.

[30] J. Dixon and L. Leal, "Current control strategy for brushless DC motors based on a common DC signal," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 232–240, Mar. 2002.

[31] C. Berendsen, G. Champenois, and A. Bolopion, "Commutation strategies for brushless DC motors: Influence on instant torque," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 231–236, Apr. 1993.

[32] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters Applications and Design* (Power Electronics: Converters, Applications, and Design), no. 1. Hoboken, NJ, USA: Wiley, 2003.

[33] K. J. Åström and B. Wittenmark, *Computer-Controlled Systems: Theory and Design*. Chelmsford, MA, USA: Courier Corporation, 2013.

[34] K. Moudgalya, *Digital Control*, 1st ed. Hoboken, NJ, USA: Wiley, 2007.

[35] P. Skogestad, *Multivariable Feedback Control 2e*. Hoboken, NJ, USA: Wiley, 2005.
[36] J. R. Hendershot and T. J. E. Miller, *Design of Brushless Permanent-magnet Motors*. Birmingham, U.K.: Motor Design Books, 2010.
[37] M. S. Zaky, "A self-tuning PI controller for the speed control of electrical motor drives," *Electr. Power Syst. Res.*, vol. 119, pp. 293–303, Feb. 2015.

RODOLFO L. VALLE received the B.S. degree in control and automation engineering from the Federal Center of Technological Education of Minas Gerais, in 2010, and the M.Sc. and Dr. Eng. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Brazil, in 2013 and 2017, respectively. Since 2015, he has been a Professor with the Federal Center of Technological Education of Minas Gerais. His research interest includes modeling and control of power electronics converters and variable-speed motor drives.

PEDRO M. DE ALMEIDA received the B.S., M.Sc., and Dr. Eng. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Brazil, in 2009, 2011, and 2013, respectively. He spent a period as a Visiting Scholar in the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2013. Since 2014, he has been a Professor with the Electrical Engineering Department, Federal University of Juiz de Fora. His research interests include control of power electronics, three-phase grid-connected converters, and integration of renewable energy systems.

GABRIEL A. FOGLI received the B.S. degree in electronics and telecommunication engineering from the Pontifical Catholic University of Minas Gerais (PUC Minas), in 2011, and the M.Sc. and Dr. Eng. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Brazil, in 2014 and 2018, respectively. Since 2019, he has been a Professor with the Federal University of Minas Gerais (UFMG). His research interest includes modeling and control of power electronic converters and distributed generation applications.

ANDRÉ A. FERREIRA received the B.S. degree in electrical engineering from the Federal University of Juiz de Fora (UFJF), in 2000, and the M.Sc. and Dr. Eng. degrees in electrical engineering from Campinas State University (UNICAMP), Brazil, in 2002 and 2007, respectively. Since 2009, he has been a Professor with the Electrical Engineering Department, Federal University of Juiz de Fora. His research interests include modeling and control of power electronics converters, electric vehicles, and photovoltaic applications.

PEDRO G. BARBOSA received the B.S. degree in electrical engineering from the Federal University of Juiz de Fora (UFJF), in 1986, and the M.Sc. and D.Sc. degrees in electrical engineering from the Federal University of Rio de Janeiro (UFRJ), in 1994 and 2000, respectively. From 1987 to 1992, he was an Engineer with the Rio de Janeiro Navy Arsenal (AMRJ). From 1992 to 1999, he participated of various research projects at the COPPE-UFRJ Power Electronics Laboratory. Since 2000, he has been with the Department of Electrical Engineering, UFJF, where he is currently a Full Professor. His research area includes power electronics applications in power systems.