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A Ku-Band 6-Bit Vector-Sum Phase Shifter With Half-Quadrant Control Technique

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ABSTRACT This paper presents a 6-bit vector-sum phase shifter with half-quadrant control technique for Ku-band phased arrays. In this paper, the gain and phase symmetry in each quadrant is studied. Based on the gain and phase symmetry in vector-sum phase shifter, the half-quadrant control technique is proposed to simplify the complexity of phase control, phase measurement and phase calibration for large-scale phased arrays. Besides, a phase optimization method without extra phase settings is proposed to achieve low phase error. As results, the measured 6-bit RMS phase error is $1.6^\circ \sim 2.3^\circ$ across $13 \sim 17$ GHz with only 64 different phase states, demonstrating the brevity and accuracy of phase control simultaneously. With the same phase optimization, six chips are measured and the maximum deviation of RMS phase error is $< 0.3^\circ$. The measured peak gain is 3.8 dB at 14.5 GHz, and the measured 3-dB frequency band is $13.4 \sim 15.5$ GHz. The measured RMS gain variation is $0.85 \sim 1$ dB across 3-dB frequency band. The input-referred P1dB is > -11.4 dBm. The chip consumes 29.7 mW with 1.8 V supply and occupies 0.9×1.45 mm^2. This work is fabricated in TSMC 180-nm CMOS technology.

INDEX TERMS Half-quadrant control technique, gain and phase symmetry, vector-sum phase shifter.

I. INTRODUCTION

There is continuous interest in developing new technique to improve the resolution of phase shifter, because of the demanding for accurately beam steering and beam forming in phased-array systems. Phase shifters can be implemented in passive type and vector-sum type. Generally, passive phase shifters are implemented with reflective-type phase shifter (RTPS), switched-type phase shifter (STPS) and transmission line based phase shifter (TLPS) [1]–[3]. The RTPS has compact size and moderate insertion loss [3]. However, limited by the bandwidth of quadrature hybrid and reflective loads, the RTPS features narrow bandwidth. For the STPS and TLPS, high resolution is achieved by cascading multiple cells together. Therefore, high resolution STPS and TLPS suffer from high insertion loss and large chip size. Compared with passive phase shifter, the vector-sum phase shifter features low linearity and power consumption. However, vector-sum phase shifter can provide high resolution with flexible phase calibration, compact size and positive gain [4] – [6], [8], [11]. Hence, vector-sum phase shifter is widely used in millimeter-wave phased arrays [7], [9], [10], where small signals will be processed.

In vector-sum phase shifter, the phase shifting is controlled by scaling the amplitudes of quadrature vectors with variable gain amplifiers (VGA). Therefore, the gain control accuracy has great influence on the phase resolution. In order to improve gain control accuracy, the VGA in vector-sum phase shifter is typically designed with 5- or 6-bit resolution [6]–[9]. With the high control resolution VGA, the ability of flexible phase calibration and improved phase resolution are achieved. However, the high control resolution VGA leads to abundant gain combinations between I- and Q- path VGA and generates a large number of phase settings. Before applying phase shifter in systems, those phase settings need to be measured to conduct phase calibration. Such as the

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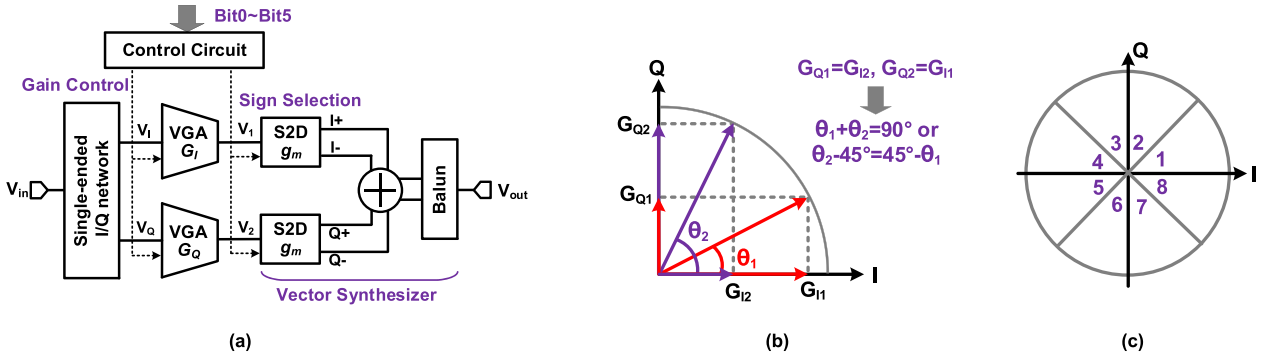
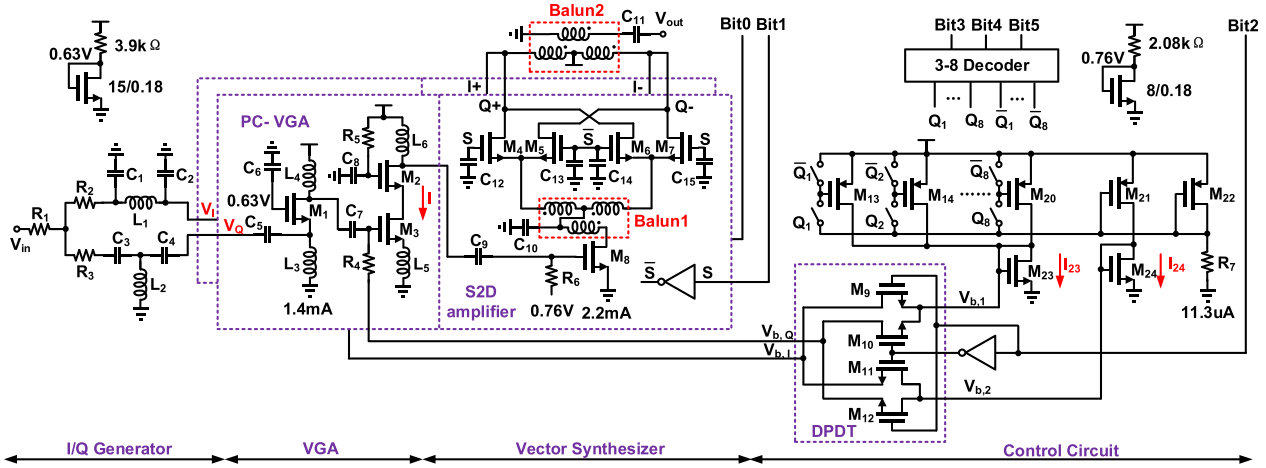


FIGURE 1. (a) Block diagram of the proposed 6-bit vector-sum phase shifter, (b) the illustration of phase and gain symmetry, (c) the eight identical regions based on the half-quadrant control technique.



L_1	486pH	L_2	963pH	L_3	658pH	L_4	575pH	L_5	200pH
L_6	560pH	C_{1-2}	81fF	C_{3-4}	767fF	C_5	483fF	C_6,C_{12-C15}	1.5pF
C_7	385fF	C_8	146fF	C_9	900fF	C_{10}	850fF	C_{11}	220fF
M_1	50/0.18	M_2	120/0.18	M_3	42/0.18	M_{4-7}	80/0.18	M_8	32/0.18
M_{9-12}	80/0.18	M_{13}	1024/0.18	M_{14}	600/0.18	M_{15}	360/0.18	M_{16}	256/0.18
M_{17}	154/0.18	M_{18}	96/0.18	M_{19}	50/0.18	M_{20}	6/0.18	M_{21}	1536/0.18
M_{22}	8/0.18	M_{23-24}	30/0.18	R_{1-3}	16.7Ω	R_{4-6}	5kΩ	R_7	112kΩ

FIGURE 2. The full schematic of the proposed vector-sum phase shifter. All the parameters of devices in schematic are determined after optimizing with layout.

measured results shown in [6] and [8]. As results, the phase shifting measurement and phase calibration in large-scale phased arrays become very complicated.

In order to alleviate this problem, the half-quadrant control technique based on the gain and phase symmetry is proposed. The block diagram of the proposed 6-bit phase shifter is shown in Fig. 1(a), and the gain and phase symmetry is illustrated in Fig. 1(b). As shown in Fig. 1(b), by swapping the gains of VGA in I- and Q-path, two phases centered on 45° will be generated. Based on this mechanism, the 360° is divided into eight identical regions, which is shown in Fig. 1(c). In each region, the number of phase states is one half of that in conventional vector-sum phase shifter. Thus, the number of phase settings is substantially lowered. As results, the proposed phase shifter achieve 6-bit phase resolution with only 64 different phase states. The measured RMS phase error is 1.6° ∼ 2.3° across 13 ∼ 17 GHz, demonstrating high phase resolution and low phase control complexity at the same time.

This paper is organized as follow. In section II, the circuit design of the proposed phase shifter is presented in detail. The measurement results are shown in Section III, and this paper is concluded in Section IV.

II. CIRCUIT DESIGN

The block diagram of the proposed phase shifter is shown in Fig. 1(a). The input signal (V_{in}) is converted into quadrature vectors (V_I, V_Q) by a single-ended I/Q generator. Then V_I and V_Q are scaled by VGA and converted into differential current signals (I+, I-, Q+, Q-) with single-to-differential (S2D) circuit. Finally, the differential quadrature vectors are added in current domain and converted into voltage signal (V_{out}) with the output balun. The gains of VGA and the polarities of the differential quadrature vectors are controlled by the control circuit. The schematic of the proposed phase shifter is shown in Fig. 2.

A. SINGLE-ENDED I/Q GENERATOR

The schematic of the single-ended I/Q generator is shown in Fig. 2. It consists of the resistor based power divider ($R_1 \sim R_3$), T-type high-pass filter (T-HPF, C_3, C_4 and L_2) and π-type low-pass filter (π-LPF, C_1, C_2 and L_1). The 90° phase difference is generated between V_I and V_Q. Both the HPF and LPF can be implemented in T-type and π-type [5]. So there are four combinations (T-LPF & T-HPF, T-LPF & π-HPF, π-LPF & T-HPF, π-LPF & π-HPF) that can generate the 90° phase difference. For the consideration of chip size, the T-HPF and π-LPF are chosen because each of them only contains one inductor. The simulated phase and amplitude mismatches are $< 1°$ and < 0.2 dB across $13 \sim 17$ GHz, respectively, which are shown in Fig. 3.

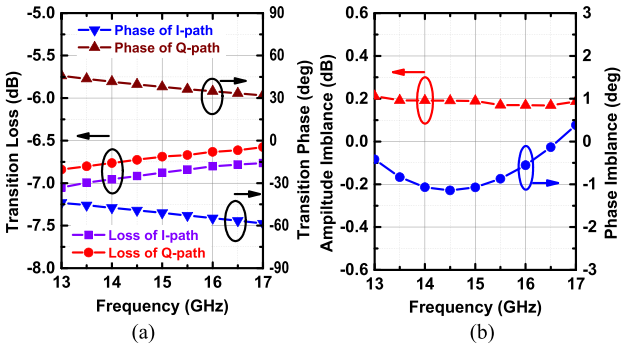


FIGURE 3. Simulated insertion phase and loss of π-LPF and T-HPF, (b) simulated relative amplitude mismatch and quadrature phase error of the quadrature vectors.

B. PHASE COMPENSATED VGA (PC-VGA)

The schematic of VGA is shown in Fig. 2. The common gate amplifier, composed of M_1, is employed to provide impedance match with I/Q generator. The variable gain stage consists of M_2 and M_3. In order to reduce additional phase shift, the capacitor C_8 and the inductor L_5 are used as series feedback elements [13]. The maximum gain tuning range of VGA is simulated and shown in Fig. 4(a). At 14 GHz, the gain of VGA varies from about -26 dB to 5 dB with bias voltage of $0 \sim 1.8$ V, demonstrating the maximum gain tuning range of about 31 dB at 14 GHz. When used in the phase shifter, the gain tuning is achieved by changing the bias current of VGA. Compared with tuning the bias voltage, tuning bias current is more accurate versus process variation, supply voltage variation and temperature because of the application of current mirrors in control circuit. The gain control circuit is shown in Fig. 2. The gain tuning range of VGA is designed about 26 dB to achieve 6-bit phase resolution [12]. As shown in Fig. 2, I denotes the bias current of M_2 and M_3. In order to achieve 26 dB gain tuning range, the bias current of VGA is tuned from 18 uA to 4 mA, which is shown in Fig. 4(b) ~ (c). With I varying from 18 uA to 4 mA, the simulated gain and phase variation of VGA are shown in Fig. 4. The maximum gain variation of VGA is about $23 \sim 28$ dB across $13 \sim 17$ GHz.

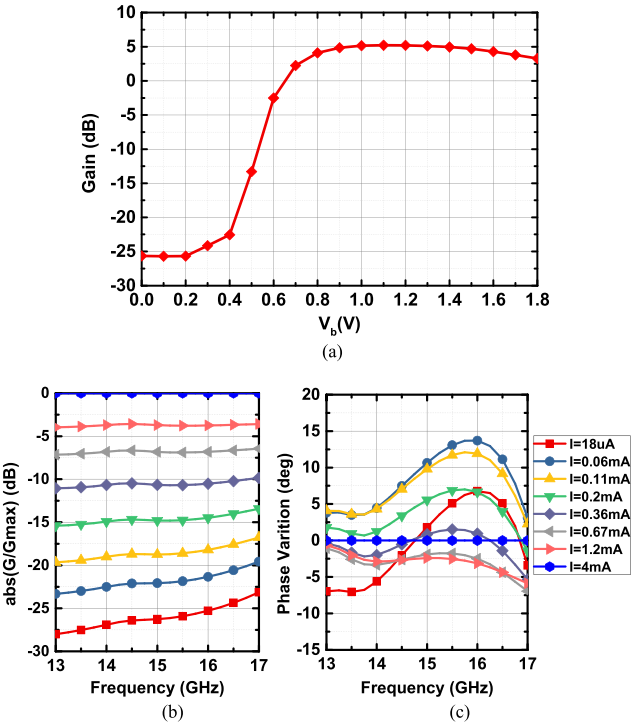


FIGURE 4. (a) Simulated gain tuning range of VGA versus bias voltage V_b at 14 GHz, (b) simulated gain variations of VGA versus bias current I, (c) simulated insertion phase variations of VGA versus bias current I.

The simulated maximum phase variation is about $-7 \sim 14°$ across $13 \sim 17$ GHz. When working in phase shifter, the corresponding bias voltage tuning range is about $374 \sim 823$ mV, which is shown in TABLE 1.

C. VECTOR SYNTHESIZER

As shown in Fig. 2, the vector synthesizer comprises two single-to-differential (S2D) amplifiers, one output balun and a current adder. Because the quadrature vectors flowing into vector synthesizer are single-ended, so the phase shifter can only cover 90°. In order to cover 360°, the quadrature vectors are converted into differential signals (I+, I-, Q+, Q-) with S2D amplifier. In S2D amplifier, balun1 is used to translate the single-ended signal to differential one. Transistors $M_4 \sim M_7$ work as quad-switch and can reverse the polarity of differential signal. By guiding the current flowing through quad-switch to travel through M_8, current-reuse technique is achieved to provide higher gain [5]. The differential quadrature vectors are directly added in current domain with the passive current adder.

The current path and layout of current adder are shown in Fig. 5. Balun2 works as inductive load of the vector synthesizer and translates differential current signal to single-ended voltage signal. The electro-magnetic simulation results of balun1 and balun2 are shown in Fig. 6. By carefully optimizing the offset of stub, the simulated phase and amplitude imbalances of balun2 are $< 1°$ and < 0.1 dB across $13 \sim 17$ GHz, respectively. For balun1, its phase and

TABLE 1. Mapping between phase states and bias.

Region	Phase states	$V_{b,I}$ (mV)	I_I (mA)	$V_{b,Q}$ (mV)	I_Q (mA)	Bit2	Bit5	Bit4	Bit3
1	2.8125°	823	3.86	374	0.013	0	0	0	0
	8.4375°	823	3.86	502	0.2	0	0	0	1
	14.0625°	823	3.86	537	0.35	0	0	1	0
	19.6875°	823	3.86	566	0.53	0	0	1	1
	25.3125°	823	3.86	603	0.82	0	1	0	0
	30.9375°	823	3.86	632	1.1	0	1	0	1
	36.5625°	823	3.86	683	1.72	0	1	1	0
	42.1875°	823	3.86	754	2.73	0	1	1	1
2	47.8125°	754	2.73	823	3.86	1	1	1	1
	53.4375°	683	1.72	823	3.86	1	1	1	0
	59.0625°	632	1.1	823	3.86	1	1	0	1
	64.6875°	603	0.82	823	3.86	1	1	0	0
	70.3125°	566	0.53	823	3.86	1	0	1	1
	75.9375°	537	0.35	823	3.86	1	0	1	0
	81.5625°	502	0.2	823	3.86	1	0	0	1
	87.1875°	374	0.013	823	3.86	1	0	0	0

Note. I_I and I_Q denote the bias currents of VGA in I- and Q-path, respectively.

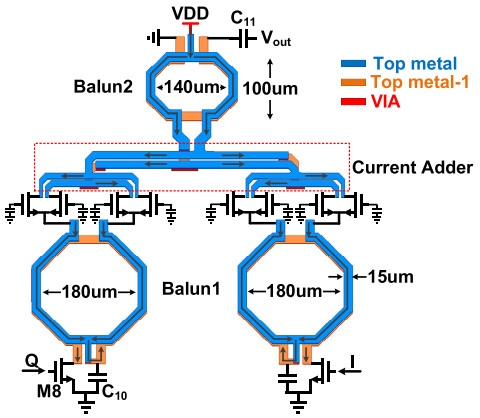


FIGURE 5. The illustration of vector synthesizer.

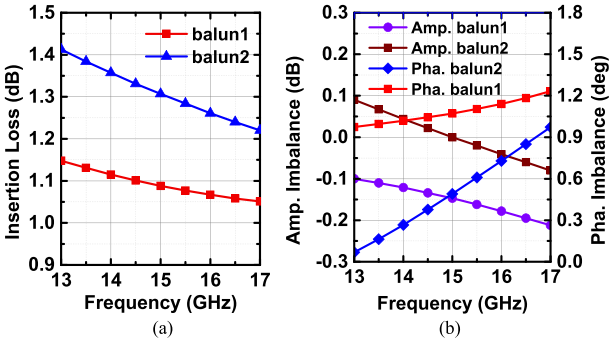


FIGURE 6. (a) Simulated insertion loss of balun1 and balun2, (b) simulated phase and gain imbalances of balun1 and balun2.

amplitude imbalances are tuned by the offset of stub and the value of C_{10}. By optimizing the two parameters, the phase and amplitude imbalances of balun1 are < 0.22 dB and $< 1.2°$, respectively. In 13 $\sim$ 17 GHz, the simulated maximum insertion loss of balun1 and balun2 are about 1.1 dB and 1.4 dB, respectively. The width of metal line is 15 um. The inductance of balun1 of each winding is about 380 pH, while that of balun2 is about 210 pH.

D. CONTROL CIRCUIT

Different from traditional control method, the proposed control method utilizes the half-control technique to divide the 360° into eight regions and reduce the number of control signals. The schematic of control circuit is shown in Fig. 2. It comprises one double-pole double-throw (DPDT) switch, one 3-8 decoder and some current sources. M_{24} is biased with current source M_{21}, so $V_{b,2}$ and I_{24} are constant. M_{23} is biased by current sources $M_{13} \sim M_{20}$, which are digitally controlled with Bit3 $\sim$ Bit5. That is, $V_{b,1}$ and I_{23} are variable and have 8 different states. In this work, I_{23} ($V_{b,1}$) is always no bigger than I_{24} ($V_{b,2}$). The output phase of the phase shifter is given by

$$\theta = arctan\frac{G(V_{b,Q})}{G(V_{b,I})} \tag{1}$$

where $G(V_b)$ denotes the gain of VGA with respect to its bias voltage V_b. In this work, assuming that the VGA always stays away from gain saturation region, therefore the gain of VGA will increase with its bias. When Bit2 $= 0$, $V_{b,I} = V_{b,2}$ and $V_{b,Q} = V_{b,1}$. Then equation (1) is rewritten as

$$\theta_1 = arctan\frac{G(V_{b,Q})_{Q,1}}{G(V_{b,I})_{I,1}} = arctan\frac{G(V_{b,1})}{G(V_{b,2})}. \tag{2}$$

Because of $V_{b,2} > V_{b,1}$, so $G(V_{b,2})$ is bigger than $G(V_{b,1})$ and θ_1 is between 0° and 45°. When Bit2 $= 1$, $V_{b,I} = V_{b,1}$ and $V_{b,Q} = V_{b,2}$. Then equation (1) is rewritten as equations (3) and (4).

$$\begin{aligned}\theta_2 &= arctan\frac{G(V_{b,Q})_{Q,2}}{G(V_{b,I})_{I,2}} = arctan\frac{G(V_{b,2})}{G(V_{b,1})} \\ &= \frac{\pi}{2} - arctan\frac{G(V_{b,1})}{G(V_{b,2})}\end{aligned} \tag{3}$$

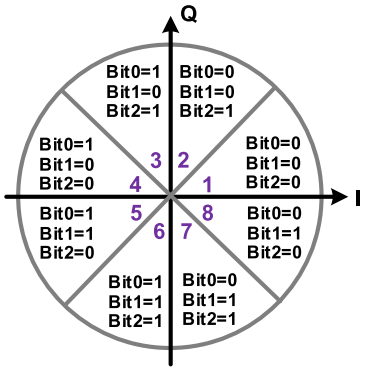


FIGURE 7. Mapping between phase regions and control signals.

$$= \frac{\pi}{2} - \theta_1. \tag{4}$$

Therefore, θ_2 is between 45° and 90°. From equations (2) ∼ (4), it can be concluded that when

$$\theta_1 + \theta_2 = 90^\circ \quad \text{or } \theta_2 - 45^\circ = 45^\circ - \theta_1, \tag{5}$$

then

$$G(V_{b,Q})_{Q,1} = G(V_{b,I})_{I,2} \quad \text{and } G(V_{b,Q})_{Q,2} = G(V_{b,I})_{I,1}. \tag{6}$$

Equations (5) and (6) demonstrate the gain and phase symmetry. According to equations (5) and (6), two complementary output phases are generated by exchanging the gains of VGA in I- and Q-path, making phase control greatly simplified. The gain exchanging is achieved by swapping their bias voltage, which are controlled by signal Bit2 and the DPDT switch. In this manner, the 90° range is divided into two regions, while the 360° range is divided into eight regions. Each region only covers 45° and the number of phase states is half of that in conventional phase shifter. In this work, the phase in each region is controlled by Bit3 ∼ Bit5, while the phase rotation among regions is controlled by Bit0 ∼ Bit2. The mapping between regions and control signals is shown in Fig. 7. Signal Bit2 exchanges the gains of VGA, making phase shifter cover 90°. Signals Bit0 and Bit1 are used to reverse the polarities of differential signals (I+, I-) and (Q+, Q-). As a result, the phase shifter covers 360°.

For a 6-bit vector-sum phase shifter, 8 different phase states will be generated in each region. In order to minimize the gain tuning range of VGA, the minimum phase sate is set as about 2.82°. So, 2.82°, 8.44°, 14.06°, 19.69°, 25.31°, 30.94°, 36.56° and 42.19° will be generated in the first region. In order to achieve 8 different phase states, the 8 current sources (M_{13} ∼ M_{20}) are implemented, which are controlled by the 3-8 decoder. Therefore, only one signal of Q_1 ∼ Q_8 is high level, while only one of the current sources among M_{13} ∼ M_{20} is turned on at any time. According to [12], the VGA with about 26.2 dB gain tuning range is needed to cover those phase states. The current values of M_{13} ∼ M_{20} are decided through simulation. The mapping between bias currents and phase states in region 1 and region 2 is shown in Table 1. Because the biases are repeated between different quadrants, only the mappings in regions 1 and 2 are shown. All current sources are biased with current mirror and use the common bias voltage generated by M_{22} and R_7.

III. MEASUREMENT RESULTS

The proposed vector-sum phase shifter is fabricated in TSMC 0.18-um CMOS technology with size of 0.9 mm × 1.45 mm (Fig. 8). The measurement was done with Agilent vector network analyzer N5247A. The power supply, control signals and ground pads were wire bonded to a PCB. The RF input and output ports of the phase shifter were connected to vector network analyzer with GSG probes and cables.

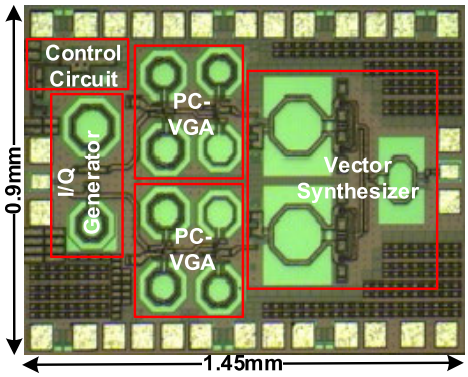


FIGURE 8. Photograph of the vector-sum phase shifter.

The phase shifter consumes 16.5 mA from a 1.8 V supply. The measured 64 different gain states and RMS gain variation are shown in Fig. 9. The measured 3-dB bandwidth of average gain is 13.4 - 15.5 GHz with peak gain of 2.3 dB, while the RMS gain variation is 0.7 ∼ 1 dB across 3-dB bandwidth. The measured input return loss is > 16 dB from 13 ∼ 17 GHz, and the measured output return loss is 5 ∼ 17 dB in 3-dB bandwidth, which are shown in Fig. 10.

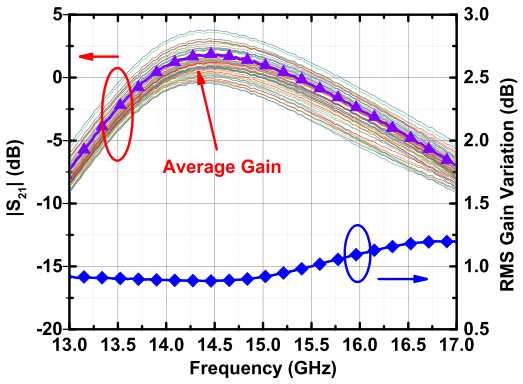


FIGURE 9. Measured gain and RMS gain variation under 64 phase shift states.

The measured 64 phase states are shown in Fig. 11, and the RMS phase error is shown in Fig. 13(a). The RMS phase errors without phase optimization are 3.3° ∼ 5° across

TABLE 2. Performance summary and comparison.

	This work	MTT 2016[7]	MWCL 2018[4]	MWCL 2016[11]	TCAS-II 2018[8]	JSSC 2018[9]	ISSCC 2019[10]	CICC 2015[6]
Technology	**0.18um CMOS**	0.13um BiCMOS	0.13um CMOS	0.25um BiCMOS	45nm CMOS	0.18um BiCMOS	65nm CMOS	65nm CMOS
Topology	**Vector Sum**	Vector Sum	Vector Sum	Vector Sum	Vector Sum	Vector Sum	Vector Sum	Vector Sum
B_{3dB} (GHz)	**13.4-15.5**	3-14	12-18	8-10.5	27-33	28-32	25-30	12-18
Phase Range	**360°**	360°	360°	360°	360°	360°	360°	360°
Phase Resolution	**6bit**	5bit	6bit	6bit	5°	6bit	6bit	5bit
RMS Phase Error	**<2.3°**	<5°	<4°	<6.4°	<0.8°	<5°	<1.4°	<1.2°
RMS Gain Error	**<1dB**	<0.9dB	<0.9dB	≤1.7dB	<0.4dB	<0.7dB	<0.25dB	<1.5dB
Peak Gain	**3.8dB**	0.5dB	0dB	-2.5dB	-5.8dB	1dB	-	1dB
Power Consumption	**29.7mW**	55mW	37.5mW	110mW	25mW	27.7mW	-	92mW
Chip Size (mm^2)	**1.45×0.9**	0.49×0.4	0.75×0.32	1.87×0.88	0.43×0.67	0.54×0.56	0.2×0.44	1.2×1.8

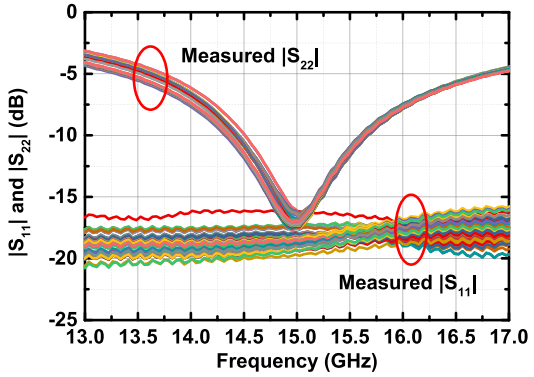


FIGURE 10. Measured return losses of the phase shifter under 64 states.

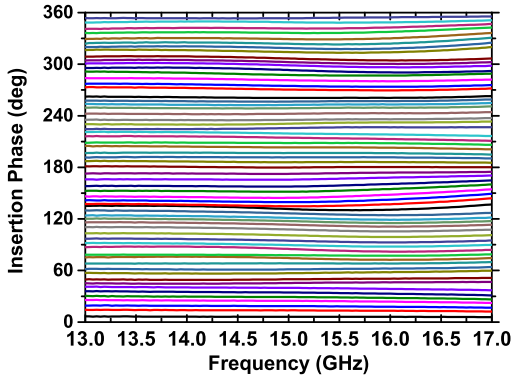


FIGURE 11. Measured 64-state relative phase shifts of the vector-sum phase shifter.

13 ∼ 17 GHz. For a better phase resolution, the phase optimization is conducted. In the measured 64 phase states, if a certain state has a big phase error, this state will be replaced with one of the measured adjacent phase settings to minimize the phase error. Repeating this process for all the phase states, the overall phase errors will be lowered greatly. In this way, although only 64 measured phase states are available, phase optimization for 6-bit phase shifter can also be carried out.

It is possible that identical phase shift is shared by different phase states after phase optimizing. As shown in Fig. 14(a), phase states 3 and 4, 28 and 29, 32 and 33, 58 and 59, 62 and 63 share the same phase shift, respectively. The phase errors of 64 states after phase optimization are shown in Fig. 14(b), and the maximum phase error is $< 3.6°$. The optimized RMS phase errors are $1.5° \sim 2.3°$ across $13 \sim 17$ GHz, which are shown in Fig. 13(a). Fixing the phase optimization, the RMS phase errors and gain variations at 15 GHz across 6 different chips are measured and shown in Fig. 13(b). At 15 GHz, the RMS phase errors vary from 2° to 2.3°, and the RMS gain variations vary from 0.7 dB to 0.85 dB across 6 chips. The measurement results indicate that the phase resolution can be maintained over different chips without re-optimization. The measured input P_{1dB} is $-11.4 \sim -3.2$ dBm across 13 - 17 GHz, which is shown in Fig. 12.

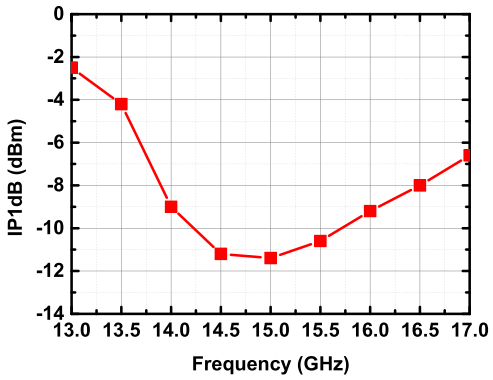


FIGURE 12. Measured input-referred P1dB.

The performances are summarized and compared with other phase shifters in Table 2. Generally, RMS phase error and gain variation can be greatly lowered by calibration. The more phase settings are available, the better phase calibration can be conducted. Benefited from the proposed half-quadrant phase control technique and phase calibration method, the proposed vector-sum phase shifter achieves 6-bit phase resolution with only 64 different phase states.

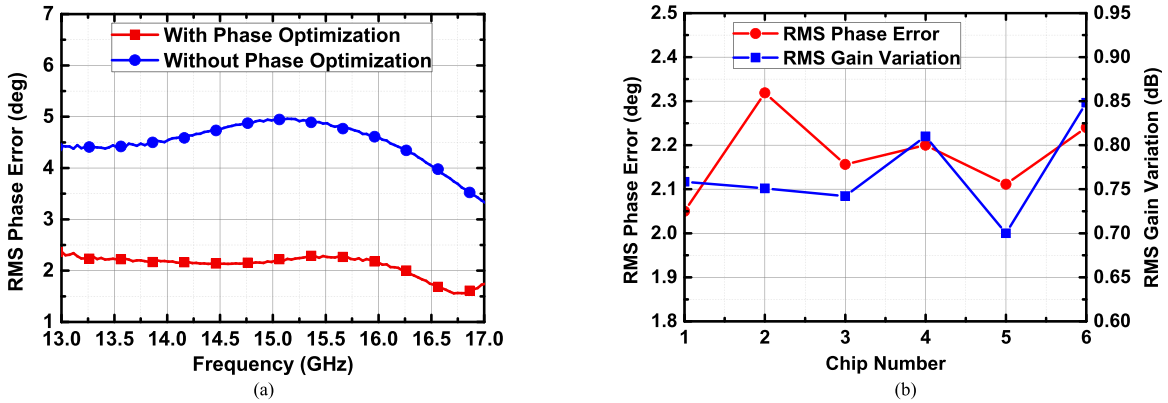


FIGURE 13. Measured RMS phase errors with and without phase optimization, (b) measured RMS phase errors and RMS gain variations with the same optimization across 6 chips at 15 GHz.

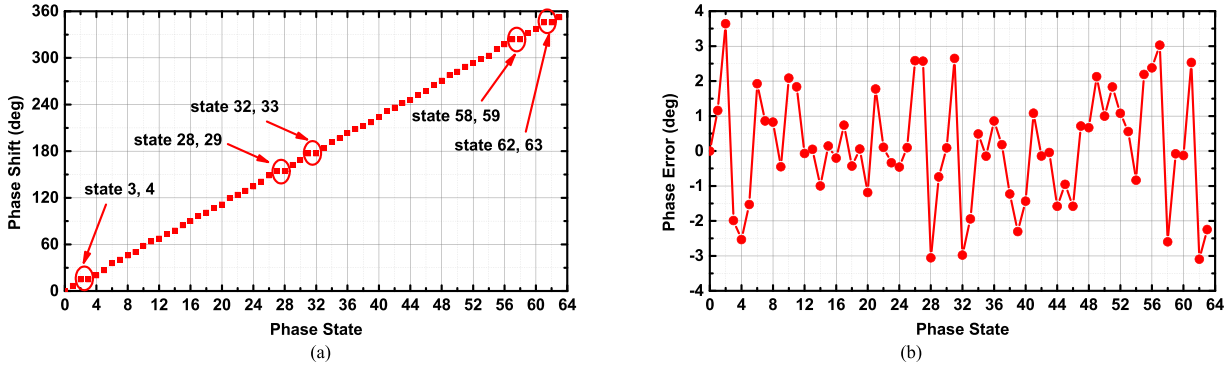


FIGURE 14. (a) The optimized relative phase shift for 64 states at 15 GHz, (b) the optimized phase errors for 64 phase states at 15 GHz.

IV. CONCLUSION

In this paper, a novel half-quadrant control circuit based on the gain and phase symmetry is proposed. Compared with conventional vector-sum phase shifter, the control signals are greatly reduced, while the complexities of phase measurement, phase control and phase calibration in large-scale phase arrays are greatly lowered. As results, the proposed phase shifter use only 6-bit control signals and achieves 6-bit phase resolution, with RMS phase error of 1.5° $\sim$ 2.3° across 13 $\sim$ 17 GHz. The excellent performances and low phase measurement and calibration complexity demonstrate that the proposed phase shifter is a great candidate for large-scale phased-array systems.

REFERENCES

[1] T.-W. Li and H. Wang, "A millimeter-wave fully differential transformer-based passive reflective-type phase shifter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2015, pp. 1–4.

[2] G.-S. Shin, J.-S. Kim, H.-M. Oh, S. Choi, C. W. Byeon, J. H. Son, J. H. Lee, and C.-Y. Kim, "Low insertion loss, compact 4-bit phase shifter in 65 nm CMOS for 5G applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 37–39, Jan. 2016.

[3] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *Proc. 2016 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, San Francisco, CA, USA, May 2016, pp. 356–359.

[4] Z. Duan, Y. Wang, W. Lv, Y. Dai, and F. Lin, "A 6-bit CMOS active phase shifter for ku-band phased arrays," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 7, pp. 615–617, Jul. 2018.

[5] Y. Yu, K. Kang, C. Zhao, Q. Zheng, H. Liu, S. He, Y. Ban, L.-L. Sun, and W. Hong, "A 60-GHz 19.8-mW current-reuse active phase shifter with tunable current-splitting technique in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1572–1584, May 2016.

[6] T.-W. Li, J. S. Park, and H. Wang, "A 2–24GHz 360° full-span differential vector modulator phase rotator with transformer-based poly-phase quadrature network," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2015, pp. 1–4.

[7] M. Sayginer and G. M. Rebeiz, "An eight-element 2–16-GHz programmable phased array receiver with one, two, or four simultaneous beams in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4585–4597, Dec. 2016.

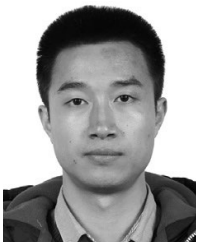
[8] J. Xia and S. Boumaiza, "Digitally assisted 28 GHz active phase shifter with 0.1 dB/0.5° RMS magnitude/phase errors and enhanced linearity," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 66, no. 6, pp. 914–918, Jun. 2019.

[9] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2 × 2 beamformer flip-chip unit cell," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, May 2018.

[10] J. Park, S. Lee, D. Lee, and S. Hong, "9.8 A 28 GHz 20.3%-transmitter-efficiency 1.5°-phase-error beamforming front-end IC with embedded switches and dual-vector variable-gain phase shifters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 176–178.

[11] B. Cetindogan, E. Ozeren, B. Ustundag, M. Kaynak, and Y. Gurbuz, "A 6 bit vector-sum phase shifter with a decoder based control circuit for X-band phased-arrays," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 64–66, Jan. 2016.

[12] M.-M. Mohsenpour and C. E. Saavedra, "Variable 360° vector-sum phase shifter with coarse and fine vector scaling," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2113–2120, Jul. 2016.
[13] F. Ellinger, U. Jorges, U. Mayer, and R. Eickhoff, "Analysis and compensation of phase variations versus gain in amplifiers verified by SiGe HBT Cascode RFIC," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 1885–1894, Aug. 2009.



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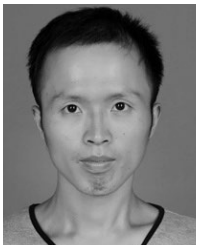

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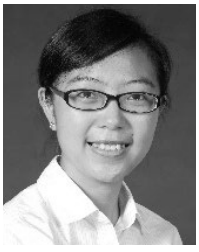

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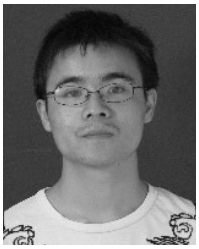

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