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Low Power and Ultrafast Multi-State Switching in nc-Al Induced Al_2O_3/Al_xO_y Bilayer Thin Film RRAM Device

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ABSTRACT Low power and ultrafast multi-state storage resistive switching memory (RRAM) device had been developed based on $Al/Al_2O_3/Al_xO_y/Al$ structure. Both of Al_2O_3 and Al nanocrystal (nc-Al) induced Al_xO_y thin films were deposited by RF sputtering. The nc-Al Al_xO_y based RRAM device showed typical unipolar switching behavior which was due to conductive filaments (CFs) connected and broke in Al_2O_3/Al_xO_y layers. An additional 30 nm Al_2O_3 thin film would deposit on Al_xO_y film to form bi-layer structure, in which the multi-state switching could be observed by applying different voltage pulses on it. In this study, a 15 V pulse with 600 ps width could trigger RRAM device switch from high resistance state(HRS)to next intermediate resistance state (IRS), the device could finally switch to LRS after continuous pulse simulation. Such switching from HRS to LRS was called ''writing'' process as data would be stored in RRAM device after this process. A longer but lower amplitude voltage pulse was required to make device switch from LRS to HRS which was called ''erasing'' process, as data would be eliminated after this process. The multi-state switching was corresponding internal switching between these IRSs during ''writing'' and ''erasing'' process. The multi-level resistances might be caused by partially formed CFs in Al_2O_3/Al_xO_y layers. The distribution of CFs could be controlled by controlling the shape of pulse voltage to achieve this multi-state storage. This bilayer structured RRAM device had good endurance and retention performances at both room and high temperatures.

INDEX TERMS Multi-state switching, nc-Al, RRAM.

I. INTRODUCTION

Nowadays, metal oxides based RRAM has many advantages in terms of the simple composition, facile fabrication process and excellent compatibility with current CMOS technology [1]–[6]. Among these metal oxides materials, Al_2O_3 as popular high-k material is found to exhibit typical switching property in some studies [7]–[9]. Based on the operating electrical polarity for resistance switching, RRAM can be classified into two different types: bipolar resistance switching (BRS) [10]–[12] and unipolar resistance switching (URS) [13]–[15]. For BRS, the off and on resistance states could be achieved only after applying voltages with certain polarities. It shows faster switching speed, lower operation energy cost and better endurance and uniformity properties. While for URS mode, owing to the single polarity operation, it allows RRAM with crossbar structure to support large-scale integrated circuits design.

Beneficial to high density data storage, multi-state switching had been demonstrated in both BRS [16]–[19] and URS [20], [21] devices. The possibility of having multiple resistance states in a single RRAM memory cell enables it to achieve high-density memory for multilevel information processing and data storage applications. Instead of only scaling down the dimensions of a memory cell for high-density memories, the utilization of IRSs between HRS and LRS to realize multi-state storage within single RRAM cell is an efficient solution to increase the storage density of the memory devices. However, for single layer Aluminum oxide based unipolar RRAM device, the multi-state switching is rarely to observe [9]. The variability in current-voltage (*I-V*) measurement is hardly to form stable multi-state storage in device operation. A new structured RRAM device need to be developed to solve this problem. In this way,

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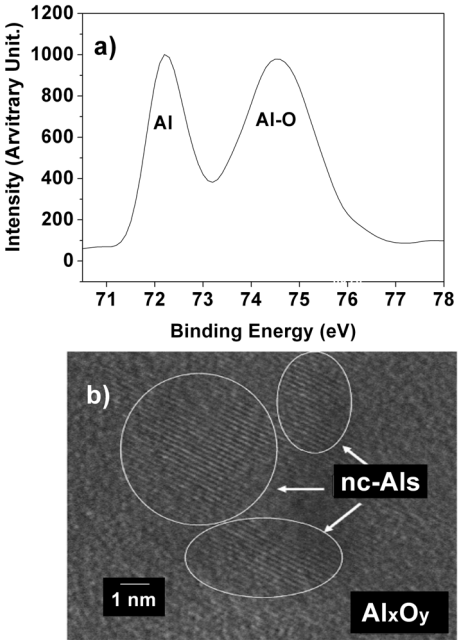

FIGURE 1. **(a) XPS and (b) TEM results of nc-Al induced Al_xO_y thin film. The diameter of nc-Als are around 5-10 nm.**

low power and ultrafast multi-state switching in Al/Al_2O_3/nc-Al Al_xO_y/Al bilayer RRAM device has been demonstrated in this paper, which is rarely to be published before. Such multi-state RRAM is good candidate of next generation memory device.

II. EXPERIEMNT

A 500nm Al film is deposited on p-type silicon wafer by using e-beam evaporation. Al_xO_y layer is deposited by RF sputtering with 99.99% pure Al target. The flow gas rate Ar:O_2 is 50:1 sccm and base pressure is about 1 Pa. The sputtering power kept at 150 W. A 200 °C 2 min annealing process is followed after Al_xO_y deposited to form nc-Al inside the film. The second Al_2O_3 layer is deposited by RF sputtering with pure Al_2O_3 target. The power keeps at 200 W and base pressure is 1 Pa. The thickness of Al_xO_y and Al_2O_3 thin film are both equal to ∼30 nm. The thickness is measured by step profiler. The top circle electrode Al is deposited by using E-beam evaporation with diameter 100 μm and thickness 500 nm. The *I-V* measurement is executed by Keithly 4200 at room (25 °C) and high temperature (85 °C).

III. DISCUSSION

The Figure 1(a) shows the XPS results of Al_xO_y thin film. There are two peaks of Al-O (74.6 eV) and metallic Al (72.4 eV) are observed, which indicates Al_xO_y layer is high of Al concentration film. It is because nc-Al will form and embedded in Al_xO_y film after annealing process. These nc-Als could be part of CFs which are basic condition of URS occurs. To prove exist of nc-Al, the TEM result of Al_xO_y layer is shown in inset of Figure 1(b). The nc-Als with diameter ∼5-10 nm could be observed clearly. The Al_2O_3 layer is an ordinary film which is not shown here.

Figure 2(a) shows the schematic diagram of the bilayer RRAM structure, where the Al is served as bottom and top electrodes. Figure 2(b) and (c) show the URS behavior at room temperature. The multi-state storage can be realized by controlling the compliance current (I_c). Prior to the test, an electroforming at ∼8 V with compliance current 50mA is utilized to trigger stable URS. After forming process, the I-V measurement of Al/Al_2O_3/nc-Al Al_xO_y/Al bilayer RRAM device exhibits typical unipolar switching. The switching process from the HRS to LRS and from LRS to HRS are corresponding to set and reset process as shown in Figure 2(b) and (c) respectively. For the oxide film-based URS RRAM device, it is suggested that by setting different I_c during set and reset process, the statuses of CFs can be controlled to obtain multiple resistance states [22]–[24].

The I_c is setting to 10 μA, 100 μA, 1 mA and 10 mA in both set and reset processes. In the set process, the voltage biased from 0 V to 3.5 V with step of 0.01 V as shown in Figure 2(b). The initial resistances are almost same. From this figure, it is clear to see that higher I_c of 10 mA will cause switching occur earlier at V_{set} equal to 1.4 V. As I_c decreased to 10 μA, the V_{set} will increased to 2.8 V. It seems RRAM need less time to switch-on at higher I_c. The reset process is shown in Figure 2(c). As I_c increased, the V_{reset} will decrease from 1.2 V to 0.5 V accordingly. It means a higher I_c may cause device switch-off faster, which is similar with the situation in set process. It is necessary to point out the breakdown of CFs is mainly dependent on power consumed on device not only depend on the value of V_{reset}. Even the higher I_c caused lower V_{reset}, the power work on it is still quite high. From these tow figures, it conclude that the device will experienced faster switching on and off in voltage biasing measurement if higher I_c applied.

The mechanism of multi-states could be explained in Figure 2(d). The initial state is high resistance state (HRS) in which only little Al vacancy (V_{Al}^-) and oxygen vacancy (V_o^+) exist in Al_2O_3 and nc-Al Al_xO_y layers respectively. Both of V_{Al}^- and V_o^+ could be part of CFs as ion migration is the key point in switching mechanism [25], [3]. However, the more accurate mechanism needs further study in our future work. As shown in IRS1 state, when top electrode applied positive voltage, V_{Al}^- will accumulate at interface of top electrode and Al_2O_3 layer, the growth direction of CFs is from top electrode to bottom electrode. At the other side electrode, the V_o^+ will accumulate at interface between bottom electrode and Al_xO_y layer. The CFs growth direction will point from bottom electrode to top electrode. As the I_c increased, the CFs in IRS2 state will continuously grow in the indicated direction. The IRS1 and IRS2 are different internal resistance states with different I_c applied, in which partially CFs will form with different shapes. Obviously, the IRS2 state will get higher conductance than IRS1 state which is corresponding with previous result, that is higher I_c will produce stronger CFs and make device conductance increased. To breakdown strong CFs need more power than delicate ones. One more thing need to point out is that the IRSs in our device should

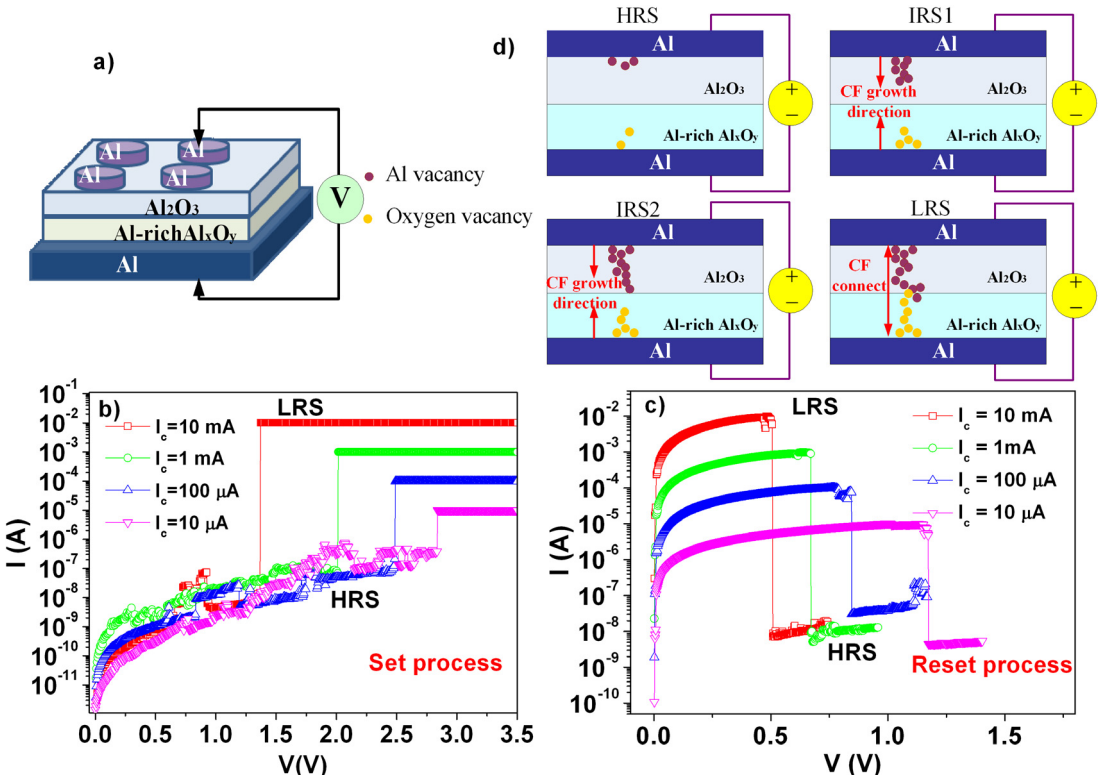

FIGURE 2. (a) Device structure with typical MIM sandwich structure; (b) the set process at different I_c equal to 10 μA, 100 μA, 1 mA and 10 mA; (c) the reset process at different I_c equal to 10 μA, 100 μA, 1 mA and 10 mA; (d) the mechanism of multi-states in Al_2O_3/nc-Al Al_xO_y bilayer RRAM device, the partially formed CFs will affect device conductance as while.

be more than two states (IRS1 and IRS2), which is totally dependent on the formation of CFs in Al_2O_3/Al_xO_y layers. In this way, it is possible to develop multi-state RRAM to multi-bit memory device in the future. When CFs connected the top and bottom electrodes, the device will switch to LRS finally. It could be achieved when device goes through high enough I_c and voltage biasing.

Figure 3(a) and (b) are statistic graphs of V_{reset},V_{set} and I_c. From the figures, both V_{reset} and V_{set} are reduced with decreased I_c. However, there is no strong evidence to define the set and reset voltages are dependent on I_c, the switching parameters should be more relate to f CFs formed and broke in film itself. For certain device, V_{reset} and V_{se} exhibit correlation with I_c, that is the higher I_c may result lower V_{reset} and V_{set} as required power consumption is fixed.

The multi-state resistances of this RRAM device measured at 0.1 V is summarized in Figure 3(c). The measured HRS resistance is $\sim 3\times 10^7\,\Omega$. When I_c is setting equal to 0.01 mA, 0.1 mA, 1 mA and 10 mA, the measured resistance are equal to $\sim 4\times 10^4\,\Omega$, $\sim 7\times 10^3\,\Omega$, $\sim 1\times 10^3\,\Omega$ and $\sim 2\times 10^2\,\Omega$ respectively. From this figure, it is clear to see that these multi-states are quite stable and could be distinguished with each other obviously. Such multi-states could be obtained by setting different I_c value for our device. At the meanwhile, the device could also switch from HRS to IRS1, IRS2 until to LRS by applying continuously increased voltage pulses as shown in Figure 3(d). The voltage pulses of 5 V, 7 V,

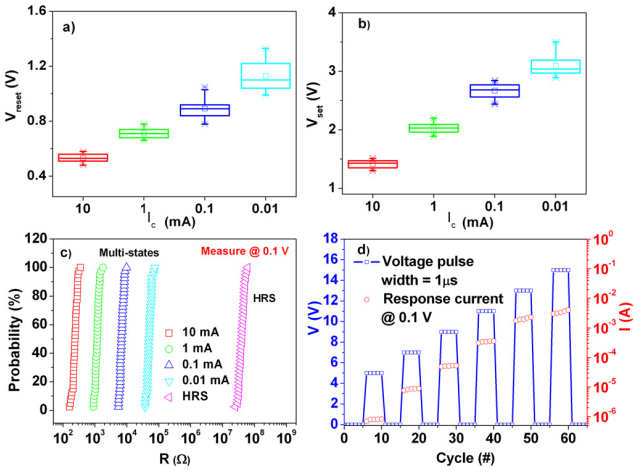

FIGURE 3. (a) Statistic graph of reset voltage and compliance current; (b) statistic graph of set voltage and compliance current; (c) resistance distribution obtained form 80 sweep cycles; (d) the device conductance increased with increasing applied positive pulse voltage.

9 V, 11 V, 13 V and 15 V with width of 1 μs are applied to device successively. The device conductance is found to increase with the increased value of applied pulse voltage. It means the switching between these IRSs could be controlled by voltage pulse as while. A pulse-controlled RRAM is really important in memory device development. At the same time, the future RRAM also need faster switching speed in practical applications which will be investigated in following part.

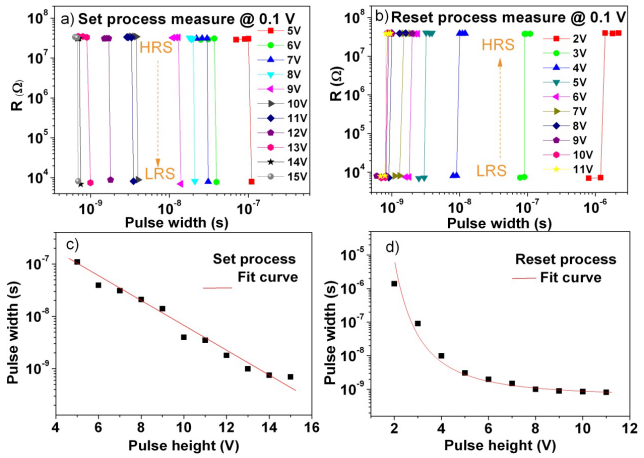

FIGURE 4. **(a) The set and (b) reset resistance as a function of pulse width for different pulse voltage; (c) pulse widths needed to trigger the set and (d) reset switching successfully. The red line indicated the measured date agree with fitting data very well.**

Compare with the DC voltage biasing mentioned in Figure 2, single voltage pulse is more desirable due to its high operation speed and low power consumption. Figure 4(a) and (b) shows the resistance switching as function of pulse width in set and reset process. The trigger of the set and reset process is successfully defined if the device resistance meets the on-off ration higher than 10^2 for different pulse amplitude. In Figure 4(a), the device could switch from HRS to LRS with different voltage pulse amplitudes. The pulse width (i.e., switching time) to trigger such switching will decrease from 1×10^{-7} s to 6×10^{-10} s when the pulse voltage increased from 5 V to 15 V. That means the set switching speed will increase when applied pulse voltage increased. A similar phenomenon could be observed in reset switching process as shown in Figure 4(b). When the pulse voltage increased from 2 V to 11 V, the pulse width will decrease from 1×10^{-6} s to 8×10^{-10} s. The reset switching time will decrease with increased applied pulse voltage as while. Figure 4(c) and (d) summarizes the pulse widths needed to successfully trigger the set and reset switching at different pulse amplitudes. It is obvious that increasing pulse amplitude results in faster switching speed. The pulse-controlled switching need higher pulse voltage and much quicker operation time compare with DC biasing ($\sim$ 25 s per loop with 0-3 V biasing range). The URS switching with high on-off ration ($\sim 10^4$) were achieved for both set and reset process with applied pulse voltage 15 V and 11 V and the pulse widths (switching time) $\sim$ 500-800 ps respectively. In this way, the Al_2O_3/nc-Al Al_xO_y bilayer based RRAM may be potential candidate for nest generation of low power and ultrafast multi-state switching memory device. To further understand the switching behavior in the set and reset process, a physical model used to describe the results of voltage-dependent switching time. An exponential dependence of the switching probability on applied voltage has been commonly observed in different experiments. Thus, the set switching time could be given as [26]:

$$t_{set} = t_0 \exp[-(V/V_0)] \tag{1}$$

where V is the voltage across the RRAM device, V_0 is related to the difficulty of CFs forming and the constant t_0 corresponds to the extrapolated characteristic time in the absence of applied voltage. As shown in Figure 4(c), the fitted curve calculated with Equation (1) well agrees with the experimental results, which shows the exponential dependence between the pulse amplitude and switching time in set process. While for the reset process, the broken of CFs is driven by the Joule Heating produced in voltage pulse applied. The reset switching time is given by [26]:

$$t_{resett} = (\varphi_0/2V_G)\exp(E_a/k_BT) \tag{2}$$

where the E_a is the activation energy of the CFs dissolution process, φ_0 is the initial size of the filament and the prefactor V_G is a diffusion parameter. In this equation, the filament temperature T could be given by:

$$T = T_0 + V_{reset}^2(R_{th}/R_{off}) \tag{3}$$

where T_0 is the ambient temperature, R_{off} is the off-state resistance and R_{th} is the equivalent thermal resistance of the filament. The fitting curve of V_{reset} and τ_{reset} is shown in Figure 4(d), which is in good agreement with measured data. According to this result, faster operation speed could be achieved if further increasing the voltage amplitude. However, the device breakdown should be avoided at the same time.

The Figure 5 exhibits the endurance and retention characteristics under ultrafast cyclic pulse switching measurement at room temperature (25 °C) and high temperature (85 °C). As shown in Figure 5(a), the voltage pulse of 15 V/600 ps for set process is used to switch device from HRS to LRS, followed by the voltage pulse of 10 V/800 ps for reset process which is used to switch device from LRS back to HRS. The operation speed is faster than normal memory device ($\sim$ ns). According to the results, the power consumption of set and reset process for single RRAM device could be as low as 26 nW and 2 μW respectively, which are quite low compared with normal electronic devices. The resistance will be measured at 0.2 V after each set and reset pulses. The HRS and LRS will keep at $\sim$ 40 MΩ and $\sim$ 6 kΩ respectively. The device showed good stability at room temperature when twenty cyclic pulses applied. At 85 °C, the measured data is more variable as more serious thermally activated process at high temperature will accelerate the generation and broken of CFs. In spite of that, the on-off ratio at high temperature could keep at $>10^3$ which is high enough in practical applications. The endurance studies with more pulses are applied at room and high temperatures are shown in Figure 5(c) and (d) respectively. The on-off ratio could keep high enough after 10^4 cycles even at high temperature. The device retention property at room and high temperatures are shown in Figure 5(e) and (f). There is no obvious data

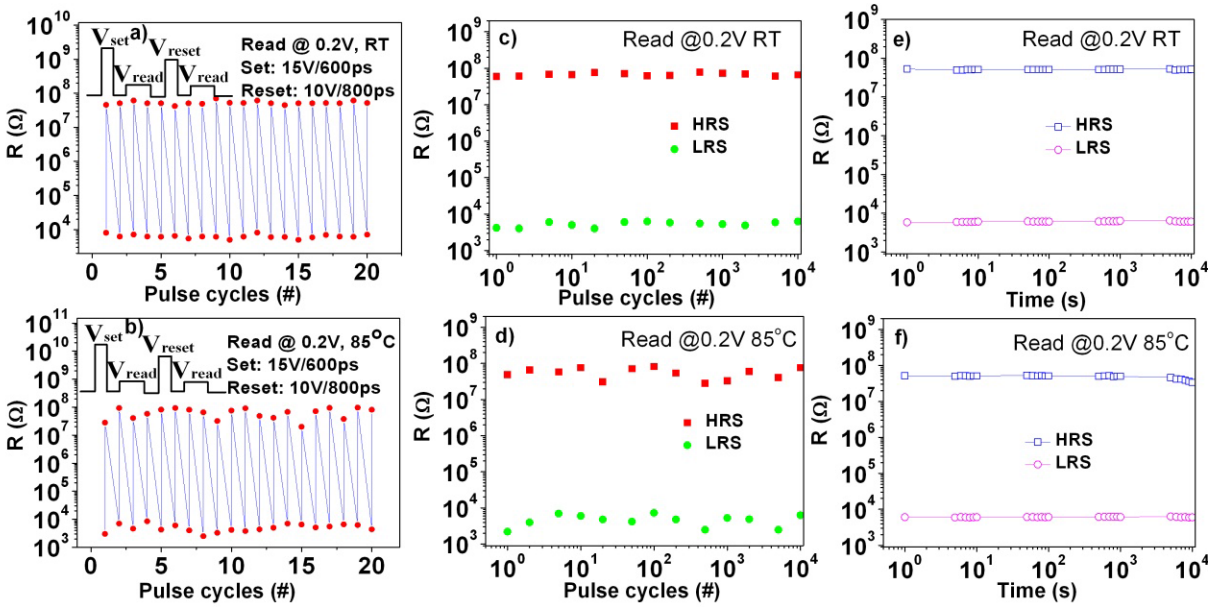

FIGURE 5. The repeatability of the set and reset operations with 15 V/600 ps and 10 V/800 ps with twenty cycles at (a) room temperature and (b) at 85 °C; the endurance properties with 10^4 cycles at (c) room temperature and (d) at 85 °C; the retention properties after 10^4 s at (e) room temperature and (f) at 85 °C.

degradation observed after 10^4 s even at 85 °C. In this way, the Al_2O_3/nc-Al Al_xO_y bilayer RRAM showed good endurance and retention characteristics to be next generation of memory device.

IV. CONCLUSION

The Al_2O_3/nc-Al Al_xO_y bilayer structure RRAM device showed multi-state by controlling its compliance current during voltage biasing. However, such multi-state also could be achieved by applying different amplitudes voltage pulses. The switching time could be as low as 600 ps to make Al_2O_3/nc-Al Al_xO_y bilayer structure RRAM device as ultrafast and low power switching device. The endurance and retention characteristics were measured at both RT and high temperature, which is quite stable and no obvious data degradation observed.

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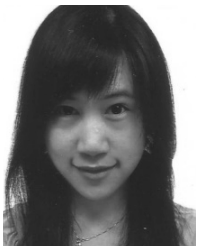

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