Time-to-Voltage Converters Based on the Time-Sharing Principle

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ABSTRACT The authors offer a new approach to the creation of linear and nonlinear pulse width modulated (PWM) signal demodulators. The proposed approach is based on the time-sharing principle in feedback and feedforward circuits. The demodulators are characterized by ease of manufacturing due to the decreased need for analog element precision. The following circuits have been designed and presented: a PWM signal demodulator performing linear conversion of a PWM signal into voltage; calculating demodulators with the function of sum of products and simple fraction; and a demodulator with a fractional rational function. All these circuits are based on the principle of continuous signal averaging by the active Miller integrator with the storing of the intermediate result in an analog memory cell. The designed demodulators are investigated during modeling and full-scale experiments. The reviewed set of demodulators can be enlarged by adding similar circuits to the proposed structures with a larger number of inputs and new functional possibilities. The proposed solutions follow the modularity principle and can be used in fully integrated implementations.

INDEX TERMS Pulse width modulation, pulse width modulation converters, digital-analog conversion, PWM-signal adders, averaging converter, continuous signal averaging, demodulator, integrator, sample and hold circuit, bit-stream.

I. INTRODUCTION

The leading trend when developing components and circuits in automation and computing is always connected with the problem of increasing equipment quality. Newly designed circuits should be more precise and faster in comparison with the existing ones, partly or completely self-adjusting, more fault-tolerant, and offer a reasonable level of complexity.

The circuits using time for data representation satisfy these criteria to the greatest extent. They use bitstream forms of data representation, i.e., flows of pulses with the unit amplitude, and in such flows, several informational parameters connected with time can be used [1].

Time-pulsed signals can be easily created and converted into different forms according to certain laws [2], [3]. The circuits processing such signals can be both digital [4], [5] and analog [6], using digital and analog approaches in some way for calculation.

The need for time-pulsed signal conversion can appear in technical systems at different stages: at the initial stage of

data collection and their representation in a form suitable for further use; at the stage of data transfer from the point of their receipt to the place of usage; or at the stage of perception and interpreting data by the final elements of controlling or regulating systems [7], [8].

At the initial stage, the problems of the time-pulsed signal conversion are solved depending on the type of sensor outputs and the method of further use of the received data, which requires specific forms of their representation. Regardless of its nature and operating principle, any sensor has specific conversion characteristics that depend on the inner structure of the item and determine the relation of the measured and output values. The form of transfer function is defined by the further practical application of measuring results.

Developers often prefer to deal with a sensor having a linear characteristic. However, the characteristic of a specific sensor is usually not ideal, and thus signal linearization may be needed. To linearize the characteristic, a special converter is used and integrated into the sensor's structure or into the interfacing circuit [9], [10]. If the data are represented in a digital form, linearization can be achieved via software. In data acquisition systems equipped with a great number

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of sensors, it is preferable to embed linearization into front-end converters. Thus, the hardware or software resources of central modules can be assigned other tasks.

Another problem can occur with measured signal preliminary processing. It may be necessary to perform nonlinear conversion of the measured value while the sensor's transfer characteristic is initially linear [11]. Such a conversion can be transferred from the processor to a special converter integrated into the sensor. Thus, the computing power of the processor is freed and can be employed to perform other work. Criteria of the converters required in this case include processing speed for the successful real-time operation and ease of implementation.

Regardless of the conversion's purpose (linearization or primary processing), it is useful to carry out processing near the sensor, thus integrating converters with the sensor [11]. Such solutions are energy-efficient.

Such signal processing "near the sensor" can be performed in different ways: in a digital form with the use of fixed-point binary codes, with the use of stochastic approaches to computing, with the use of pulsed unary processing [12], or on the base of the analog decision elements [13]. At the same time, many complex functional conversions (fractional and fractional rational) are more easily performed in analog form [14].

For complex computing problems, the most suitable approaches are software solutions using general purpose processors.

The application of circuits operating with bit-stream data is also possible in the development of neuronal structures, where bit streams can be effectively applied both at the stage of data transfer and in function implementation in network nodes. This is conditioned by the fact that the information about the functions implemented by neurons can be put only into the sequences with stable amplitude and time parameters. In technical implementation, this corresponds to pulse-frequency or pulse-time modulations, the latter of which has analog characteristics [15]–[18].

Depending on the forms of the signals being processed, converters are classified into modulators converting analog signals to PWM-form [19], [20] and demodulators performing the reverse conversion [21]. Depending on the implemented function, linear and nonlinear converters can be identified.

This paper analyzes the existing technical solutions in the field of creating PWM-signal demodulators and develops a class of linear and nonlinear demodulating averaging converters based on the time-sharing principle, which is used in analogous hardware solutions [22], [23].

In many cases, the best way to ensure stable and reliable systems in real-time work is the application of circuits based on the principle of signal averaging by time. The implementation of signal averaging by time is carried out routinely, and timewise averaging does not require extra hardware expenses and computations if bitstream forms of data representation are used in which time parameters are used as a data carrier

[24], [25]. Higher noise immunity in that case is ensured due to freeing the wanted signal of high-frequency and periodical noise.

In information-measuring systems, the task of averaging variable analog and pulsed signals is widespread. In addition to interference protection, averaging can be applied for reading data modulated in a complex signal (demodulation).

We further review the averaging structures operating with voltage-time area of a signal, although everything that follows can also be applied to circuits with current output as well as to nonelectrical devices (working on pneumatic or optic principles).

II. MATERIALS AND METHODS
A. DEMODULATION OF PWM SIGNALS

The simplest circuit performing demodulation of PWM signals is a typical passive integrating RC chain with an input switch. Its main disadvantage is the need for a large capacitor, and it leads in many cases to an unacceptably low speed of conversion. In addition, such an averaging element has a large input current that is inadmissible when processing informational signals of low power.

There are a number of active circuits for PWM signal demodulation based on the well-known principle of continuous signal averaging. These circuits use an active Miller integrator with storage of the intermediate result in the analog memory cell of the sample and hold circuit [26], [27]. The tick-by-tick result fixation method is used here. The operative cycle of the circuit consists of two ticks. During the first tick, the input and feedback signals are simultaneously integrated in the demodulator. During the second tick, the result is fixed in the S/H circuit.

As an example of a demodulator with the result fixation, let us consider the converter of a PWM signal into an analog signal [28]. The converter receives a digital pulse-width modulated signal with a pulse width τ and a period T: $\Theta = \tau/T$. At the output of the circuit, analog signal Uout is being formed. The structure and functioning chart of the converter is shown in Fig. 1.

The circuit consists of two switches SW_1 and SW_2, two resistors R_1 and R_2, a capacitor C, an amplifier and a sample and hold (S/H) circuit for analog signal storage.

We will analyze the operation of the circuit at the functional level, i.e. without regard to the nominal characteristics of the components used.

D_1 and D_2 are the logic signals synchronous with the signal Θ that control the circuit's components. ΘD_1 indicates that the signals Θ and D_1 are merged by the "AND" operation. Signal Uin is used as a reference voltage.

To be more specific, let us assume that the switches SW close in case of the logic level of "1" on their control input and are open during the other time periods. Let us also assume that sample and hold circuit (S/H circuit) switches into the sampling mode when the logical signal "1" appears on its control input. Otherwise, the S/H circuit is in the hold mode. Let us consider the assertion time of S/H circuit's output
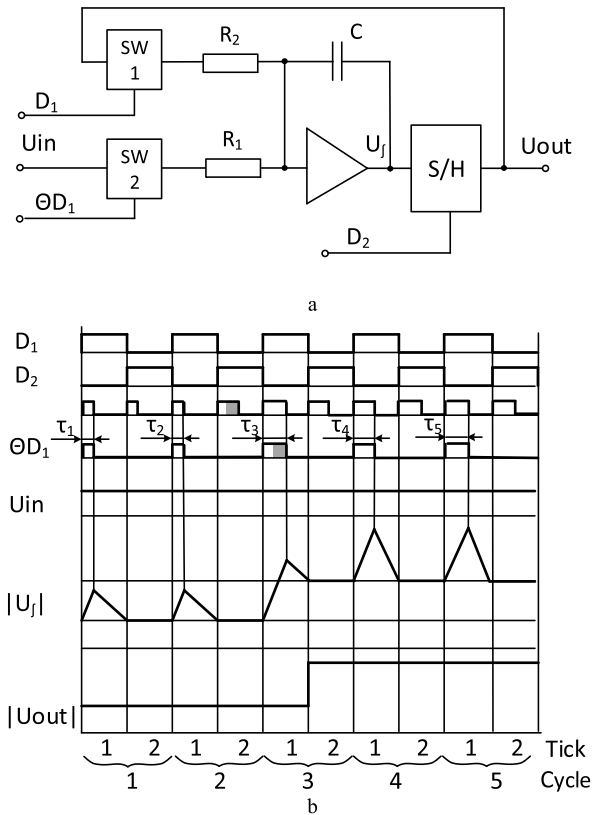
FIGURE 1. Linear Signal Multiplier: (a) Structure, (b) Functioning chart.

signal to be negligible and not show it on the chart. The signal's storage can last during the entire clock tick.

The essence of the processes taking place during the cycle number "n" can be described with the following integral expression:

$$Uout_n = Uout_{n-1} - \frac{1}{R_1 C} \int_0^{\tau_n} Uin_n dt - \frac{1}{R_2 C} \int_0^T Uout_{n-1} dt$$

where τn is the width of the PWM signal pulse in the "n" cycle;

$Uout_n$ and $Uout_{n-1}$ are the output voltages in the "n" and "n–1" operation cycles; Uin_n is the input voltage in the "n" operation cycle.

After the transients have been completed, the Uout voltage remains unchanged. Assuming that the input voltage remains the same, the following expression can be written:

$$Uout = Uout - \frac{1}{R_1 C} \int_0^{\tau_n} Uin\, dt - \frac{1}{R_2 C} \int_0^T Uout\, dt.$$

The latter expression is transformed as follows:

$$-\frac{1}{R_1 C} \int_0^{\tau_n} Uin\, dt = \frac{1}{R_2 C} \int_0^T Uout\, dt.$$

Integrating the preceding expressions gives

$$-\frac{Uin\, \tau_n}{R_1 C} = \frac{Uout\, T}{R_2 C}.$$

Therefore, the circuit in Fig. 1 eventually implements the following function.

$$Uout = -\Theta Uin \frac{R_2}{R_1} \quad (1)$$

For the circuit to function as a linear averaging multiplier, an exact equality of the resistances of the first and second integrator's resistors is necessary: $R_1 = R_2$. Naturally, it is impossible to guarantee this equality in reality, and the real error due to the difference of the resistances manifests itself in their ratio. The value of the error in the worst case is equal to the doubled resistor tolerance, and if nonprecision resistors are used, it can reach 10%.

In the worst case, the reaction time of the converter to the surge of the input action reaches two ticks, i.e., coincides with the conversion cycle duration (the change of the input signal Θ during the second tick of the second cycle is shown on the chart as a gray rectangle).

B. PRECISION INCREASE OF PWM SIGNAL DEMODULATOR

The authors suggest a fundamentally new approach, based on the time-sharing principle, to the implementation of demodulation. In the proposed PWM signal converter into the analog signal, the integration of the input signal and the feedback signal is carried out with the time-sharing and not simultaneously.

Such an approach assumes integration of the input and feedback signals during different ticks of the operation cycle of the circuit and not at the same time.

Such sharing allows for using the same integrating circuit and the single integrator input. The need for a second resistor is also eliminated. In this case, the conversion function (1) will take the following form:

$$Uout = -\Theta Uin.$$

The structure and charts of such a converter with the multiplication function are shown on Fig. 2.

PWM signal Θ with a period T enters the input of the circuit. The converter carries out a three-tick conversion of the relative width of the PWM signal Θ into the voltage with the distribution in time for the input and feedback signal accumulation processes, as well as the sampling of integrator voltage $U\int$ by the sample and hold circuit.

The logic signal levels on the inputs D_1, D_2, D_3 and the states of the switches SW_1 and SW_2, as well as of the S/H circuit for different time intervals of the single cycle, are shown in Table 1.

The converter works in the following way. At the initial time t0, the switch SW_1 is open and the S/H circuit is in the storage mode that is conditioned by the zero value of D_3. Some voltage U0 is on the output of the S/H circuit.

In the first tick during the PWM signal pulse (line 1, Table 1), the voltage Uin via the switch SW_2 passes to the input of the integrator, which accumulates the voltage and forms the output signal $U\int$. At the moment of the PWM signal

TABLE 1. Signal Levels and State of the Device Elements During a Work Period.

	Moment/ Time interval	Tick number	Θ	ΘD_1	D_2	D_3	State of the switches		State of the S/H circuit
							SW_1	SW_2	
1	t0: t0'	1	1	1	0	0	open	closed	storage
2	t0': t1	1	0	0	0	0	open	open	storage
3	t1: t2	2	1	0	1	0	closed	open	storage
4	t2: t3	3	0	0	0	1	open	open	sampling
5	t3: t3'	3	1	1	0	0	open	closed	storage
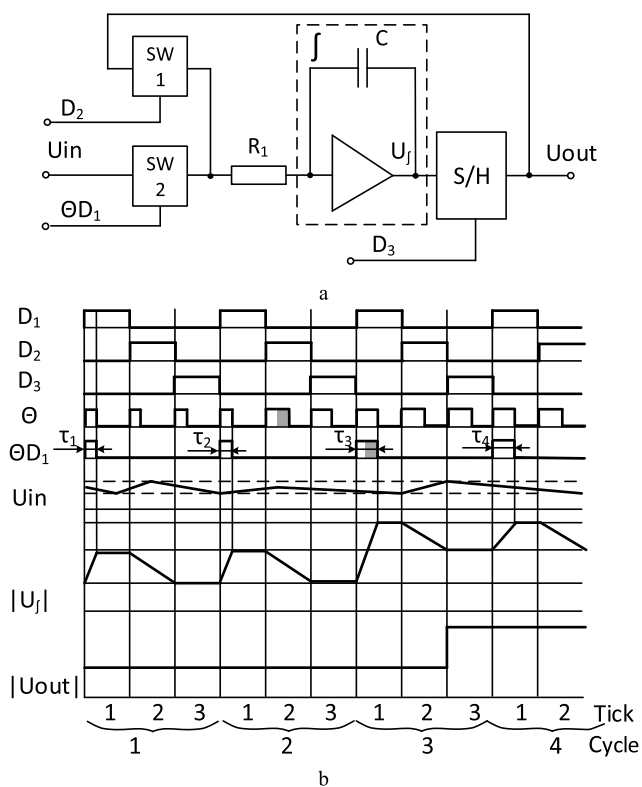
FIGURE 2. Precise Linear Signal Multiplier (a) Structure, (b) Functioning chart.

pulse termination t0', the second switch uncloses by the zero level of ΘD_1 (line 2, Table 1). Some voltage $U_{\int 1}$ is retained on the integrator's output.

In the second tick, the switch SW_1 closes under the action of the D_2 signal (line 3, Table 1), and as a result, the voltage from the output of the S/H circuit enters the input of the integrator and forms the voltage $U_{\int 2}$ on its output.

In the third tick (line 4, Table 1), the switch SW_1 is unclosed by the zero signal D_1, and the S/H circuit, controlled by the "1" signal D_3, passes into the sampling mode. At the S/H circuit output (i.e., at the output of the device) the voltage Uout equal to $U_{\int 2}$ settles.

It is obvious that every three sequential ticks of the converter will be analogous to the first, second and third ticks, respectively. Such a sequence of ticks are deemed a cycle.

Let us denominate the pulse width at the PWM signal output in the first tick of "n" cycle as τn; the pulse widths in the second and third ticks of cycles do not influence the converter's work. The voltage at the device's output in the end of "n" cycle is denoted as $Uout_n$.

The voltage at the device's output at the end of every cycle is equal to the voltage at the integrator's output in the end of the second tick of the cycle. At the integrator's output at the end of the second tick of the "n" cycle (and consequently, at the output of the device in the end of the cycle as well) we have the following:

$$Uout_n = Uout_{n-1} - \frac{1}{\tau} \int_0^{\tau_n} Uin_n dt - \frac{1}{\tau} \int_0^T Uout_{n-1} dt, \quad (2)$$

where $\tau = RC$ – time constant of the integrator, U_{n-1}– the voltage on the device's output in the previous "n–1" cycle.

The voltage Uin, fed to the integrator's input during the PWM signal pulse in the first tick of the conversion cycle, can have any form and parameter. After the integration of the signal and storing the intermediate value, its average value over the integration period, and not the voltage itself, takes part in all the following operations. In so doing, high-frequency and impulse noise is filtered out, as well as harmonic constituents of signals if their period is equal or proportional to the integration period.

As $Uout_{n-1}$ and Uin_n are constant during the cycle "n", the expression (2) can be transformed to the following view:

$$Uout_n = Uout_{n-1} - \frac{\tau_n}{\tau}\overline{Uin} - \frac{T}{\tau}Uout_{n-1}, \quad (3)$$

where $\overline{Uin}$ – averaged value of the input voltage.

For the steady mode when $\tau_n = \tau_{n-1}$, where τ_{n-1} is the pulse width in the cycle prior to the reviewed one, $Uout_{n-1} = Uout_n$. Then, expression (3) will become the following:

$$Uout_n = Uout_n - \frac{\tau_n}{\tau}\overline{Uin} - \frac{T}{\tau}Uout_n,$$

where

$$Uout_n = -\frac{\tau_n}{T}\overline{Uin} или Uout = -\Theta\overline{Uin}. \quad (4)$$

From the last expression, it can be seen that the transmission factor of the device in principle does not depend

on the integrator time constant τ, i.e., from the R and C values. Therefore, the device is distinguished with a higher conversion precision

The voltage fed to the multiplier's input is the rightful argument as well as the PWM signal. Thus, signals of different forms, the useful information of which is characterized with the average value over some period, whether its own or external as to the signal, can be processed by the same universal elements.

Moreover, both types of data (amplitude and pulse duty factor) can be contained in the same (analog) signal when using this device, and the second one (rectangular pulse) will have a controlling function and, in principle, can be received from the first signal by way of noncomplicated transformations.

As seen from Fig. 2, the conversion cycle duration and the time of reaction to the input action change is in this structure a slightly longer than in the prototype. In the worst case, i.e., the input signal hops just after the tick of its perception (the second tick of the second cycle on the chart), the result will appear at the output of the device after three ticks. However, for applications more sensitive to precision than to conversion rate, this price for the precision increase is not crucial.

It should also be noted that if $\Theta \equiv 1$, the precise averaging multiplier transforms into the precise averaging inverter.

The reviewed device implements linear conversion, but the time-sharing principle can be easily spread on devices with a nonlinear function.

The conversion time will increase in this case because of the additional operation ticks, but the use of the same elements for different calculations will minimize hardware resource expenditures and consequently increase nonlinear conversion precision at the expense of error elimination because of nonidentity of analog element characteristics.

Let us further consider the circuit modules using only the integrating circuit and the set of switches allowing commutation of different combinations of signals forming different functions.

C. PWM SIGNAL DEMODULATOR WITH THE SUM OF PRODUCTS FUNCTION

By adding new elements to the converter shown in Fig. 2 and extra ticks to the conversion cycle, it is possible to get devices implementing different functions of adder-multiplier. The example of such an implementation is shown in Fig. 3. To simplify the picture, an integrator is shown as the unity module $\int$.

The essence of the difference between this device and a multiplier lies in the fact that there are two ticks of input signal perception (integration), a tick for every set of the input voltage and PWM signal (Uin_1, Θ_1) and (Uin_2, Θ_2) instead of one tick. Accordingly, the expression for the output signal at the end of the "n" cycle can be written in

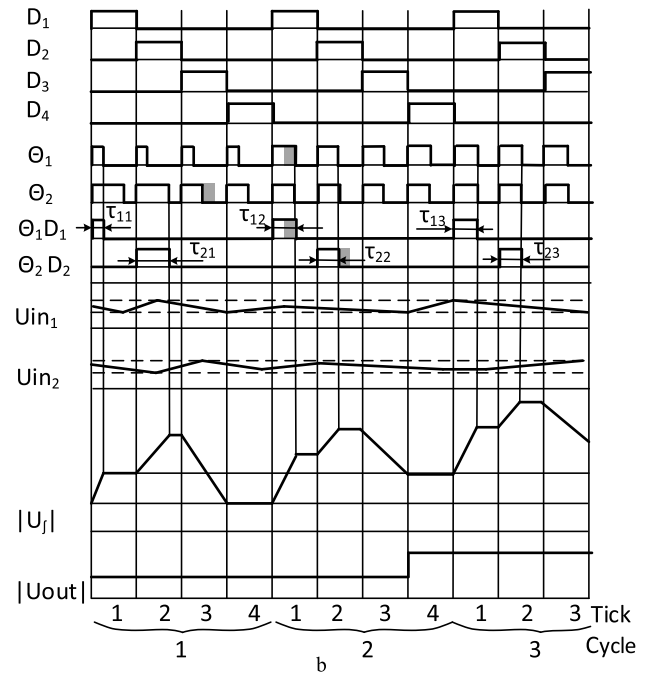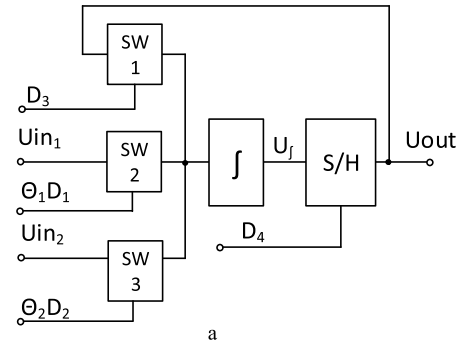**FIGURE 3.** Precise Linear Adder-Multiplier (a) Structure, (b) Functioning chart.

the following form:

$$Uout_n = Uout_{n-1} - \frac{1}{RC} \int_0^{\tau_{1n}} Uin_{1n} dt$$

$$- \frac{1}{RC} \int_0^{\tau_{2n}} Uin_{2n} dt - \frac{1}{RC} \int_0^{T} Uout_{n-1} dt.$$

After noncomplicated transformations, it is possible to obtain the following expression for the device function:

$$Uout = -(\overline{Uin_1}\Theta_1 + \overline{Uin_2}\Theta_2) \qquad (5)$$

The conversion cycle duration consists of four ticks.

D. PWM SIGNAL DEMODULATOR WITH SIMPLE FRACTION FUNCTION

The demodulator with the simple fraction function has a fundamental distinction from the previous two versions. It is based on the multiplying pulse-width demodulator described above, but here, the feedback signal, i.e., the output value
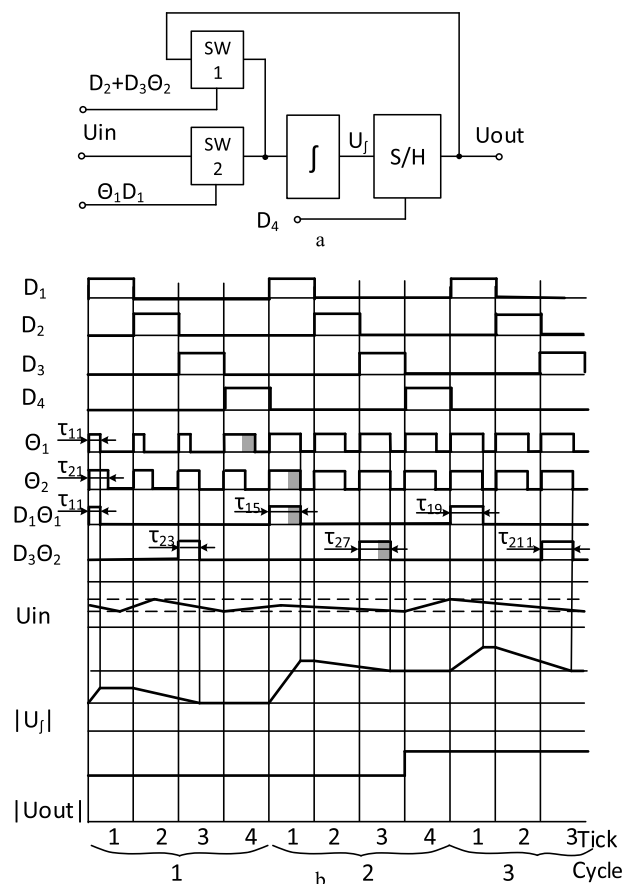
FIGURE 4. Precise Signal Divider (a) Structure, (b) Functioning chart.

of the previous tick, is integrated during the whole period T and is under the control of one of the input PWM signals for part of the period. The integral expression for $Uout_n$ can be expressed as follows:

$$Uout_n = Uout_{n-1} - \frac{1}{\tau}\int_0^{\tau_{1n}} Uin_n dt - \frac{1}{\tau}\int_0^{T+\tau_{2n}} Uout_{n-1} dt.$$

Similar to the converters already reviewed in this paper, we can obtain, by way of noncomplicated transformations, the following expression for the function of the basic unit:

$$Uout = -(\overline{Uin}\frac{\Theta_1}{1+\Theta_2}). \tag{6}$$

The conversion cycle duration in this unit consists of 4 ticks, and the time of the process reaching the steady mode (when $\tau = T$) depends on the Θ value. The generalized structure necessary for the implementation of the divider, and the timing charts of its work, are shown in Fig. 4.

E. PWM SIGNAL DEMODULATOR WITH FRACTIONAL RATIONAL FUNCTION

"Combining" all three devices discussed above will lead to a universal structure fit for the implementation of any of the three functions. The new structure is described with the
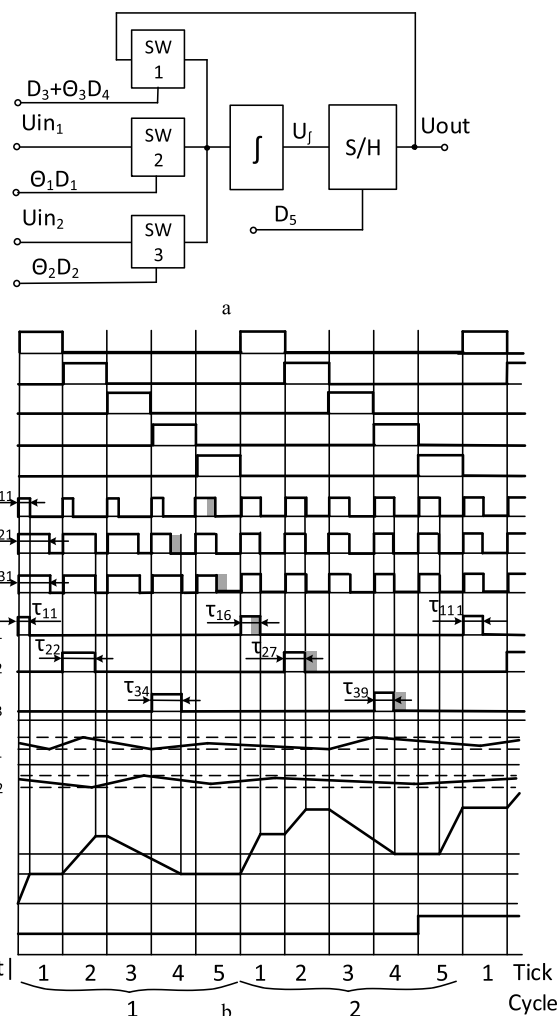

FIGURE 5. Precise Universal Signal Converter (a) Structure, (b) Functioning chart.

following integral expression for $Uout_n$:

$$Uout_n = Uout_{n-1} - \frac{1}{\tau}\int_0^{\tau_{1n}} Uin_{1n} dt$$

$$-\frac{1}{\tau}\int_0^{\tau_{2n}} Uin_{2n} dt - \frac{1}{\tau}\int_0^{T+\tau_{3n}} Uout_{n-1} dt.$$

Accordingly, the function of the basic unit can be expressed as follows:

$$Uout = -(\frac{\overline{Uin_1}\Theta_1 + \overline{Uin_2}\Theta_2}{1+\Theta_3}). \tag{7}$$

The cycle duration in the unit consists of five ticks, and the time needed for the process to reach a steady mode (when $\tau = T$) depends on the Θ value. The generalized structure necessary for the divider implementation, and its time charts, are shown in Fig. 5.

It follows from (7) that in cases of $\Theta_1 \equiv 0$ or $\Theta_2 \equiv 0$, the function of the new device becomes a simple fraction (6), and if $\Theta_3 \equiv 0$, it takes the form of the sum of products (5).
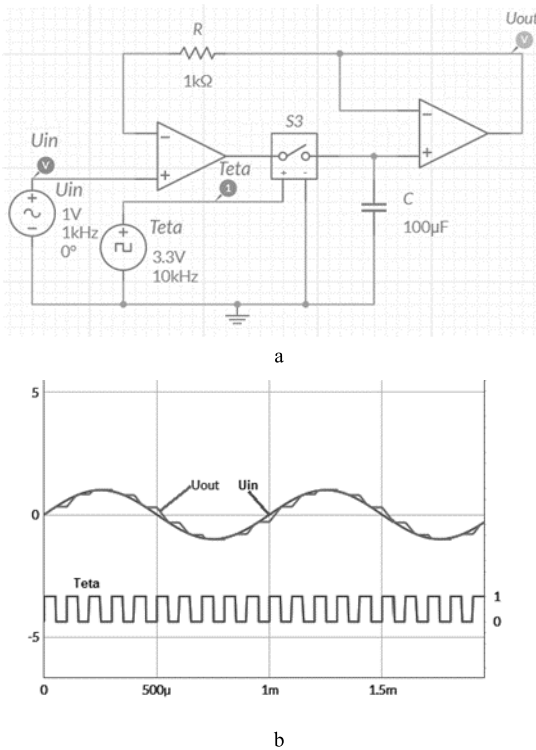
FIGURE 6. Sample and hold circuit (a) Circuit diagram, (b) Functioning timing chart.

If $\Theta_2 \equiv 0$ and $\Theta_3 \equiv 0$ at the same time (or $\Theta_1 \equiv 0$ and $\Theta_3 \equiv 0$), the implemented function coincides to the product (4).

III. RESULTS

The proposed solutions for constructing PWM signal demodulators were studied in model experiments. The experiments were carried out with the use of an online-simulator with open access Multisim Live [29], which enables the creation and study of analog and digital circuits.

One of the main elements of the reviewed devices is the sample and hold circuit. The S/H circuit used in the following experiments is shown on Fig. 6.

To emulate the input analog signal, a generator of alternating voltage Uin (Voltage VA=1V, Frequency F=1kHz) is used, and the controlling pulse-time signal Teta (Θ) is formed by a square wave generator (Voltage VP=3.3 V, Frequency F=10kHz, Duty cycle DC=52%, Rise time TR=1ns, Fall time TF=1ns).

In the sampling mode corresponding to a "1" level of the controlling pulse Θ at the output of the S/H circuit Uout follows the input voltage. When switching to the storage mode, i.e., when $\Theta = 0$, the current output voltage is fixed and stays practically unchanged. After the return to the sampling mode, the output voltage of the S/H circuit will follow the input voltage again.

The circuit diagram and the modeling results of the built converter in Fig. 1 of a PWM signal into an analog one are shown in Fig. 7.
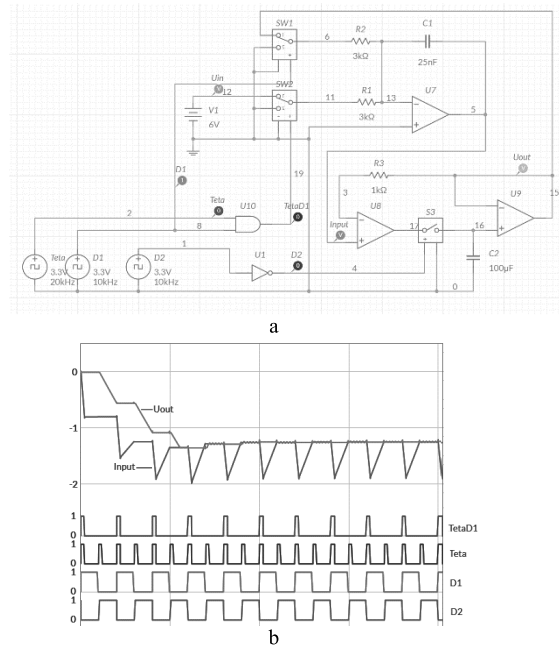

FIGURE 7. Conversion of PWM signal into analog signal (a) Circuit diagram, (b) Functioning timing chart.

In the linear signal converter, the generators D1, D2 provide the formation of controlling PWM signals, and elements U1 and U10 provide the PWM signals. The S/H circuit is built on the elements U8, U9, R3 (1 $\kappa\Omega$), C2 (100μF) and S3. The functional part of the converter corresponds to the circuit shown in Fig. 1.

In the first phase of the first cycle of the device (D1=1) during Teta=1, integration of the input voltage Uin and the signal Uout, coming through the feedback circuit, is performed. Uin and Uout are connected to integrator inputs by the switches SW1 and SW2, respectively.

After the end of the active signal D2, the voltage fixed by the S/H circuit is supplied to the input switch SW1 and takes part in a new device operation cycle.

In this manner, a gradual approximation to the result of the computational operation is performed. When the values accumulated in the integrator during one cycle along the input circuit and through the feedback loop become the same, the voltage at the output of the S/H circuit will be stored. The device in Fig. 7a has reached this state on the fourth cycle of the input signal processing, as seen in the diagram in Fig. 7b.

The circuit diagram and the modeling results of the precision linear multiplier (built according to Fig. 2) of PWM signal Teta by an analog signal are shown on Fig. 8.

The generators D1, D3 and the elements U1 to U4 provide the generation of digital control signals. The voltage source signal Uin is used as an input analog signal. The S/H circuit is built on the elements U6, R2 (1 $\kappa\Omega$), C2 (180μF), SW4 and U7. The functional part of the converter corresponds to the circuit shown in Fig. 2.

The diagram shows that each cycle of the device consists of three ticks. This is shown in detail in Fig. 8 c. In the first phase (P1) of the first tick (T1) of the device operation, when
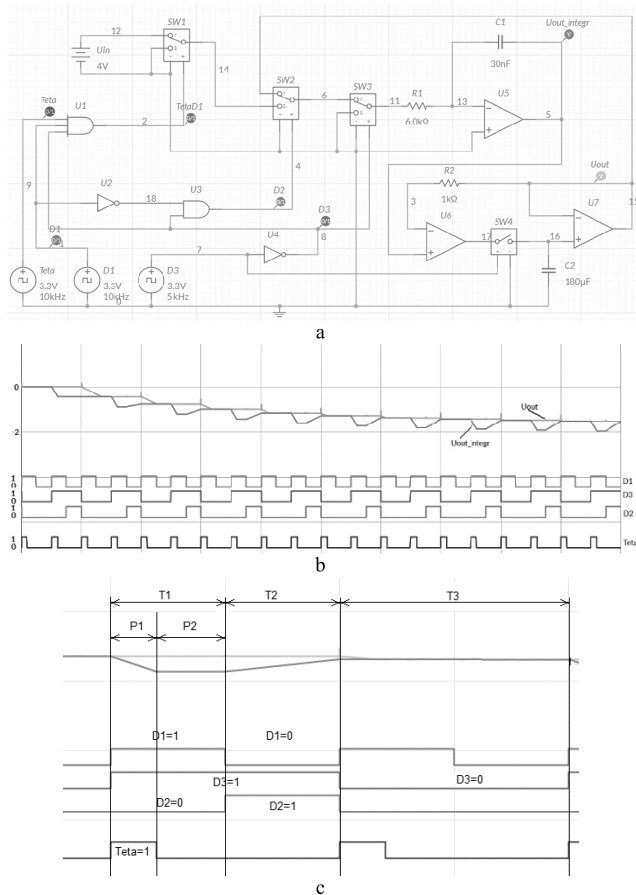
FIGURE 8. Precision Linear Signal Multiplier (a) Circuit, (b) Functioning timing chart, (c) One cycle operation of the multiplier.

D1 = 1 and D3 = 1 during signal Teta = 1, the input voltage Uin is being integrated. In the second phase (P2) of the first tick (T1) during signal Teta = 0, no changes occur in the device state. At the second tick (T2) when D2 = 1, the signal from the output of the S/H circuit is integrated. At the third tick (T3), the S/H circuit switches to tracking mode by the signal D3 = 0.

At the end of the converter operation cycle, the voltage stored in the S/H circuit comes to the input of the SW2 switch and participates in a new device operation cycle. The device gradually approaches the dynamic equilibrium mode when the output signal Uout is held in a stable state.

The reviewed circuits are placed in open access on the site https://www.multisim.com.

IV. EXPERIMENTAL RESULTS

To assess metrological characteristics of the proposed Linear Signal Multiplier and Precision Linear Signal Multiplier, a specialized laboratory model was created. The following elements are used in a model implementing circuits shown in Fig. 1 and Fig. 2: switches AD444BN, operational amplifiers AD820AN, resistors with a resistance tolerance of ±5%, and capacitors with a capacitance tolerance of ±20%.

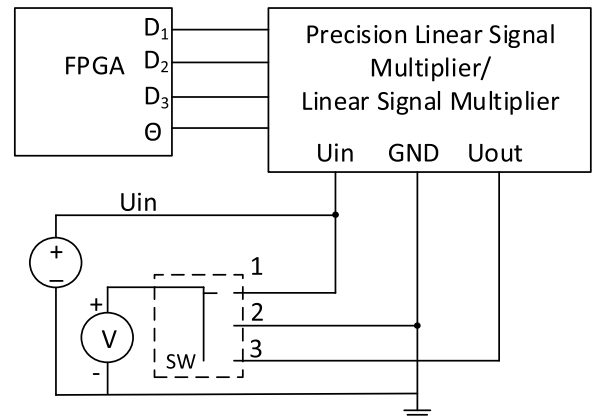The circuit diagram of the experiment is shown in Fig. 9. To minimize the measuring errors during the experiment,
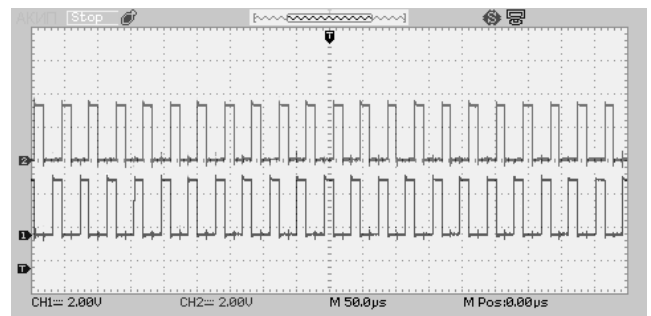

FIGURE 9. Circuit diagram of the experiment.

FIGURE 10. Input signals D_2 (CH1) and D_3 (CH2) for testing Precision Linear Signal Multiplier.

the model was placed into a measurement chamber made of magnetically soft material. The signals to be measured were connected to the voltmeter V input by way of the switch SW. During the experiment, the input and output voltages at the contacts Uin and Uout (positions 1 and 3 of the switch SW respectively) were measured, and from time to time the zero offset of the voltmeter was checked by measuring the zero voltage (position 2 of the SW switch). The model assumes the use of an external controlling device, and FPGA was applied as such a device.

A. LINEARITY CONTROL

The PWM-signal Θ values varied in a range from 0 to 1 with a step of 0.05. The error value of the device was determined by way of comparison of the measured voltage with the target value. The measurements precision was 0.01%.

We used dual-trace storage oscilloscope to control the processes in the converter. The generated input signals D_2 and D_3 as well as D_1 and Θ are illustrated in Fig.10 and Fig.11, respectively. Input signal Θ = 0.3 and output signal Uout are shown in Fig.12.

The linearity control results of the Linear Signal Multiplier and the Precise Linear Signal Multiplier at an input PWM signal frequency of 50 Hz are presented in Table 2. Here, Uout is the measured value of the output signal; Uout_c is the target value of the output signal. The error is calculated as the difference between these values.

The experiment results show that the error of the output signal of a linear precision high-speed demodulator does not

TABLE 2. The results of performance comparison of a linear signal multiplier and a precise linear signal multiplier.

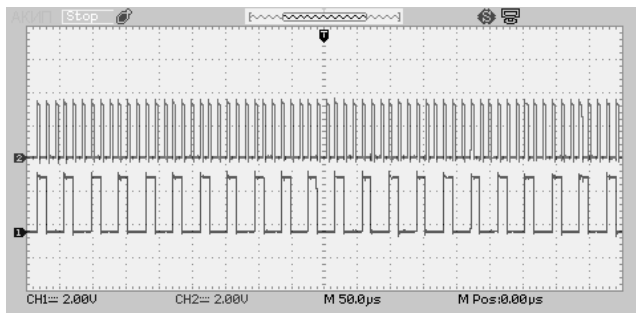| Θ	Precise Linear Signal Multiplier				Linear Signal Multiplier				
	$|Uout|$, V	$|Uout\_c|$, V	$|\Delta U|$, V	$|\delta U|$,%	$|Uout|$, V	$|Uout\_c|$, V	$|\Delta U|$, V	$|\delta U|$,%	R_2/R_1
0.00	0.0001	0.0000	0.0001	0.007	0.0001	0.0000	0.0001	0.007	–
0.05	0.0728	0.0725	0.0003	0.020	0.0745	0.0725	0.0020	0.136	1.0273
0.10	0.1453	0.1449	0.0004	0.025	0.1487	0.1450	0.0037	0.258	1.0258
0.15	0.2178	0.2174	0.0004	0.025	0.2229	0.2175	0.0054	0.373	1.0249
0.20	0.2902	0.2899	0.0003	0.023	0.2969	0.2899	0.0070	0.482	1.0241
0.25	0.3627	0.3624	0.0003	0.022	0.3710	0.3625	0.0086	0.590	1.0236
0.30	0.4352	0.4349	0.0003	0.022	0.4452	0.4349	0.0103	0.708	1.0236
0.35	0.5077	0.5073	0.0004	0.027	0.5194	0.5074	0.0120	0.827	1.0236
0.40	0.5801	0.5798	0.0003	0.020	0.5937	0.5799	0.0138	0.949	1.0237
0.45	0.6525	0.6522	0.0003	0.018	0.6676	0.6523	0.0153	1.053	1.0234
0.50	0.7250	0.7248	0.0002	0.017	0.7419	0.7249	0.0170	1.173	1.0235
0.55	0.7974	0.7973	0.0001	0.010	0.8162	0.7974	0.0188	1.295	1.0235
0.60	0.8700	0.8697	0.0003	0.022	0.8903	0.8699	0.0204	1.410	1.0235
0.65	0.9424	0.9422	0.0002	0.014	0.9645	0.9423	0.0222	1.530	1.0235
0.70	1.0148	1.0146	0.0002	0.013	1.0385	1.0148	0.0237	1.633	1.0233
0.75	1.0873	1.0871	0.0002	0.012	1.1127	1.0874	0.0254	1.749	1.0233
0.80	1.1598	1.1596	0.0002	0.012	1.1869	1.1599	0.0270	1.864	1.0233
0.85	1.2322	1.2321	0.0001	0.010	1.2613	1.2323	0.0290	1.999	1.0235
0.90	1.3047	1.3046	0.0001	0.009	1.3354	1.3048	0.0306	2.108	1.0234
0.95	1.3771	1.3770	0.0001	0.007	1.4094	1.3773	0.0321	2.216	1.0233
1.00	1.4497	1.4495	0.0002	0.014	1.4837	1.4498	0.0339	2.338	1.0234

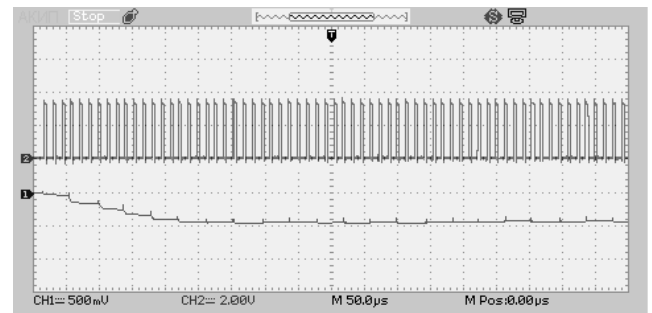**FIGURE 11.** Input signals D_1 (CH1) and Θ (CH2) for testing Precision Linear Signal Multiplier.

FIGURE 12. Input signal Θ (CH2) and output signal Uout (CH1) of Precision Linear Signal Multiplier.

exceed 0.03% compared with the target value. At the same time, the error of the linear signal multiplier implemented with the same components was above 2%. In addition, the error value depends on the Θ input parameter, i.e., its compensation is difficult. The relationship between device errors, as well as the nature of their change depending on Θ, is shown in Fig.13.

In addition, the actual relationship between resistances of R_1 and R_2 was experimentally determined. This is approximately equal to 1.024 when the resistance tolerance is 5%.

B. DEMODULATOR OPERATION TEST AT DIFFERENT FREQUENCIES

The PWM signal frequency of 50 Hz is optimal for the considered circuit, since the integration period coincides with the

period of voltage oscillations in industrial electrical networks, and so the corresponding noise is suppressed. During the study of the experimental model we tested the demodulator operation at the PWM signal frequencies of 500 Hz, 5 kHz, 50 kHz and 200 kHz.

The test results at the mentioned PWM signal frequencies are shown in Fig.14 and Fig.15, where dependencies of the circuit error on the PWM signal frequencies are displayed for a group of low and high frequencies, respectively. It is experimentally shown that the operational error increases with the increase of a frequency, and at a frequency of 200 kHz, it reaches more than one percent. This result is connected with the increase in the error fraction caused by switching processes in the structure.
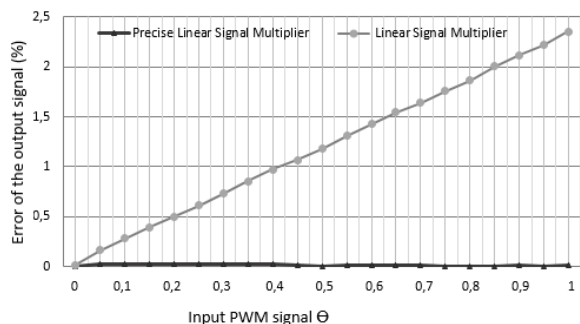
FIGURE 13. Dependence of the error of the Precise Linear Signal Multiplier and Linear Signal Multiplier on the input value at a frequency of 50 Hz.
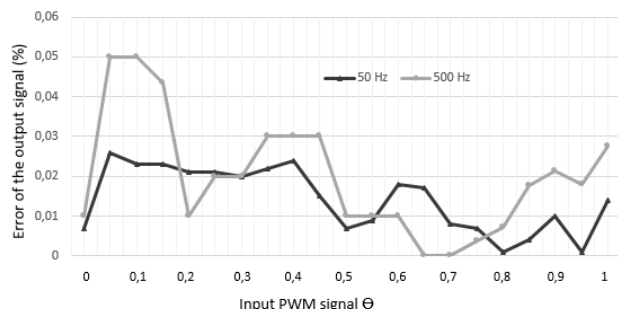

FIGURE 14. Dependence of the Precise Linear Signal Multiplier error on the input value at frequencies of 50 and 500 Hz.
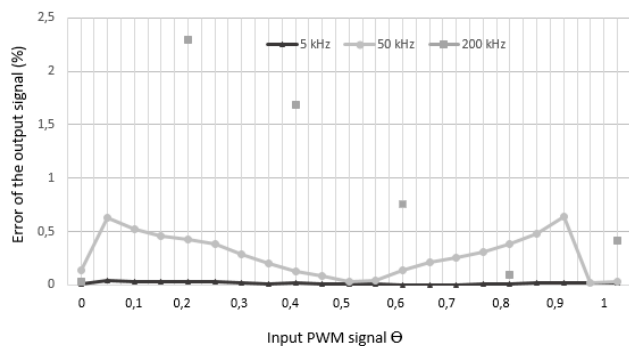

FIGURE 15. Dependence of the Precise Linear Signal Multiplier error on the input value at frequencies of 5, 50 and 200 kHz.

V. DISCUSSION

As a result of the performed studies, the following devices have been proposed: a PWM signal demodulator carrying out linear conversion of the PWM signal into voltage; computing demodulators with the functions of sum of products and simple fraction; and a demodulator with a fractional rational function.

For the work of the devices, a control pulse (D_1, D_2, D_3, D_4) distributor is necessary. The component can be included in the reviewed demodulating structures or be external. In the first case, for synchronizing the generator with the pulse-width arguments Θ, an extra external signal should be used, for example, the signal formed with the participation of one of these arguments. Naturally, all the pulse-width signals Θ are assumed to be synchronized between each other. As the

special case of identical equality of all the used PWM-signals to "1" ($\Theta \equiv 1$) is admissible, an external quantization signal is necessary for the proper functioning of the device.

Application of the external generator admits more flexible but at the same time more complicated control of the conversion cycle, and the inner generator allows the ease of demodulator usage at the expense of the rigidly set succession of the input signal processing. It is also possible to use an intelligent controller as a part of the reviewed structures and requiring preliminary programming.

As seen from the timing charts, the cycle of the result forming consists of five ticks, for there are two addends in the numerator and denominator of the function (7). In case of equality to zero of any of the addends, the need for one of the first two ticks or of the fourth tick is eliminated. This means that nothing happens with the integrator voltage during the respective tick, and so the tick may be not implemented at all. Exclusion of the unnecessary tick is possible if the converter with the external control is used, and this will promote an increase in operation speed. The more easily used option with the inner control will not allow changing the conversion cycle.

Multiplication of the signal by the integer constant can be achieved with the program method, i.e., by way of adding extra integration ticks for the same signal. If the constant has a fractional part, the latter can be entered as an addition to the whole integrating tick. While it is in some way complicated, it can be implemented by way of organizing ticks of programmable duration.

The duration of the conversion cycle and the time of data passing from the input to the output of the device coincide in the reviewed devices. For the converters, implementing more complicated functions, as a rule, consisting of two or more basic demodulators, the concept of a general cycle is inapplicable. In such devices, the data spread processes are wavelike [30]. For example, the square-low function generator composed of two serially connected demodulators-multipliers has a propagation delay of the data equal to six ticks, while the input signal sampling will be done every three ticks. Data processing in these structures will proceed via the pipeline principle: after processing of the data portion, the structure's cell will pass it further and perceive the next quantum of the input data.

The reviewed set of basic units can be enlarged by adding to the proposed structures similar devices with a larger number of inputs. In this case, for example, summing the average values of three or more input signals (regardless of their form) by the only averaging unit will become possible. Naturally, it will take place at the expense of the conversion cycle enlargement. Therefore, the developers will get the possibility to synthesize computing structures with a large number of units with the short cycle or with a smaller number of units with the enlarged cycle.

The choice between these solutions is based on the following. For the same conversion function, the informational process is shorter in case of the structure consisting of fewer more complicated units because fewer ticks are needed

for data storage into the sample and hold circuit. At the same time, the longer conversion cycle leads to slowing the device's reaction to the input action change because the coincidence probability of the moment of the change with the moment of the input data perception decreases.

The converter's speed of action depends on the time constants of integrators and an S/H circuit. It can be seen that the relation between the integrator time constant and the PWM signal period influences the rate of the device's reaching a stable mode. In addition, thermal currents of the closed switches determine the pulses amplitude at the averaging unit output.

Capacitance of the capacitor included in the S/H circuit directly affects the speed of action because the time constant of the S/H circuit determines the minimal admissible period of a PWM signal. The period should be adjusted so the transient process in the S/H circuit ends at the finish of the period. For the elementary RC chain, this time is approximately equal to 3 RC. If the transient period of the S/H circuit does not completely finish, it can negatively influence the dynamic characteristics of the device, though in general, it will not disturb its work. In selecting the capacitance of the S/H circuit capacitor, the choice should be made between high speed of action (the lesser capacitance – the lesser time constant) and high precision (the larger capacitance – the lesser pulsation amplitude at the output).

Circuit design solutions discussed in the current paper can be applied to the implementation of integrated circuits.

VI. CONCLUSION

Being constantly improved, the subclass of averaging pulse-time devices is lately approaching its limiting characteristics.

The reason for this is that the devices of this class require accurate settings of analog component nominal values. To obtain exact numbers of, for example, resistor nominal values, which is to some extent technologically difficult, at a certain stage, their improvement becomes impossible. This is especially important when implementing elements inside chips [31]. Because of this, new solutions are required, ensuring lesser dependence of calculation results on the precision of the used elements. [32].

One of the ways to solve this problem assumes the use of the same components in different measurement phases, i.e., with time sharing. In the considered circuits used to minimize conversion errors, there is no need for the use of exact combinations of nominal values of R1 and R2 (for the circuit in Fig.1) or of the only resistor R1 (Fig.2), which takes part in different computing phases.

The principle of time-sharing is in good concord with the modern technological trends offering minimizing the analog (executive) part of devices at the expense of the share enlargement of the logical (controlling) part.

We have achieved a result providing conceptual independence of the converter's functional characteristic neither on RC-components included in the device nor on

the initial conditions of the transient process. Four original solutions, having the abovementioned quality, have been proposed, where a time-sharing principle is used.

The proposed time-sharing principle in the construction of demodulators, which is connected with the use of the same elements in different time moments, is effective regardless of the technology of device implementation.

The proposed approach to converter organization, based on the time-sharing principle, enables the use of integrators containing one nonprecision resistor instead of two precision resistors. This leads to the simplified and less expensive production of electronic instruments applying these converters.

The solutions offered in the current work follow the modularity principle, which makes them fit for integral implementation as a set of programmable basic cells. Their high adaptivity and commutative abilities give the method the ability to create adjustable analog and mixed-signal architectures.

For a successful ASIC design, it is necessary to have an available library of typical elements based on these solutions, which have been worked through at the circuit level. The proposed solutions can be applied in creation of such libraries.

The proposed basic demodulators are distinguished with the high adaptivity of circuit structures to different variations of parameters, which take place in mass-scale production. In addition, the application of many modules containing memory elements gives the opportunity to create more reliable computing converters. The more S/H circuits there are in a structure, the more distributed is the system's memory, and that enhances its stability and the rate of restoration after short-time errors.

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