

Received December 11, 2019, accepted December 23, 2019, date of publication December 30, 2019, date of current version January 8, 2020.

Digital Object Identifier 10.1109/ACCESS.2019.2962869

3D Geometric Engineering of the Double Wedge-Like Electrodes for Filament-Type RRAM Device Performance Improvement

JIANXUN SUN^{1,3}, YUAN BO LI¹, YIYANG YE¹, JUN ZHANG¹, GANG YIH CHONG²,
JUAN BOON TAN³, ZHEN LIU⁴, AND TUPEI CHEN¹

¹School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

²Nanyang NanoFabrication Centre (N2FC), Nanyang Technological University, Singapore 639798

³GLOBALFOUNDRIES Singapore Pte Ltd., Singapore 738406

⁴School of Materials and Energy, Guangdong University of Technology, Guangzhou 510006, China

Corresponding author: Tupei Chen (echentp@ntu.edu.sg)

This work was supported in part by the National Research Foundation of Singapore Program under Grant NRF-CRP13-2014-02, in part by the EDB-IPP Program under Grant RCA-16/335, and in part by the Science and Technology Program of Guangdong Province of China under Grant 2016A050502058.

ABSTRACT The resistive switching variability and reliability degradation are the two major challenges that hinder the high-volume production of the Resistive Random Access Memory (RRAM) devices. In this work, a 3D electrode structure engineering method is proposed. The geometric parameters defined as electrode angle (EA), electrodes spacing (ES) and electrode trench depth (ETD) associated with the double wedge-like electrodes of the filament-type RRAM devices are studied for the first time. Our experimental results show that apart from the resistive switching uniformity, the reliability performance such as cycling endurance and data retention are significantly improved for the device with small EA (90°), narrow ES (440 nm) and deep ETD (90 nm) owing to the electric field confinement and enhancement. Thus, this new approach can be served as a guideline for the design and optimization of the filament-type RRAM devices.

INDEX TERMS Electrode structure engineering, resistive switching uniformity, RRAM device reliability.

I. INTRODUCTION

The fourth fundamental two-terminal circuit element named memristor has been found by Hewlett Packard labs more than one decade ago [1]. Up to now, a wide range of applications such as non-volatile memory [2], in-memory computing [3], artificial neural network [4], [5], and chaotic system [6] have been demonstrated by using memristor. Resistive Random Access Memory (RRAM) as one type of memristor has drawn much attention due to its fast read/write speed, low power consumption, simple metal-insulator-metal (MIM) device structure, and Complementary Metal Oxide Semiconductor (CMOS) compatibility [7]–[9]. However, the resistive switching variability which is caused by the inherently stochastic nature of the defects generation and migration [10] seems to be the fundamental issue of the RRAM devices despite various techniques [11]–[20] have been implemented. Among which the electrode structure engineering through the

Reactive Ion Etching (RIE) process can be widely adopted by the CMOS foundries to enhance the performance of the filament-type RRAM devices [15], [16]. The electrode structure induced filaments confinement provides good filament control [15] without embedding additional materials into the RRAM stacks [11], [12] and scales the effective switching area to several nanometers in diameter [16] without using the expensive lithography process. To date, prior works [14]–[20] have shown improvement by engineering the structure of a single electrode. The filaments confinement can only be achieved near the engineered electrode. Devices with both structurally modified electrodes have not been demonstrated. Therefore, the effects of the variation of the electrode geometric parameters on device performance have not been investigated as well. Furthermore, the filaments confinement which has been mostly explained by the models and simulation results has yet to be proven by the microscopic images.

The Ag-based RRAM devices with planar double wedge-like electrodes were designed and fabricated in this work. The combination of one flat electrode with one wedge-like

The associate editor coordinating the review of this manuscript and approving it for publication was Sun Junwei¹.

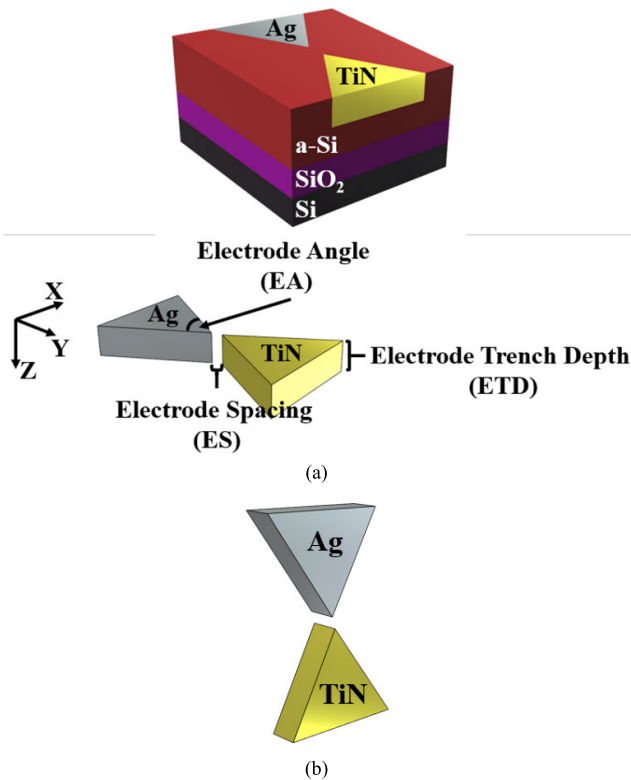


FIGURE 1. (a) 3D schematics of the fabricated RRAM device and the planar double wedge-like electrodes with three geometric parameters. (b) 3D schematic of the vertical double wedge-like electrodes.

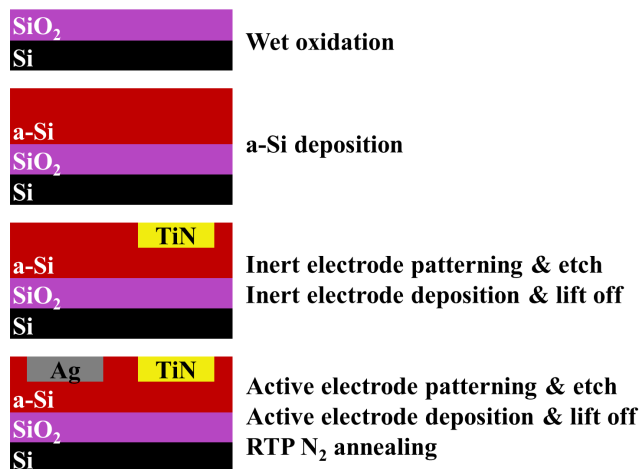


FIGURE 2. Schematics of the cross-sectional view of the device after each fabrication process.

electrode was not studied here as many research works have been done with similar comparison and the conclusions have been consistent with better performance being achieved using non-flat type electrodes. Thus, the engineering of the electrode geometric parameters of both electrodes was the key focus in this article. The 3D schematics of the fabricated device and the planar double wedge-like electrodes with three geometric parameters are shown in Fig. 1(a). Electrode angle (EA) is defined as the vertex angle of the isosceles

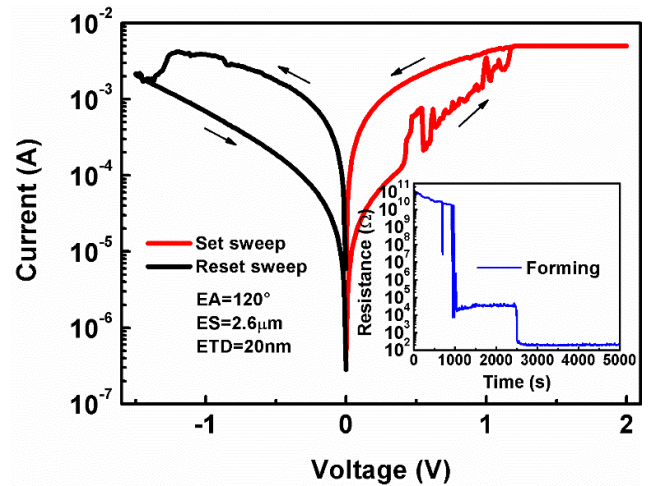


FIGURE 3. Bipolar *I-V* characteristics of the Ag/a-Si/TiN device after the forming process. The inset shows the constant voltage forming process.

triangle within the XY plane, and it can be varied by changing the photomask patterns (isosceles triangles) with different vertex angles. Electrodes spacing (ES) in the Y direction is the minimum distance between two wedge-like electrodes, which can be adjusted by fine-tuning the photolithography alignment process. Electrode trench depth (ETD) is equivalent to the thickness of the electrode along the Z direction and it can be modified by changing the duration of the etch process. The improvement of the device performance including resistive switching uniformity, cycling endurance, and data retention was achieved by appropriate engineering of the above electrode geometric parameters. It is noteworthy that both wedge-like electrodes are placed side by side with the tip to tip orientation for the ease of device fabrication and Ag filaments observation [21], [22] as compared to the vertical one which is shown in Fig. 1(b). The main objective of this work is to demonstrate and validate the feasibility of the proposed 3D electrode structure engineering method by comparing the performance of devices with different sets of electrode geometric parameters. The data presented here serve as important references for the future development of the filament type RRAM device with vertical configuration for high-density memory application.

II. EXPERIMENT

The Ag/a-Si/TiN RRAM device was fabricated with the following process steps. First, a 550 nm SiO₂ isolation layer was grown on the silicon substrate by the wet oxidation process. Then, a 300 nm a-Si layer which served as the solid electrolyte was deposited by the Plasma Enhanced Chemical Vapor Deposition (PECVD) at 300 °C. The inert electrode pattern was transferred to the sample through the i-line UV photolithography process followed by the Reactive Ion Etch (RIE) with Cl₂ gas. The inert electrode trench was filled by TiN during DC magnetron sputtering of Ti target in the N₂ environment. The subsequent lift-off process ensured only the defined electrode area was covered by TiN. Similar

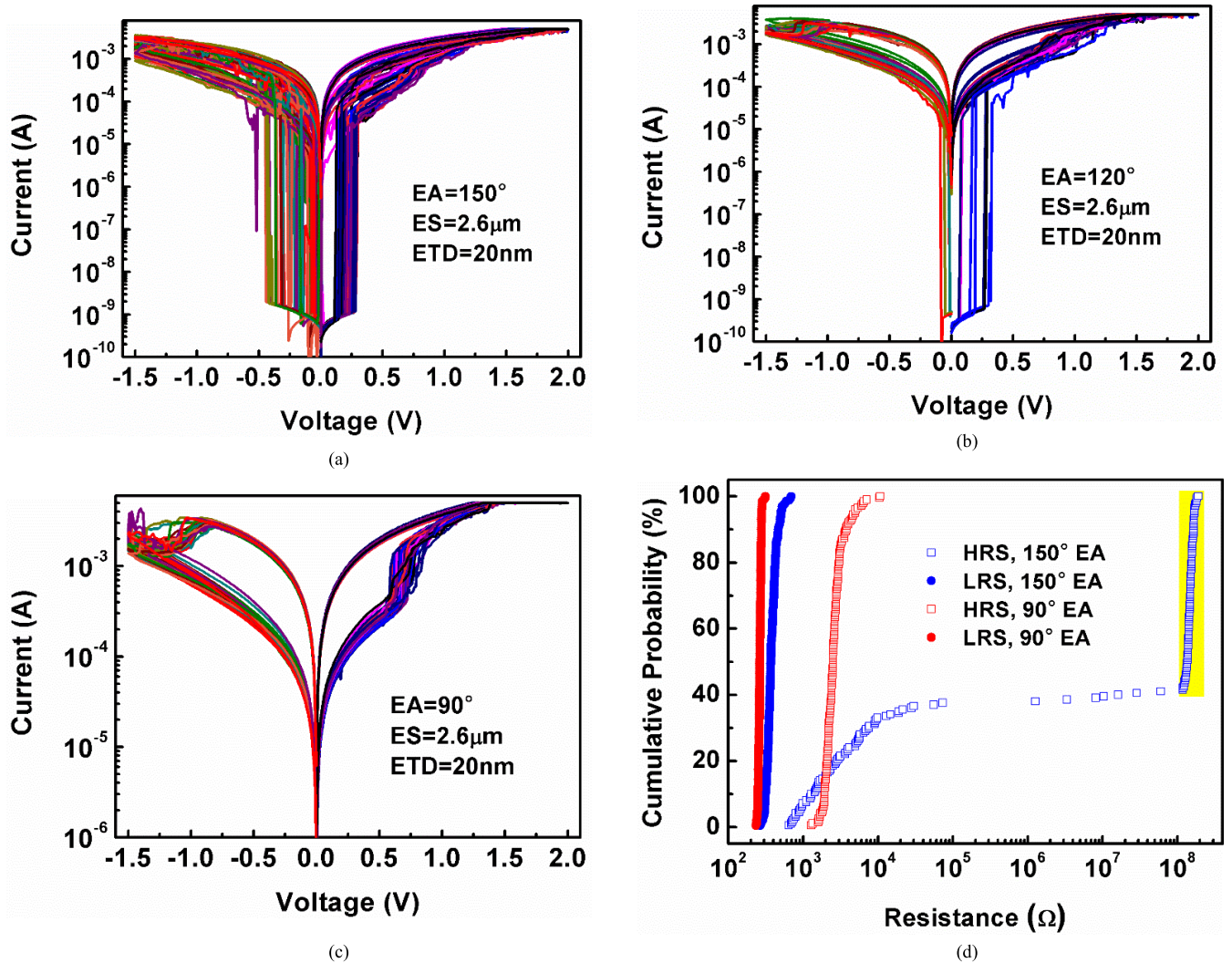


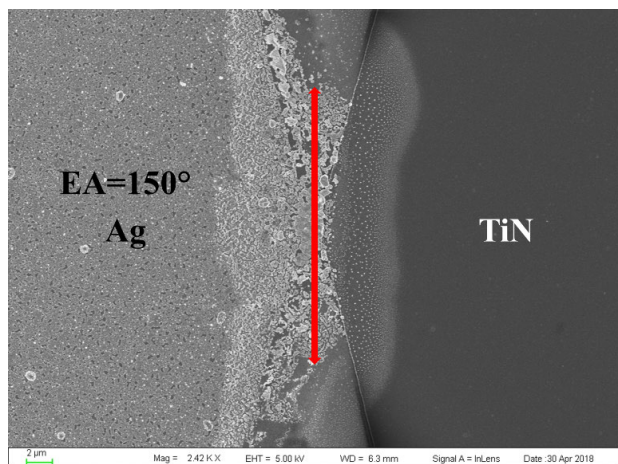
FIGURE 4. (a)-(c) 50 DC sweep cycles of *I-V* characteristics of devices with 150°, 120°, and 90° EA respectively. (d) The statistical distribution of resistances in HRS and LRS for 200 DC sweep cycles for devices with different EAs.

lithography, RIE and lift-off processes were used to pattern the Ag active electrode. The electron beam evaporation was used to deposit Ag due to lower deposition rate as compared to that of the sputtering process. A good Ag to a-Si adhesion can be achieved with the low deposition rate. At last, the device was N_2 annealed by the Rapid Thermal Processing (RTP) at 400 °C for 600 s. The schematics of the cross-sectional view of the device fabrication processes are shown in Fig. 2. All electrical tests were conducted by using the Keithley 4200 semiconductor characterization system. The double wedge-like electrodes and the distribution of the Ag filaments were observed by the Scanning Electron Microscopy (SEM).

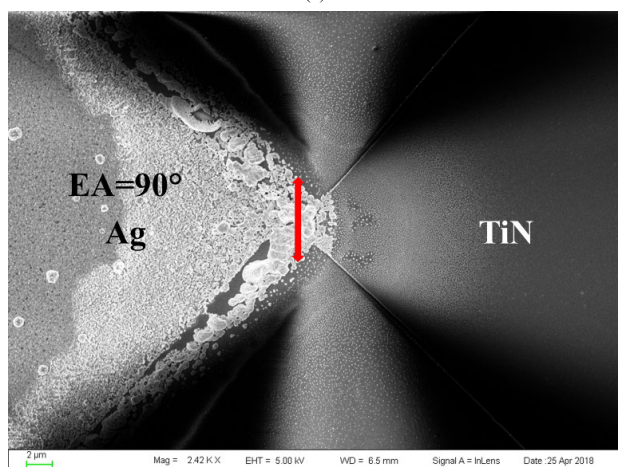
III. RESULTS AND DISCUSSION

Research on the electrode geometric parameters was systematically carried out. First, EA parameter was examined. A total of five EAs namely 150°, 120°, 90°, 60°, and 30° were designed. With fixed ETD (20 nm) and photomask pattern

defined ES (2 μm), the actual ES measured by the SEM for different EAs (not shown here) indicated that the devices with EAs less than 90° suffered from serious electrode corner shrinkage issue due to pattern dependent optical proximity effects [23]. In other words, ES gets larger for smaller EA. To exclude the ES variation, only the EAs of 150°, 120°, and 90° with almost the same ES (2.6 μm) were used in this experiment. As the device dimensions are limited by the resolution of the i-line UV mask aligner, the advance lithography techniques are required for future study of the effects of the small EAs (<90°). The inset of Fig. 3 shows the forming process, which was conducted on the device with 120° EA by applying a small constant voltage (1 V) to the Ag anode for 5000 s while the TiN cathode was grounded. The cell resistance decreased from the initial high resistance ($\sim 10^{11}$ Ω) to the final low resistance (~ 200 Ω) with a stepwise profile owing to the gradual growth of the Ag filaments [24]. The saturation of resistance after 2500 s indicated the cease of filament growth, which was attributed to the reduction of the



(a)



(b)

FIGURE 5. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 150° EA; and (b) device with 90° EA.

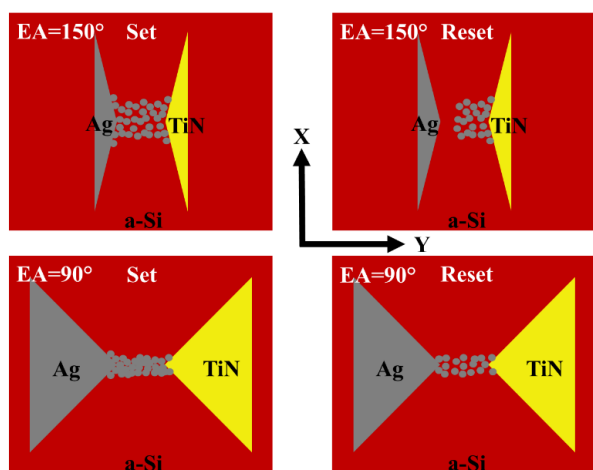


FIGURE 6. Proposed resistive switching models for devices (top view) with different EAs.

voltage drop across the solid electrolyte. As shown in Fig. 3, typical bipolar resistive switching behaviour was observed with the set process (the increase of conductance) occurred in the positive DC sweep (0 V → 2 V) and reset process (the

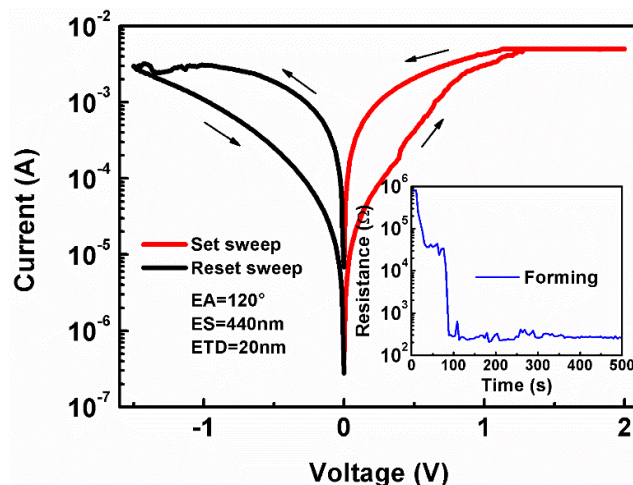


FIGURE 7. Bipolar *I-V* characteristics of the Ag/a-Si/TiN device after the forming process. The inset shows the constant voltage forming process.

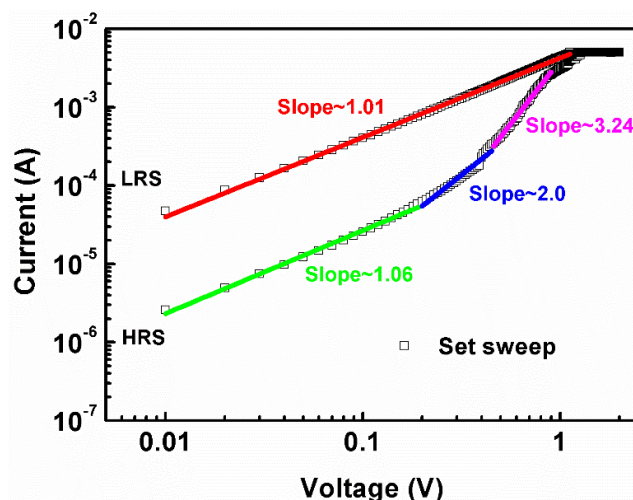


FIGURE 8. Logarithmic *I-V* plot of the Ag/a-Si/TiN device. The linear fittings show good agreement with space-charge-limited current (SCLC) conduction mechanism.

decrease of conductance) occurred in the negative DC sweep (0 V → -1.5 V). The formation and dissolution of the Ag filaments were responsible for the resistive switching from high resistance state (HRS) to low resistance state (LRS) and vice versa, respectively [25]. The resistance window (the ratio of HRS resistance to LRS resistance) read at 0.1 V was about 13 which fulfilled the requirement for practical applications. The same test conditions of forming, set, and reset were used to characterize the other devices with different electrode parameters. 200 consecutive DC sweep cycles were conducted on the aforementioned three devices immediately after the forming process to study the resistive switching uniformity. An obvious trend towards stable resistive switching was noticed by comparing the 50 cycles of the *I-V* characteristics of devices with different EAs as shown in Fig. 4(a)-(c). The instability of the resistive switching which was described as the abrupt current drop during the

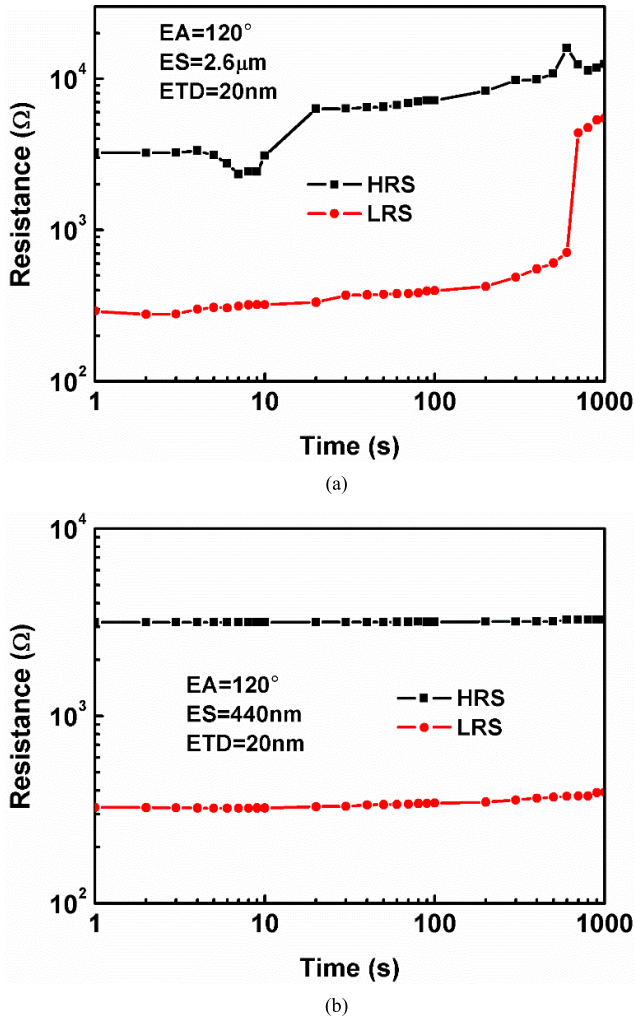


FIGURE 9. Data retention tests performed at room temperature for 1000 s: (a) device with 2.6 μm ES; and (b) device with 440 nm ES.

reset process was significantly reduced through shrinkage of the EAs. Since the event of the abrupt reset was random, the cumulative probability versus resistance plot was used to illustrate the changes. For striking comparison, only the worse and the best data are shown in Fig. 4(d). For the device with 150° EA, the extremely high resistances ($>10^8 \Omega$) which were caused by the abrupt reset were highlighted by yellow. The percentage was calculated to be 59% whereas the occurrence probability of the extremely high resistances was 0% for the device with 90° EA (the average value of the HRS resistances was $\sim 2.8 \text{ K}\Omega$). It was assumed that different EAs led to different resistive switching mechanisms. To verify the assumption, SEM was used to directly observe the distribution of the filaments. Interestingly, a clear tendency of narrowing of the Ag filaments distribution along the X direction was captured right after the cycling operation for the above three devices. As shown in Fig. 5, with the same magnification (x2420), the distribution of the Ag filaments (indicated by the red bidirectional arrow) in the device with 150° EA was much broader than that of the device with 90° EA, which implied that smaller EA could provide better

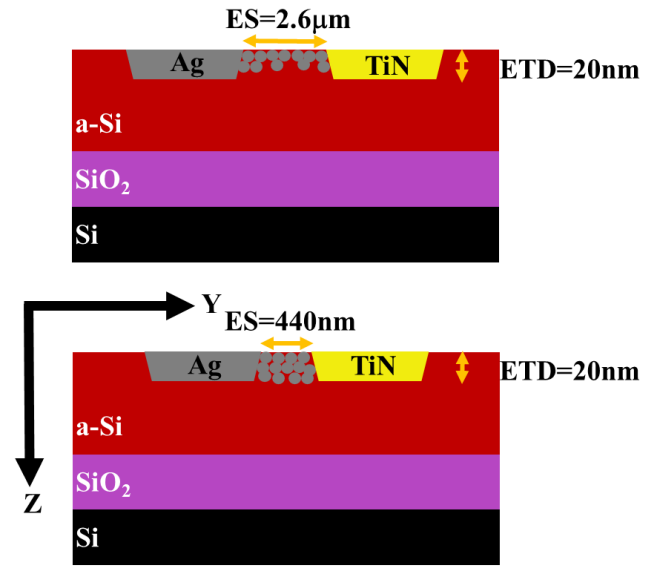


FIGURE 10. Proposed model for the formation of stable filaments in the device (cross-sectional view) with shorter ES.

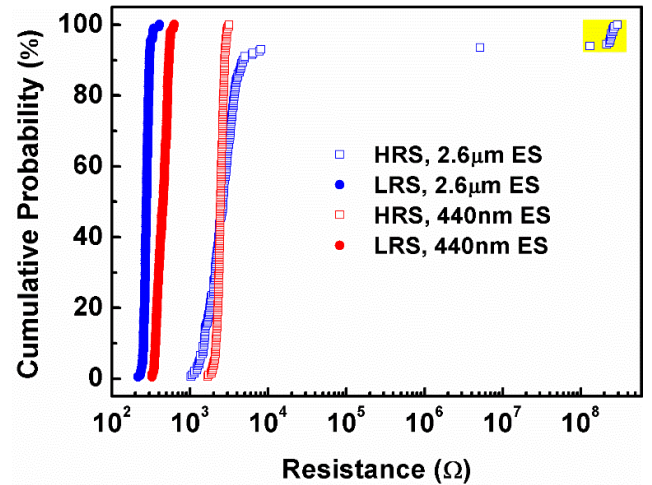
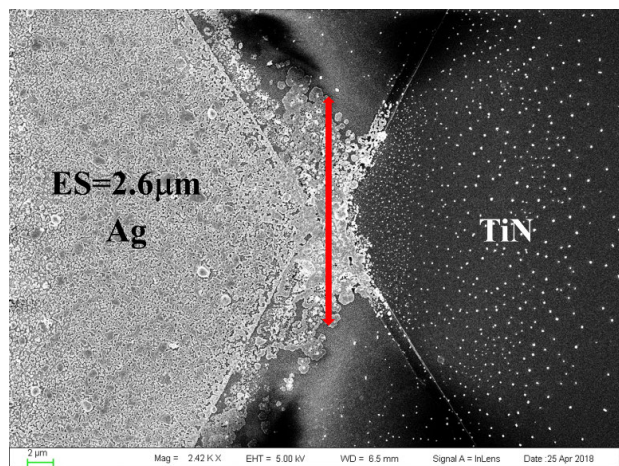
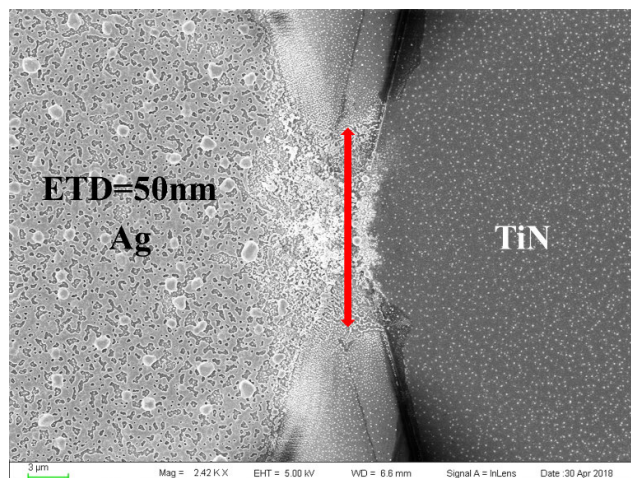


FIGURE 11. The statistical distribution of resistances in HRS and LRS for 200 DC sweep cycles for devices with different ESs.

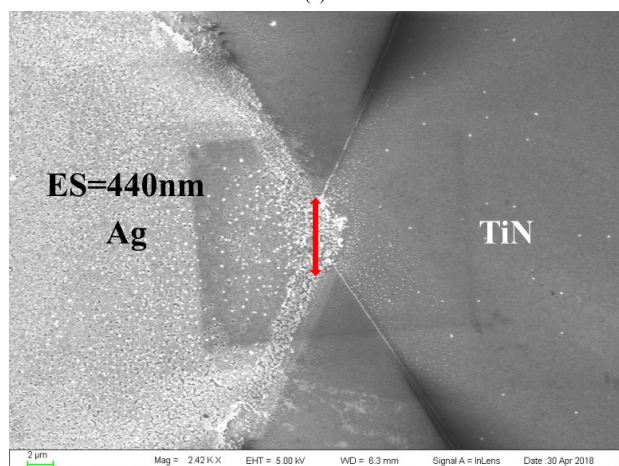
filaments confinement, thus better filaments control and switching uniformity. To theoretically explain the phenomenon, we referred to the electric field simulation works done by other groups [15], [16], the strongest electric field along the Y direction should be allocated at the tip region of the double wedge-like electrodes and the electric field strength gradually get weakened in the surrounding area according to the contour of the electrode. It is clear that the decreasing rate of the electric field strength is inversely proportional to the EA. For a given voltage bias, the coverage of the electric field which could drive the Ag ions was much smaller in the device with a smaller EA. Therefore, electric field confinement could be achieved by reducing the EA. At the meantime, a smaller EA associated with a smaller electrode tip radius also gave rise to the enhancement of electric field [26]. To explain the huge difference between



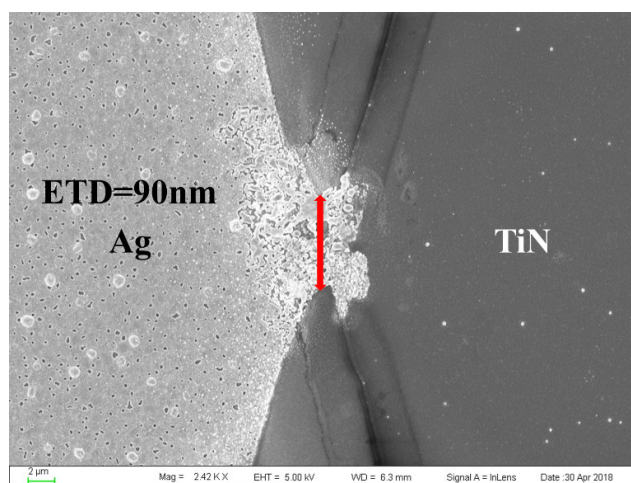
(a)



(a)



(b)



(b)

FIGURE 12. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 2.6 µm ES; and (b) device with 440 nm ES.

FIGURE 14. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 50 nm ETD; and (b) device with 90 nm ETD.

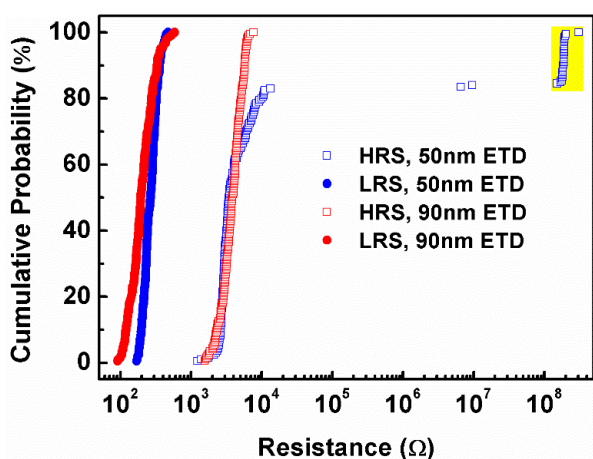


FIGURE 13. The statistical distribution of resistances in HRS and LRS for 200 DC sweep cycles for devices with different ETDs.

the R_{HRS} of the two devices, two resistive switching models as shown in Fig. 6 were proposed. For the device with 150° EA, multiple filaments with low Ag atom density were formed after the set process due to distributed and weak

electric field. Rupture of the filaments was more likely to be the resistive switching mechanism during the reset process. However, the filaments formed in the device with 90° EA were concentrated and dense owing to the confined and strong electric field. The increasing of the Ag atom concentration in the filaments should be the resistive switching mechanism for the set process, and vice versa for the reset process. We also studied the effect of EA variation on device reliability such as data retention due to instability of the Ag filaments [27]. The same set of devices was tested at room temperature with the application of 0.1 V read voltage for 1000 s. However, the effect of EA variation on data retention was insignificant based on the test results (not shown here). A plausible explanation was given in the following section.

Next, the ES parameter was investigated. A 440 nm ES was obtained by fine-tuning the UV lithography alignment process. Both EA and ETD were fixed at 120° and 20 nm, respectively. The forming process was found to be much faster in the device with shorter ES. As shown in the inset of Fig. 7, the forming process took about 100 s to change

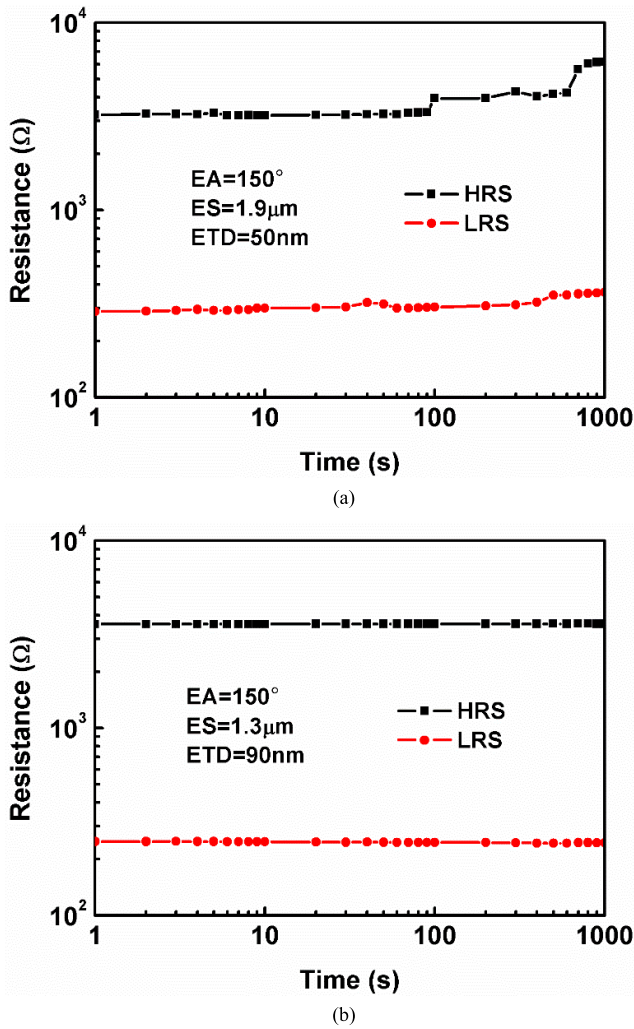


FIGURE 15. Data retention tests performed at room temperature for 1000 s: (a) device with 50 nm ETD; and (b) device with 90 nm ETD.

the device's resistance from the initial state of ~ 800 K Ω to the LRS of ~ 300 Ω . The acceleration of the forming process was caused by the shortening of the Ag migration path and the enhancement of the electric field. Furthermore, the set sweep (0 V \rightarrow 2 V \rightarrow 0 V) current-voltage curve as shown in Fig. 7 was smoother than that of Fig. 3, which indicated the formation of more stable Ag filaments. To investigate the current conduction mechanism, the set sweep current-voltage curve was replotted in log-log scale with linear fittings as shown in Fig. 8. Ohmic conduction with the slope of ~ 1 was demonstrated in the LRS curve. However, the HRS curve was divided into three different segments. In the low-voltage region, Ohmic transport with the slope of ~ 1 was observed whereas the slope increased to ~ 2 and further rose up to ~ 3 in the high-voltage region, which showed good agreements with space-charge-limited current (SCLC) conduction mechanism [28]. The stability of the Ag filaments was further verified by the data retention tests as shown in Fig. 9. As compared to the device with 440 nm ES, both HRS and LRS resistances of the device with 2.6 μm ES were increasing, which

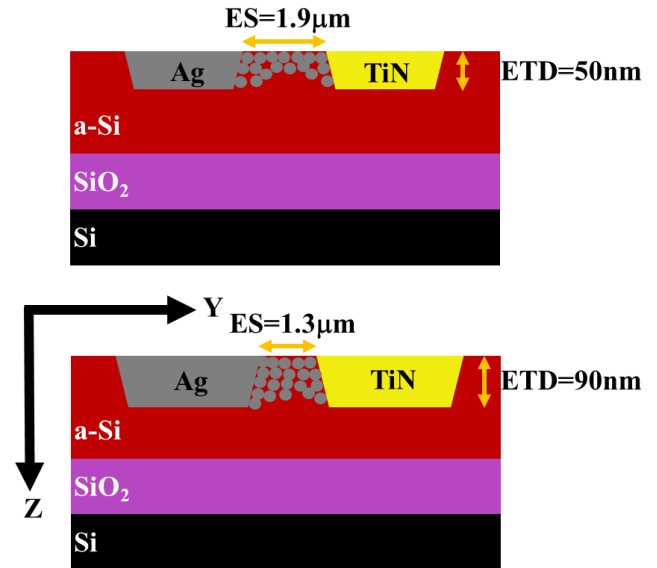
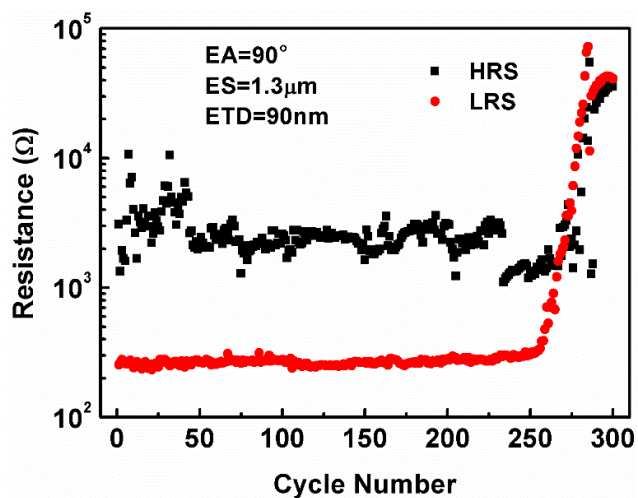
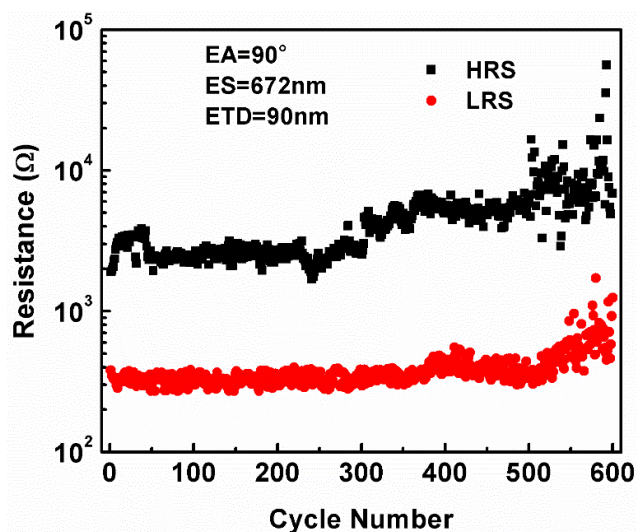


FIGURE 16. Proposed model for the formation of stable filaments in the device (cross-sectional view) with deeper ETD.

led to the shrinkage of the resistance window from ~ 11 to ~ 2 . The drifting of the resistances suggested the dissolution of the Ag filaments and the dissolution rate was highly dependent on the width of the filaments [29]. To acquire better data retention, wider filaments width was required. For this case (planar device), the length of the filament was along the Y direction and the width of the filament was along the Z direction. A model as shown in Fig. 10 was proposed to illustrate the improvement of data retention. It was worth noting that the actual angle formed between the trench base and the trench sidewall was not 90° due to the lateral etching effect. The electric field became weak as it went deep along the Z direction because of the slanted sidewall profile. Since the stronger electric field was induced in device with narrower ES, Ag atoms located below the electrode surface could participate in the process of filaments formation, which resulted in filaments with the wider diameter. In the previous section, although the electric field was enhanced by reducing the EA, the electric field strength might not be sufficient to drive the Ag atoms beneath the surface as the bulk migration was more resistive than the surface migration. It is speculated that the small EAs ($<90^\circ$) could further improve both the switching uniformity and data retention. Similarly, the resistive switching uniformity test was carried out for the two devices. As shown in Fig. 11, the occurrence probability of the extremely high resistances was reduced from 6.5% to 0% by narrowing the ES from 2.6 μm to 440 nm. Once again, the improved resistive switching uniformity was attributed to the confined distribution of the Ag filaments as shown in Fig. 12. The relatively dark rectangle appeared in Fig. 12(b) was caused by the enhanced electron charging effect during the focus tuning process within a small rectangular area which was defined by the SEM user, and the distribution of the filaments was not affected by the electron irradiation. The rapid formation of the Ag filaments in the centre of the



(a)

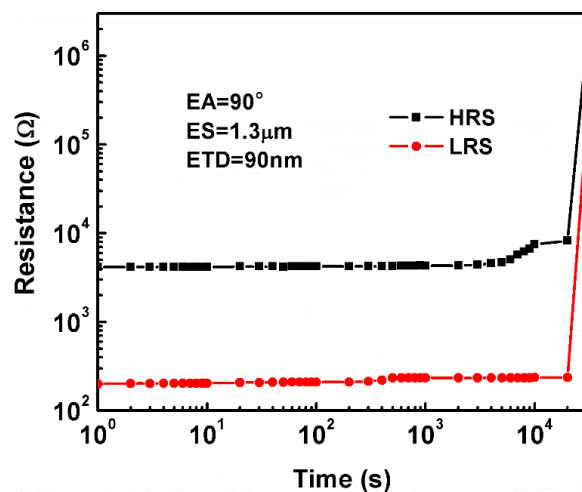


(b)

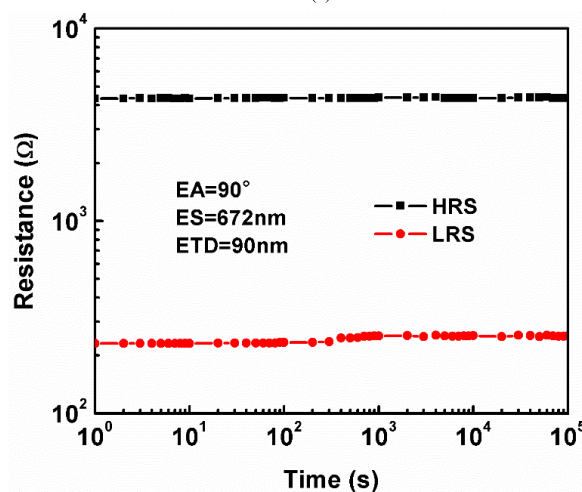
FIGURE 17. Endurance tests performed with more than 200 consecutive DC sweep cycles: (a) device with 1.3 μm ES; and (b) device with 672 nm ES.

device with short ES eliminated the growth of the surrounding filaments due to reduction of the voltage drop across the solid electrolyte. The reliability data of the submicron-scale device with Ag electrode and a-Si solid electrolyte [30], [31] were demonstrated. However, the device performance was limited by the ES, which was limited by the resolution of the i-line UV mask aligner. Based on the promising data shown by other references in [32]–[34], the vertical cell configuration could provide an easy way to achieve nanometer-scale ES with better results.

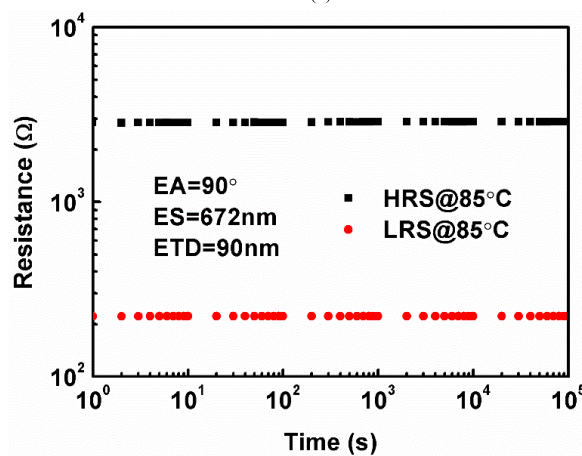
Finally, the ETD parameter was studied. A total of three ETDs of 20 nm, 50 nm, and 90 nm were attained through tuning of the a-Si RIE etching time. As lateral etching was inevitable, the ES parameter also played a part in the course of ETD engineering. SEM measurements (not shown here) indicated that ES decreased from 2.6 μm to 1.9 μm and then 1.3 μm with increasing ETD from 20 nm to 50 nm and then 90 nm, respectively. EA was fixed at 150°. A trend towards



(a)



(b)



(c)

FIGURE 18. Data retention tests performed at room temperature for more than 1000 s: (a) device with 1.3 μm ES; and (b) device with 672 nm ES. (c) For the device with 672nm ES, further data retention test was conducted at elevated temperature for 10⁵ s.

better resistive switching uniformity and data retention was observed. To avoid showing duplication, data collected from the device with 20 nm ETD is not shown here. The plot of cumulative probability versus resistances for two devices

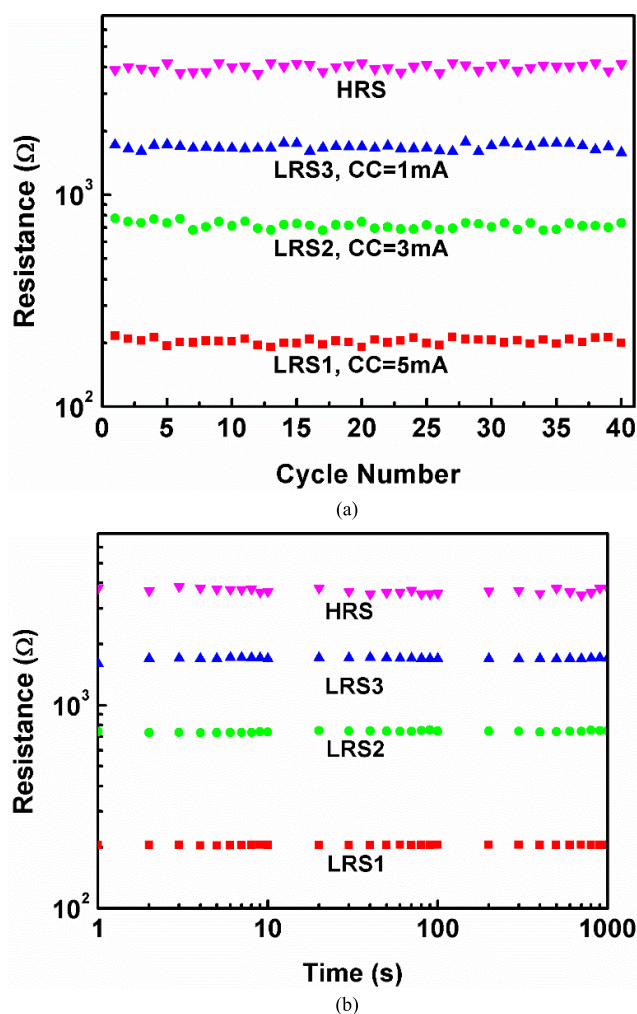


FIGURE 19. Multilevel cell operation: (a) Cycling endurance; and (b) Data retention.

with different ETDs is shown in Fig. 13. The occurrence probability of the extremely high resistances decreased from 16% to 0% by increasing ETD from 50 nm to 90 nm. The same argument can be used to explain the improvement of resistive switching uniformity as a result of the ES reduction. SEM images as shown in Fig. 14 support the argument. As shown in Fig. 15(b), no up-drifting trend was observed for both HRS and LRS resistances during the data retention test period. The degradation of the resistances shown in Fig. 15(a) could be explained by the model proposed in Fig. 16. With thicker Ag electrode and electric field enhancement, more Ag atoms located in the deeper region could take part in the filaments formation process, which resulted in thicker filaments.

To further check the device reliability performance, both the cycling endurance and the data retention tests were carried out at room temperature with more cycles and longer duration, respectively. As shown in Fig. 17 and Fig. 18(a) and (b), both the cycling endurance and the data retention failures occurred earlier in the reference device with 90° EA, $1.3 \mu\text{m}$ ES, and 90 nm ETD. For the device with 672 nm ES, although the HRS and LRS resistances were

drifting up, no set/reset failure was observed after 600 consecutive DC sweep cycles. Furthermore, no significant sign of the resistance degradation was observed after 10^5 s data retention test. The data retention test was also performed at an elevated temperature. The resistance states were maintained at 85°C for 10^5 s without any degradation as shown in Fig. 18(c). With the improved reliability, the multilevel cell operation was investigated in device with 90° EA, 672 nm ES, and 90 nm ETD as well. Three different LRS resistances were achieved by varying the set compliance current (CC) from 5 mA to 1 mA, while the HRS resistances were retained at $\sim 4 \text{ K}\Omega$ by fixing the reset stop voltage to -1.5 V . The stable cycling endurance and data retention of the four-level cell are shown in Fig. 19(a) and (b), respectively.

IV. CONCLUSION

In summary, the Ag-based RRAM device with planar double wedge-like electrodes was successfully fabricated and characterized for the first time. The device with small EA, narrow ES and deep ETD exhibited better resistive switching uniformity, cycling endurance, and data retention thanks to the electric field confinement and enhancement. Moreover, no tradeoffs between the performance indices have been demonstrated during the electrode structure engineering process. It is believed that the 3D electrode structure engineering method discussed in this work will pave the way for performance improvement of the filament type RRAM devices.

ACKNOWLEDGMENT

This work was led by the Principal Investigators J. B. Tan and T. Chen.

REFERENCES

- [1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
- [2] P. W. C. Ho, H. A. F. Almurib, and T. N. Kumar, "One-bit non-volatile memory cell using memristor and transmission gates," in *Proc. Int. Conf. Electron. Design*, 2014, pp. 244–248.
- [3] D. Ielmini and H.-S.-P. Wong, "In-memory computing with resistive switching devices," *Nature Electron.*, vol. 1, no. 6, pp. 333–343, Jun. 2018.
- [4] J. Sun, G. Han, Z. Zeng, and Y. Wang, "Memristor-based neural network circuit of full-function pavlov associative memory with time delay and variable learning rate," *IEEE Trans. Cybern.*, to be published.
- [5] W. Banerjee, Q. Liu, H. Lv, S. Long, and M. Liu, "Electronic imitation of behavioral and psychological synaptic activities using $\text{TiO}_x/\text{Al}_2\text{O}_3$ -based memristor devices," *Nanoscale*, vol. 9, no. 38, pp. 14442–14450, Sep. 2017.
- [6] J. Sun, X. Zhao, J. Fang, and Y. Wang, "Autonomous memristor chaotic systems of infinite chaotic attractors and circuitry realization," *Nonlinear Dyn.*, vol. 94, no. 4, pp. 2879–2887, Dec. 2018.
- [7] W. Banerjee, X. Zhang, Q. Luo, H. Lv, Q. Liu, S. Long, and M. Liu, "Design of CMOS compatible, high-speed, highly-stable complementary switching with multilevel operation in 3D vertically stacked novel $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{TiO}_x$ (HAT) RRAM," *Adv. Electron. Mater.*, vol. 4, no. 2, Feb. 2018, Art. no. 1700561.
- [8] W. Banerjee and H. Hwang, "Quantized conduction device with 6-bit storage based on electrically controllable break junctions," *Adv. Electron. Mater.*, vol. 5, no. 12, Dec. 2019, Art. no. 1900744.
- [9] W. Banerjee, Q. Liu, S. Long, H. Lv, and M. Liu, "Crystal that remembers: Several ways to utilize nanocrystals in resistive switching memory," *J. Phys. D, Appl. Phys.*, vol. 50, no. 30, Aug. 2017, Art. no. 303002.

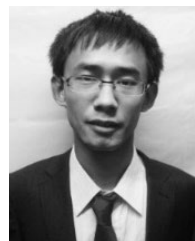
- [10] S. Yu, X. Guan, and H.-S.-P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," in *IEDM Tech. Dig.*, Dec. 2011, pp. 17.3.1–17.3.4.
- [11] S. Yu, B. Gao, H. Dai, B. Sun, L. Liu, X. Liu, R. Han, J. Kang, and B. Yu, "Improved uniformity of resistive switching behaviors in HfO₂ thin films with embedded Al layers," *Electrochem. Solid-State Lett.*, vol. 13, no. 2, pp. H36–H38, 2010.
- [12] H. Xie, M. Wang, P. Kurunczi, Y. Erokhin, Q. Liu, H. Lv, Y. Li, S. Long, S. Liu, and M. Liu, "Resistive switching properties of HfO₂-based ReRAM with implanted Si/Al ions," in *Proc. Eur. Solid State Device Res. Conf.*, 2009, pp. 221–224.
- [13] J. Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park, and H. Hwang, "Diode-less nano-scale ZrO_x/HfO_x RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications," in *IEDM Tech. Dig.*, Dec. 2010, pp. 19.5.1–19.5.4.
- [14] Y. Ahn, H. W. Shin, T. H. Lee, W.-H. Kim, and J. Y. Son, "Effects of a Nb nanopin electrode on the resistive random-access memory switching characteristics of NiO thin films," *Nanoscale*, vol. 10, no. 28, pp. 13443–13448, Jun. 2018.
- [15] G. Niu, P. Calka, M. Auf Der Maur, F. Santoni, S. Guha, M. Frasccke, P. Hamoumou, B. Gautier, E. Perez, C. Walczyk, C. Wenger, A. Di Carlo, L. Alff, and T. Schroeder, "Geometric conductive filament confinement by nanopins for resistive switching of HfO₂-RRAM devices with high performance," *Sci. Rep.*, vol. 6, no. 1, Sep. 2016, Art. no. 25757.
- [16] Z. Zhang, Y. Wu, H.-S. P. Wong, and S. S. Wong, "Nanometer-scale HfO_x RRAM," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1005–1007, Aug. 2013.
- [17] Y.-C. Huang, W.-L. Tsai, C.-H. Chou, C.-Y. Wan, C. Hsiao, and H.-C. Cheng, "High-performance programmable metallization cell memory with the pyramid-structured electrode," *IEEE Electron Device Lett.*, vol. 34, no. 10, pp. 1244–1246, Oct. 2013.
- [18] Z. Wang, K. Zhao, H. Xu, L. Zhang, J. Ma, and Y. Liu, "Improvement of resistive switching memory achieved by using arc-shaped bottom electrode," *Appl. Phys. Express*, vol. 8, no. 1, Jan. 2015, Art. no. 014101.
- [19] S. Otsuka, T. Shimizu, S. Shingubara, K. Makihara, S. Miyazaki, A. Yamasaki, Y. Tanimoto, and K. Takase, "Effect of electric field concentration using nanopink structures on the current-voltage characteristics of resistive switching memory," *AIP Adv.*, vol. 4, no. 8, Aug. 2014, Art. no. 087110.
- [20] H.-D. Kim, M. J. Yun, S. M. Hong, and T. G. Kim, "Effect of nanopyramid bottom electrodes on bipolar resistive switching phenomena in nickel nitride films-based crossbar arrays," *Nanotechnology*, vol. 25, no. 12, Mar. 2014, Art. no. 125201.
- [21] H. Sun, Q. Liu, C. Li, S. Long, H. Lv, C. Bi, Z. Huo, L. Li, and M. Liu, "Direct observation of conversion between threshold switching and memory switching induced by conductive filament morphology," *Adv. Funct. Mater.*, vol. 24, no. 36, pp. 5679–5686, Sep. 2014.
- [22] S. Gao, C. Song, C. Chen, F. Zeng, and F. Pan, "Formation process of conducting filament in planar organic resistive memory," *Appl. Phys. Lett.*, vol. 102, no. 14, Apr. 2013, Art. no. 141606.
- [23] A. Yen, A. Tritchkov, J. P. Stimiman, G. Vandenberghe, R. Jonckheere, K. Ronse, and L. Van den hove, "Characterization and correction of optical proximity effects in deep-ultraviolet lithography using behavior modeling," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 14, no. 6, pp. 4175–4178, 1996.
- [24] T. Tsuruoka, T. Hasegawa, K. Terabe, and M. Aono, "Conductance quantization and synaptic behavior in a Ta2O5-based atomic switch," *Nanotechnology*, vol. 23, no. 43, Nov. 2012, Art. no. 435705.
- [25] I. Valov and R. Waser, "Comment on real-time observation on dynamic growth/dissolution of conductive filaments in oxide-electrolyte-based ReRAM," *Adv. Mater.*, vol. 25, no. 2, pp. 162–164, Jan. 2013.
- [26] S. A. Guerrero and A. I. Akinwande, "Nanofabrication of arrays of silicon field emitters with vertical silicon nanowire current limiters and self-aligned gates," *Nanotechnology*, vol. 27, no. 29, Jul. 2016, Art. no. 295302.
- [27] C.-P. Hsiung, H.-W. Liao, J.-Y. Gan, T.-B. Wu, J.-C. Hwang, F. Chen, and M.-J. Tsai, "Formation and instability of silver nanofilament in Ag-based programmable metallization cells," *ACS Nano*, vol. 4, no. 9, pp. 5414–5420, Sep. 2010.
- [28] S. Kim, S. Cho, and B.-G. Park, "Effect of bottom electrode on resistive switching voltages in ag-based electrochemical metallization memory device," *J. Semicond. Technol. Sci.*, vol. 16, no. 2, pp. 147–152, Apr. 2016.
- [29] Y. Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. S. Kar, A. Fantini, G. Groeseneken, D. J. Wouters, and M. Jurczak, "Endurance/retention trade-off on HfO₂/metal cap 1T1R bipolar RRAM," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1114–1121, Mar. 2013.
- [30] J. Hu, H. M. Branz, R. S. Crandall, S. Ward, and Q. Wang, "Switching and filament formation in hot-wire CVD p-type a-Si:H devices," *Thin Solid Films*, vol. 430, nos. 1–2, pp. 249–252, Apr. 2003.
- [31] M. Jafar and D. Haneman, "Switching in amorphous-silicon devices," *Phys. Rev. B, Condens. Matter*, vol. 49, no. 19, pp. 13611–13615, Jul. 2002.
- [32] Y. Dong, G. Yu, M. C. Mcalpine, W. Lu, and C. M. Lieber, "Si/a-Si core/shell nanowires as nonvolatile crossbar switches," *Nano Lett.*, vol. 8, no. 2, pp. 386–391, Feb. 2008.
- [33] S. H. Jo and W. Lu, "CMOS compatible nanoscale nonvolatile resistance switching memory," *Nano Lett.*, vol. 8, no. 2, pp. 392–397, Feb. 2008.
- [34] Z. Wu, X. Zhao, Y. Yang, W. Wang, X. Zhang, R. Wang, R. Cao, Q. Liu, and W. Banerjee, "Transformation of threshold volatile switching to quantum point contact originated nonvolatile switching in graphene interface controlled memory devices," *Nanoscale Adv.*, vol. 1, no. 9, pp. 3753–3760, Aug. 2019.



JIANXUN SUN received the B.E. degree from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, in 2016, where he is currently pursuing the Ph.D. degree. He is also with the GLOBAL-FOUNDRIES Singapore as an Integration Engineer. His research focuses on the multibit resistive random access memory (RRAM) device fabrication and characterization.



YUAN BO LI received the bachelor's degree from the Wuhan University of China (WHU), in 2016, and the M.S. degree from Nanyang Technological University (NTU), Singapore, in 2017, where he is currently pursuing the Ph.D. degree. His research focuses on the transparent or flexible thin film transistor fabrication and its applications.



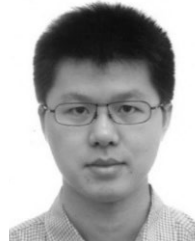
YIYANG YE received the B.E. degree from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, in 2015, where he is currently pursuing the Ph.D. degree. His research focuses on the light scattering properties of metallic nanoparticles.



JUN ZHANG received the bachelor's and master's degree from the University of Electronic Science and Technology of China (UESTC), in 2010 and 2013, respectively, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2017. He is currently a Research Associate with NTU. His research focuses on the optical properties of thin films in the applications of renewable energy.



GANG YIH CHONG received the B. Eng., M.Eng., and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1997, 2002, and 2014, respectively. He is currently a Senior Specialist with the Nanyang NanoFabrication Centre (N2FC), NTU. His research focuses on the process development of thin films deposition and dry etch for the applications of semiconductor devices.



ZHEN LIU received the B.Eng. and Ph.D. degrees in microelectronics from Nanyang Technological University (NTU), Singapore, in 2006 and 2011, respectively. He worked as a Research Fellow with NTU for about two years. In 2012, he joined the School of Materials and Energy, Guangdong University of Technology (GDUT), Guangzhou, China, where he is currently a Professor. His research interests include synthesis of ink-jet materials, ink-jet printing, metal oxide thin films and associated devices (thin-film transistors, resistive memory devices, memristors), and electrochromic films and devices.



JUAN BOON TAN received the D.Phil. degree in engineering science from the University of Oxford, U.K. He is currently a Director of the Technology Development of eNVM and Integration Technology Division, GLOBAL-FOUNDRIES, Singapore. His areas of interest and expertise include integrated process module development, CMOS integration, embedded non-volatile memory, reliability, and chip packaged interaction.



TUPEI CHEN has been a Faculty Member with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, since February 2000. He is the author or coauthor of more than 280 peer-reviewed SCI journal articles, more than 130 conference presentations, one book, and six book chapters. He has filed ten U.S. patents and 12 Technology Disclosures. His research areas include the applications of nanoscale materials in electronic devices, nanophotonic devices and renewable energy, novel memory devices, memristor and its application in artificial neural networks, Si photonics, and metal oxide thin films and their applications in flexible/transparent devices.

...