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Triple-Phase-Shift Modulation Strategy for Diode-Clamped Full-Bridge Three-Level Isolated DC/DC Converter

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ABSTRACT A triple-phase-shift (TPS) modulation strategy with reduced transformer's voltage stress is proposed in this paper for the diode-clamped full-bridge (FB) three-level isolated DC/DC converter. The proposed strategy can keep the transformer's maximum voltage changes (ΔV) at only half of the input voltage ($V_{in}/2$) by employing three phase-shift delays. Consequently, comparing with the conventional strategies, the merits of the proposed strategy include: 1) reducing the voltage change rate (dv/dt) on the transformer and 2) improving the transformer's voltage harmonics due to the merit of the multi-level voltage. Additionally, the proposed strategy has two operating modes with zero-voltage switching (ZVS) for fulfilling the wide input voltage range. Finally, the proposed strategy is verified by both simulation and experimental results.

INDEX TERMS DC/DC converter, full-bridge three-level, phase-shift control, wide input voltage range, zero-voltage switching (ZVS).

I. INTRODUCTION

Microgrid technologies are being under a huge development in recent years due to widespread utilization of distributed energy resources [1]. When refers to the type of microgrids, DC microgrids are becoming promising solutions for future smart-grid systems because of the increasing usage of renewable distributed energy sources and energy storage systems in DC form. In addition, DC microgrids have obvious merits such as high efficiency, frequency stability, no reactive power, and easy system control [2]–[7] in comparison with AC microgrids. In general, DC microgrids prefer a high DC bus voltage to increase the power delivery capability and reduce transmission losses. In DC microgrids, isolated DC/DC converters, which are responsible for delivering power and interlinking different bus voltages, are fundamental components and largely influence performances of DC microgrids [8]–[10]. Accordingly, the researches on the high-input-voltage and high-reliability isolated DC/DC converters are desired for DC microgrids.

For high voltage applications, one of most competitive candidates is the three-level (TL) based isolated DC/DC converter due to the lower switch voltage stress in comparison with the two-level based DC/DC converter [11], [12]. A lot of research about the TL based isolated DC/DC converter has been carried out so far. Reference [13] proposed an improved half-bridge (HB) TL isolated DC/DC converter (TL-IDC) with the simple phase-shift control. Based on [13], a TL-IDC with an auxiliary circuit was proposed in [14] to reduce the circulating current and thus improve the efficiency. Reference [15] proposed a new TL-IDC with series-connected transformers to both realize the zero-voltage switching (ZVS) in the almost entire load range and balance the output currents. In [16], a novel four-switch TL-IDC with a compact circuit structure was proposed. Based on [15], four kinds of TL-IDCs with wider soft-switching range were proposed in [17]. In [18], a novel ZVS control strategy was proposed to balance the currents among input capacitors and primary-side power switches for the four-switch TL-IDC proposed in [16]. Additionally, a new ZVS TL-IDC with a corresponding secondary-side phase-shift-control was proposed in [19] to reduce the circulating current for high voltage applications.

The above research is mainly about the HB TL-IDCs. However, the HB converter maybe not the most attractive choice for the high-power applications due to the high current stress on the power switch. Normally, the FB converter is preferable

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for high-power applications [20], [21]. Two hybrid full-bridge (FB) TL-IDCs were presented for the high-power applications in [22], [23]. Reference [24] proposed a chopping phase-shift (CPS) modulation strategy for the diode-clamped FB TL-IDC. Based on [24], a double phase-shift (DPS) modulation strategy was proposed to reduce the power switches' conduction loss in [25]. Additionally, reference [26] proposed a new modulation strategy to balance the currents among the primary-side power devices. However, these modulation strategies would lead the high harmonics and large electromagnetic interference due to causing the high voltage change rate (*dv/dt*) on the transformer, especially for the medium or high voltage applications. For reducing such high *dv/dt*, an improved diode-clamped FB TL-IDC with the primary-side passive filter was proposed in [27]. However, the added primary-side passive filter would increase the primary-side conduction loss and cause voltage conversion rate loss. Additionally, reference [28] proposed a new DPS modulation strategy for reducing the high *dv/dt* on the transformer, but the wide input voltage range cannot be fulfilled.

In this paper, a triple-phase-shift (TPS) modulation strategy is proposed for the diode-clamped FB TL-IDC as an extension of our previous work [29]. High voltage changes with the value of the full input voltage on the transformer occur under the conventional strategies, but the proposed strategy can maximum value of these voltage changes at only half of the input voltage (V_{in}/2). Consequently, the proposed strategy can mitigate the voltage stress, voltage change rate (*dv/dt*), and voltage harmonics on the transformer. Additionally, the proposed strategy comprises two operating modes with ZVS to fulfill the wide input voltage range. The transition between these two operating modes is seamless. Finally, the simulation and experimental results are given to validate the proposed strategy.

Comparing with the previous work in [29], this paper adds the following new contents.

1) The introduction has been enhanced.

2) The analysis of the operation principle of TPS strategy has been enhanced.

3) The theoretical analysis of the ZVS performances under the TPS strategy has been added.

4) The verified simulation results have been added.

5) More experimental results and related analysis have been added, including ZVS performances, transformer's voltage harmonics, and efficiency comparison.

The rest of this paper is organized as follows. The proposed strategy's operation principle is analyzed in detail in Section II. Section III presents a detailed analysis of the characteristics and performances of the diode-clamped FB TL-IDC under the proposed strategy. Section IV presents the simulation and experimental results to verify the proposed strategy. At last, Section V summarizes the main contributions of this paper.

II. OPERATION PRINCIPLE

The circuit topology of the diode-clamped FB TL-IDC is presented in Fig. 1, in which C_{i1} and C_{i2} are two input

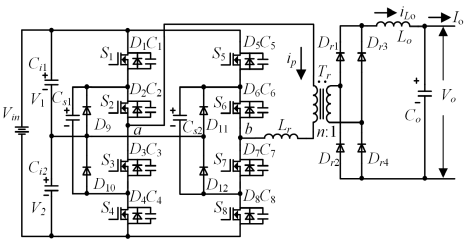

FIGURE 1. Diode-clamped FB TL isolated DC/DC converter.

capacitors; $S_1 - S_8$ and $D_1 - D_8$ are power switches and diodes; $C_1 - C_8$ are junction capacitors of $S_1 - S_8$; C_{s1} and C_{s2} are two flying capacitors; $D_9 - D_{12}$ are clamping diodes; T_r is the transformer; L_r is the leakage inductance of T_r plus the inductor in series with T_r if added; $D_{r1} - D_{r4}$ are output rectifier diodes; L_o is an output filter inductor; and C_o is an output filter capacitor. Additionally, V_1 and V_2 are voltages on C_{i1} and C_{i2}, respectively; V_{in} is the input voltage; V_{ab} and i_p are the primary-side voltage and current; n is the turns ratio of T_r; i_{Lo} is the current on L_o; V_o is the output voltage; I_o is the output current.

It is well known that the two-level FB isolated DC/DC converter is one of the most simple and common circuit topologies. When comparing with the two-level full-bridge isolated DC/DC converter, the diode-clamped FB TL-IDC as shown in Fig. 1 has more complex topology and control strategy, which means it would have higher cost and implementation complexity. However, the diode-clamped FB TL-IDC has the following merits. 1) It can withstand higher input voltage because the voltage stresses of power devices in the three-level converter is only half of that in the two-level converter. Therefore, it is more suitable for higher voltage applications. 2) It has a reconfigurable circuit structure with two operation modes, which can thus satisfy a wider range of the input voltage. 3) It has a lower ripple current on the output inductor thanks to the benefit of multi-level voltage. The detailed explanations about these merits will be provided in the following contents.

It also needs to be mentioned that the diode-clamped FB TL-IDC as shown in Fig. 1 has two flying capacitors C_{s1} and C_{s2}, which is different from the conventional diode-clamped multi-level topology without flying capacitors. The diode-clamped TL-IDC was firstly proposed in [30], in which there is no flying capacitor. However, this conventional converter can be only controlled by chopping pulse width if soft switching realization is required. Then, reference [13] proposed a diode-clamped TL-IDC with flying capacitor, which results in that the simple phase shift strategy becomes applicable for the diode-clamped TL-IDC and the soft switching can be realized meanwhile. For the diode-clamped FB TL-IDC in this paper, the reason why having flying capacitors C_{s1} and C_{s2} is the same as that in [13] to realize the soft switching under the phase shift strategy.

For simplifying the following analysis, some assumptions are made.

1) $S_1 - S_8$ have the same junction capacitors, which means that $C_1 - C_8 = C_j$.

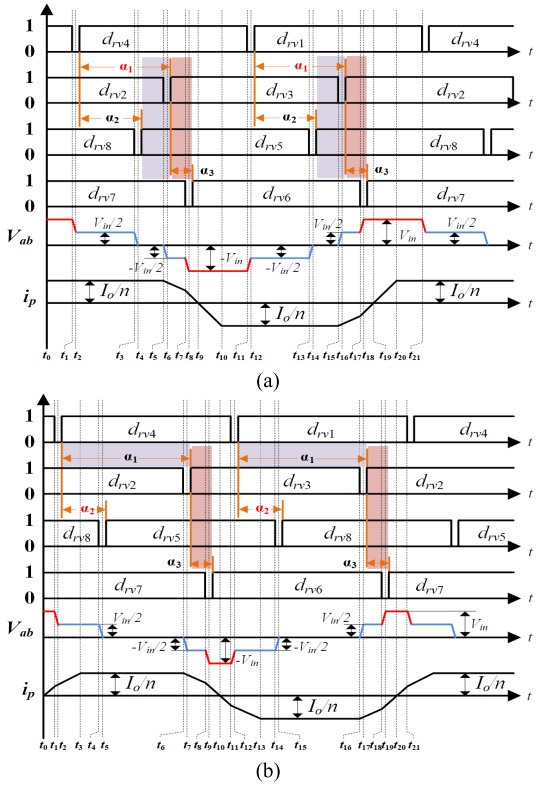

FIGURE 2. TPS modulation strategy with main waveforms. (a) Mode I. (b) Mode II.

2) L_o is regarded as a constant current source.

3) C_{i1}, C_{i2}, C_{s1}, C_{s2} are regarded as constant voltage sources with the value of $V_{in}/2$.

Fig. 2 presents the proposed TPS strategy including two operating modes named mode I and mode II. In Fig. 2, $d_{rv1} - d_{rv8}$ are driving signals of $S_1 - S_8$; α_1, α_2, and α_3 are phase-shift delays.

Mode I is used when the input voltage is low, in which $\alpha_1 - \alpha_2$ and α_3 are both kept constant. By adjusting α_1, the time intervals of the third-level voltage (V_{in} and $-V_{in}$) as highlighted by the red color in Fig. 2(a) would be changed, so the output voltage V_o can be adjusted. For example, when increasing α_1, the time length of V_{in} and $-V_{in}$ would be reduced, which means that V_o would be reduced.

Mode II is used when the high input voltage is high after α_1 increases to its maximum value. In mode II, α_1 is kept at its maximum value and α_3 is kept constant. By adjusting α_2, the time intervals of the second-level voltage ($V_{in}/2$ and $-V_{in}/2$) as highlighted by the blue color in Fig. 2(b) would be changed, so the output voltage V_o can be adjusted. For example, when decreasing α_2, the time length of $V_{in}/2$ and $-V_{in}/2$ would be reduced, which means V_o would be reduced.

It needs to be mentioned that the maximum voltage changes on the transformer in the mode I and II can be kept at only half of the input voltage ($V_{in}/2$) as shown in Fig. 2.

A. MODE I

Fig. 3 presents the equivalent circuits during the half cycle $[t_1 - t_{11}]$ in mode I. The related analysis of these equivalent

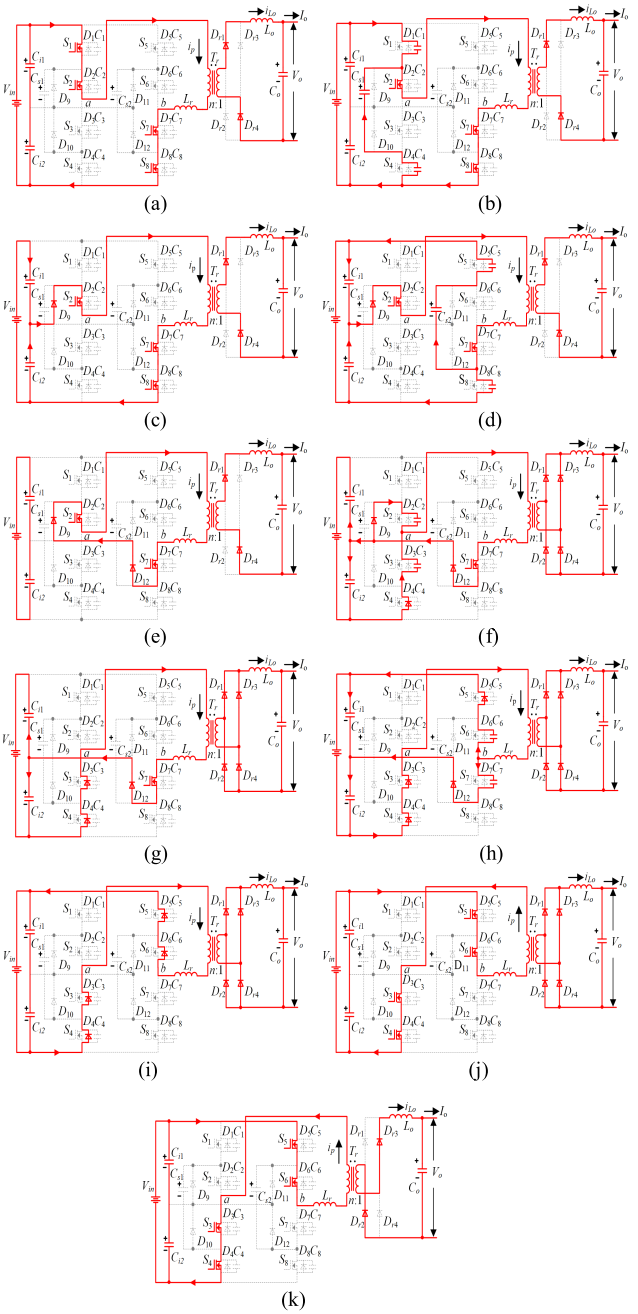

FIGURE 3. Equivalent circuits in mode I. (a) [before t_1]. (b) $[t_1 - t_2]$. (c) $[t_2 - t_3]$. (d) $[t_3 - t_4]$. (e) $[t_4 - t_5]$. (f) $[t_5 - t_6]$. (g) $[t_6 - t_7]$. (h) $[t_7 - t_8]$. (i) $[t_8 - t_9]$. (j) $[t_9 - t_{10}]$. (k) $[t_{10} - t_{11}]$.

circuits is illustrated as below. In the following analysis, $V_{c1} - V_{c8}$ are the voltages of junction capacitors $C_1 - C_8$.

Stage 1 [before t_1]: S_1, S_2, S_7, and S_8 are in on-state, so V_{ab} equals to V_{in} and D_{r1}, D_{r4} conduct. During this interval, the primary-side current i_p equals to I_o/n.

Stage 2 $[t_1 - t_2]$: At t_1, S_1 is turned off. Then, the primary-side current i_p with the value of I_o/n is to charge C_1 and discharge C_4 via C_{s1}. Consequently, V_{c1} and V_{c4} increases and decreases linearly, respectively.

Stage 3 $[t_2 - t_3]$: At t_2, V_{c1} increases to $V_{in}/2$. Then, D_9 conducts, which clamps V_{c4} at 0 V. Consequently, S_4 would

be turned on at zero-voltage. During this interval, V_{ab} equals to $V_{in}/2$ and i_p is still I_o/n.

Stage 4 [$t_3 - t_4$]: At t_3, S_8 is turned off; C_5 and C_8 would be discharged and charged by the primary-side current i_p through C_{s2}. Thus, V_{c5} decreases and V_{c8} increases linearly.

Stage 5 [$t_4 - t_5$]: At t_4, V_{c5} decreases to 0 V and V_{c8} increases to $V_{in}/2$. Then, D_{12} conducts and V_{c5} is clamped at 0 V. Consequently, S_5 would be turned on at zero-voltage. During this interval, V_{ab} and i_p equal to 0 V and I_o/n, respectively.

Stage 6 [$t_5 - t_6$]: At t_5, S_2 is turned off. Then, C_2 and C_3 are charged and discharged respectively; V_{ab} changes to be negative; i_p begins to decrease and cannot provide enough output current. All D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct and both transformer's primary voltage and secondary voltage are clamped at 0 V. Consequently, the voltage on L_r equals to V_{ab}. During this interval, L_r resonates with C_2 and C_3.

Stage 7 [$t_6 - t_7$]: At t_6, V_{c2} increases to $V_{in}/2$; V_{c3} decreases to 0 V; V_{ab} decreases to $-V_{in}/2$. Then, D_3 conducts, V_{c3} is clamped at 0 V. Consequently, S_3 would be turned on at zero-voltage. D_{r1}, D_{r2}, D_{r3}, and D_{r4} still conduct, thus the voltage on L_r equals to $-V_{in}/2$ and i_p keeps decreasing linearly.

Stage 8 [$t_7 - t_8$]: At t_7, S_7 is turned off; C_6 and C_7 are discharged and charged respectively; V_{ab} starts to decrease. i_p continues to decrease because D_{r1}, D_{r2}, D_{r3}, and D_{r4} conducts. During this interval, L_r resonates with C_6 and C_7.

Stage 9 [$t_8 - t_9$]: At t_8, V_{c7} is $V_{in}/2$ and D_6 conducts. Then, V_{c6} is clamped at 0 V. Consequently, S_6 can be turned on at zero-voltage. During this interval, D_{r1}, D_{r2}, D_{r3}, and D_{r4} still conduct, the voltage on L_r equals to $-V_{in}$, thus i_p still decreases linearly.

Stage 10 [$t_9 - t_{10}$]: At t_9, i_p decreases to 0 A. Then, the current direction of i_p begins to change. During this interval, the voltage on L_r maintains at -V_{in}, thus i_p maintains decreasing linearly.

Stage 11 [$t_{10} - t_{11}$]: At t_{10}, i_p decreases to the negative reflected output current $-I_o/n$. Then, D_{r1} and D_{r4} turn off, and D_{r2}, D_{r3} is responsible for transferring the power.

At t_{11}, S_4 is turned off. Then, the second half cycle [$t_{11} - t_{21}$] begins. The analysis during [$t_{11} - t_{21}$] is similar to that during [$t_1 - t_{11}$], thus it is not repeated here.

B. MODE II

The analysis of the equivalent circuits during the half cycle [$t_1 - t_{11}$] in the mode II is similar to that in mode I. Fig. 4 only presents the different equivalent circuits in the mode II from that in the mode I (during the time periods [$t_1 - t_3$]).

Stage 1 [before t_1]: During this interval, although S_1, S_2, S_7, and S_8 are in on-state, the primary current i_p cannot provide the enough output current and increases linearly. All D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct, thus both primary and secondary voltage on the transformer are clamped at 0 V.

Stage 2 [$t_1 - t_2$]: At t_1, S_1 is turned off. C_1 and C_4 are charged and discharged respectively by the primary-side current i_p via C_{s1}. Consequently, V_{c1} and V_{c4} increases and decreases, respectively.

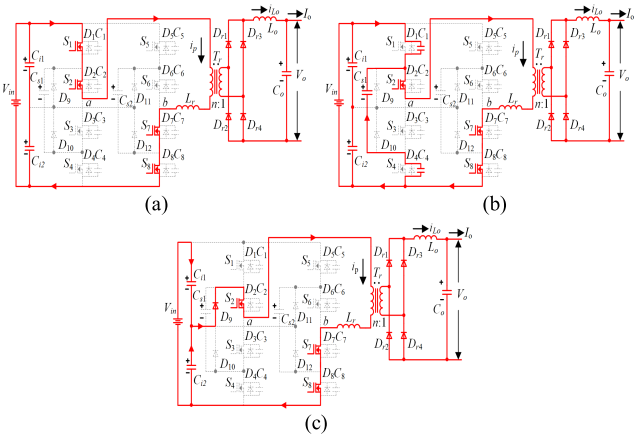

FIGURE 4. Selected equivalent circuits in mode II. (a) [before t_1]. (b) [$t_1 - t_2$]. (c) [$t_2 - t_3$].

Stage 3 [$t_2 - t_3$]: At t_2, V_{c1} increases to $V_{in}/2$, V_{c4} decreases to 0 V. Then, D_9 conducts, V_{c4} is clamped at 0 V. Therefore, S_4 can be turned on at zero-voltage. During this interval, V_{ab} is $V_{in}/2$ and i_p maintains increasing linearly.

III. CHARACTERISTIC AND PERFORMANCE ANALYSIS

A. DUTY CYCLE LOSS

Under the mode I, [$t_5 - t_{10}$] and [$t_{15} - t_{20}$] are time intervals of duty cycle losses within one switching period. If ignoring short time intervals [$t_5 - t_6$] and [$t_7 - t_8$], the time intervals [$t_5 - t_{10}$] and [$t_{15} - t_{20}$] can be given by

$$t_{10} - t_5 = t_{20} - t_{15} = \frac{\alpha_3}{2} + \frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}} \tag{1}$$

The duty cycle loss within one switching period namely D_{loss_I} can be given by

$$D_{loss\_I} = \frac{(t_{10} - t_5) + (t_{20} - t_{15})}{T_s} = \frac{\alpha_3}{T_s} + \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s} \tag{2}$$

Under the mode II, [$t_6 - t_{13}$] and [$t_{16} - t_{23}$] are time intervals of duty cycle losses within one switching period. If ignoring short time intervals [$t_6 - t_7$], [$t_8 - t_9$], and [$t_{11} - t_{12}$], the time intervals [$t_6 - t_{13}$] and [$t_{16} - t_{23}$] can be given by

$$t_{13} - t_6 = t_{23} - t_{16} = \alpha_1 + \alpha_3 + \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in}} - \frac{T_s}{2} \tag{3}$$

The duty cycle loss within one switching period namely D_{loss_II} can be given by

$$D_{loss\_II} = \frac{(t_{13} - t_6) + (t_{23} - t_{16})}{T_s} = \frac{2 \cdot (\alpha_1 + \alpha_3)}{T_s} + \frac{8 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s} - 1 \tag{4}$$

B. OUTPUT CHARACTERISTIC

Under the mode I, the average value of the output voltage namely V_{o_I} can be calculated by (5) with the consideration of the duty cycle loss in (2).

$$V_{o\_I} = \frac{V_{in}}{n} \cdot \left(1 - \frac{2 \cdot \alpha_1}{T_s} - \frac{\alpha_3}{T_s} + \frac{\alpha_2}{T_s} - \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s}\right) \tag{5}$$

Under the mode II, the average value of the output voltage namely V_{o_II} can be obtained by (6) with the consideration of the duty cycle loss in (4).

$$V_{o\_II} = \frac{V_{in}}{n} \cdot (1 + \frac{\alpha_2}{T_s} - \frac{\alpha_3}{T_s} - \frac{2 \cdot \alpha_1}{T_s} - \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s}) \quad (6)$$

C. ZVS PERFORMANCES

The ZVS performances under the mode I and II are the same, whose analysis is given as below.

1) LEADING SWITCHES

Whether the leading switches S_1, S_4, S_5, S_8 can realize zero-voltage switch-on or not is mainly decided by the reflected current from the output filter inductor. Normally, output filter inductance is quite large to ensure the leading switches realizing the zero-voltage switch-on even at the light load. For example, the energy E_1 is needed to fully discharge C_4 and charge C_1 to realize the zero-voltage switch-on of S_4. The energy E_1 can be obtained by (7).

$$E_1 \geq \frac{1}{2} \cdot C_1 \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_4 \cdot (\frac{V_{in}}{2})^2 = \frac{1}{4} \cdot C_j \cdot V_{in}^2 \quad (7)$$

2) LAGGING SWITCHES

Whether the lagging switches S_2, S_3, S_6, S_7 can realize zero-voltage switch-on or not mainly depends on the energy stored in L_r. For example, in order to achieve the zero-voltage switch-on of S_3 and S_6, the switch pairs S_2, S_7 and S_3, S_6 need to be fully charged and discharged respectively, and there also needs energy to keep the primary voltage of the transformer V_{ab} at $V_{in}/2$ in the delay time α_3. Accordingly, the equation (8) should be fulfilled to realize the zero-voltage switch-on of S_3, S_6 and S_2, S_7.

$$\frac{1}{2} L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2} \cdot C_j \cdot V_{in}^2 + \frac{V_{in} \cdot \alpha_3}{2} \cdot (\sqrt{\frac{I_o^2}{n^2} - \frac{C_j \cdot V_{in}^2}{2 \cdot L_r}} - \frac{V_{in} \cdot \alpha_3}{4 \cdot L_r}) \quad (8)$$

In (8), $\frac{V_{in} \cdot \alpha_3}{2} \cdot (\sqrt{\frac{I_o^2}{n^2} - \frac{C_j \cdot V_{in}^2}{2 \cdot L_r}} - \frac{V_{in} \cdot \alpha_3}{4 \cdot L_r})$ is the energy to keep the transformer's primary voltage V_{ab} at $-V_{in}/2$ or $V_{in}/2$ in the time intervals α_3, and $C_j \cdot V_{in}^2/2$ is the energy to fully charge the junction capacitors of (S_2, S_7) or (S_3, S_6) and discharge the junction capacitors of (S_3, S_6) or (S_2, S_7).

According to (8), the ZVS range under the TPS strategy can be obtained as

$$I_o \geq n \cdot \sqrt{\frac{C_j \cdot V_{in}^2}{L_r} + \frac{V_{in} \cdot \alpha_3}{L_r} \cdot (\sqrt{\frac{I_o^2}{n^2} - \frac{C_j \cdot V_{in}^2}{2 \cdot L_r}} - \frac{V_{in} \cdot \alpha_3}{4 \cdot L_r})} \quad (9)$$

It needs to be mentioned that: in the light load, the ZVS range can be extended by reducing α_3. The ZVS range under the proposed strategy would be the same as that under the conventional strategies when α_3 is set at zero.

D. OUTPUT FILTER INDUCTANCE

Under the mode I, two operating conditions ($V_o \geq V_{in}/2n$ and $V_o < V_{in}/2n$) are included.

If $V_o \geq V_{in}/2n$, the ripple current on the output filter inductor namely Δi_{Lo} is

$$\Delta i_{Lo} = \frac{V_{in}/n - V_o}{L_o} \cdot (\frac{2 \cdot n \cdot V_o}{V_{in}} - 1 + D_{loss\_I}) \cdot \frac{T_s}{2} \quad (10)$$

If $V_o < V_{in}/2n$, the ripple current flowing through L_o is

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot D_{loss\_I} \cdot \frac{T_s}{2} \quad (11)$$

Under the mode II, the ripple current through L_o is

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot (1 - \frac{2 \cdot n \cdot V_o}{V_{in}}) \cdot \frac{T_s}{2} \quad (12)$$

Based on the above analysis, the ripple current through L_o under the TPS strategy can be summarized as

$$\Delta i_{Lo} = \begin{cases} \frac{V_{in}/n - V_o}{L_o} \cdot (\frac{2 \cdot n \cdot V_o}{V_{in}} - 1 + D_{loss\_I}) \cdot \frac{T_s}{2} \\ \quad \text{mode I } (\mathrm{V_o} \geq \frac{V_{in}}{2 \cdot n}) \\ \frac{V_o}{L_o} \cdot D_{loss\_I} \cdot \frac{T_s}{2} \\ \quad \text{mode I } (\mathrm{V_o} < \frac{V_{in}}{2 \cdot n}) \\ \frac{V_o}{L_o} \cdot (1 - \frac{2 \cdot n \cdot V_o}{V_{in}}) \cdot \frac{T_s}{2} \\ \quad \text{mode II} \end{cases} \quad (13)$$

E. IMPLEMENTATION

For the mode I, the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of all power switches $S_1 - S_8$. $\alpha_1 - \alpha_2$ is set constant. The output voltage V_o is adjusted by changing α_1 calculated by the controller (e.g. PI controller). If neglecting the dead time, $\alpha_1 - \alpha_2$ should be longer than the voltage falling time $[t_3 - t_4]$ (from $V_{in}/2$ to 0 V) and voltage rising time $[t_{13} - t_{14}]$ (from $-V_{in}/2$ to 0 V) as shown in Fig. 2(a) to make sure that the primary voltage V_{ab} can appear 0 V; α_3 should be longer than the voltage falling time $[t_5 - t_6]$ (from 0 V to $-V_{in}/2$) and voltage rising time $[t_{15} - t_{16}]$ (from 0 V to $V_{in}/2$) as shown in Fig. 2(a) to produce the second-level voltage ($V_{in}/2$ and $-V_{in}/2$). Such voltage falling and voltage rising time are mainly determined by the capacitances of the switches' parasitic capacitors and values of the reflected current from the output current I_o.

For the mode II, the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of all power switches $S_1 - S_8$. α_1 is kept at its maximum value and α_3 is kept constant. The output voltage V_o is adjusted by changing α_2 calculated by the controller (e.g. PI controller). If neglecting the dead time, $T_s/2 - \alpha_1 - \alpha_3$ should be longer than the voltage falling time $[t_8 - t_9]$ (from $-V_{in}/2$ to $-V_{in}$) and voltage rising time $[t_{18} - t_{19}]$ (from $V_{in}/2$ to V_{in}) as shown in Fig. 2(b); α_3 should be longer than the voltage falling time $[t_6 - t_7]$ (from 0 V to $-V_{in}/2$) and voltage rising time

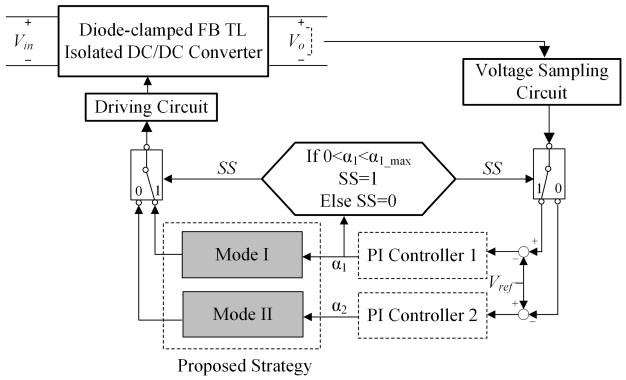

FIGURE 5. Control block of TPS strategy.

$[t_{16}-t_{17}]$ (from 0 V to $V_{in}/2$) as shown in Fig. 2(b) to produce the second-level voltage ($V_{in}/2$ and $-V_{in}/2$). Such voltage falling and voltage rising time are mainly determined by the capacitances of the switches' parasitic capacitors and values of the reflected current from the output current I_o.

Fig. 5 presents the control block of the TPS strategy for the diode-clamped FB TL-IDC, in which the conventional proportional-integral PI control algorithm is utilized to calculate phase shift delays α_1 and α_2. As shown in Fig. 5, the mode I is used for the low input voltage by adjusting α_1 from 0 to its maximum value α_{1_max}; when α_1 increases to α_{1_max} due to the increase of the input voltage, the mode II would be used for the higher input voltage by adjusting α_2.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. SIMULATION VERIFICATION

For validating the TPS strategy, a simulation model is established in PLECS, whose parameters are given in Table 1 in Appendix.

Figs. 6(a) and 6(b) show the simulation results under the three-level and two-level mode under the DPS strategy respectively. Figs. 6(c) and 6(d) show the simulation results under the mode I and II under the proposed strategy respectively. Based on the comparison results in Fig. 6, the following points can be observed.

1) The maximum voltage changes on the transformer under the three-level and two-level mode are 4 kV and 8 kV respectively, which are both full input voltages as highlighted in Figs. 6(a) and 6(b).

2) The maximum voltage changes on the transformer under the mode I and II can be reduced to 2 kV and 4 kV respectively, which are only half of the input voltages as highlighted in Figs. 6(c) and 6(d).

Consequently, it can be concluded that the voltage change rate (dv/dt) on the transformer can be effectively reduced by utilizing the TPS strategy based on 1) and 2).

B. EXPERIMENTAL VERIFICATION

A laboratory prototype with 1 kW is built to validate the TPS strategy. Table 2 in Appendix presents the circuit parameters.

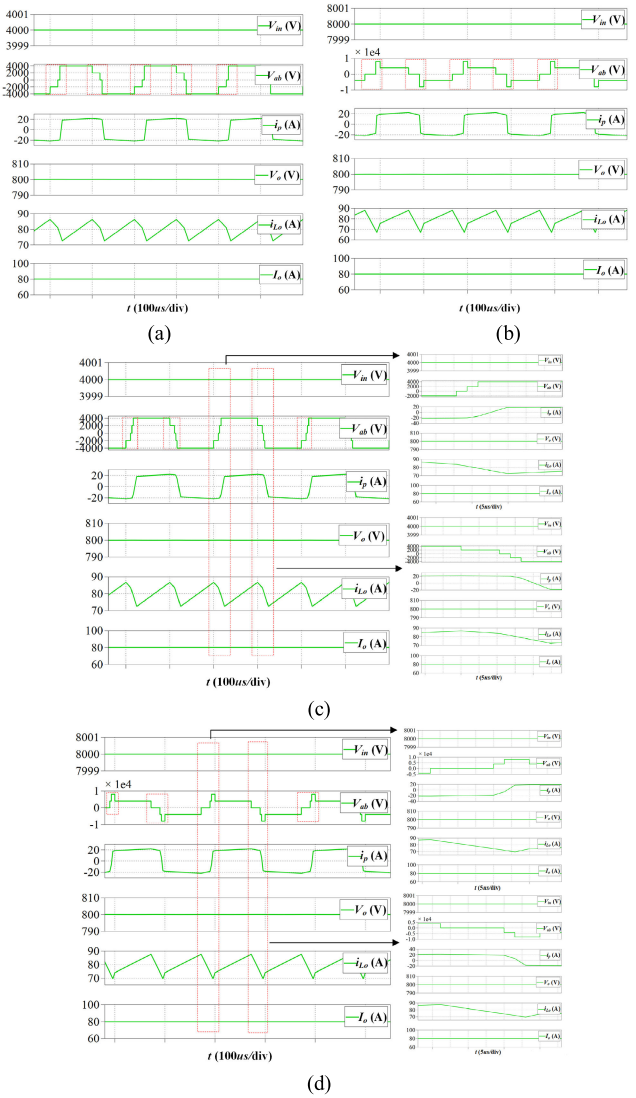

FIGURE 6. Simulation results. (a) Three-level mode of DPS strategy (V_{in} = 4 kV, P_o = 64 kW). (b) Two-level mode of DPS strategy (V_{in} = 8 kV, P_o = 64 kW). (c) Mode I of proposed strategy (V_{in} = 4 kV, P_o = 64 kW). (d) Mode II of proposed strategy (V_{in} = 8 kV, P_o = 64 kW).

The experimental results including the voltages V_{in}, V_{ab}, V_o, and the primary-side current i_p under the conventional DPS and proposed strategy are presented in Fig. 7 when V_o is 50 V and P_o is 1 kW.

From Fig. 7, the following points can be observed.

1) The mode I and II are applied to adjust the output voltage when the input voltage is low (280 V) and high (420 V) respectively, which verifies that the proposed strategy can fulfill the wide input voltage range.

2) Under the DPS strategy, the maximum voltage changes on the transformer are the full input voltage: they are 280 V and 420 V under the three-level and two-level mode respectively, as shown in Figs. 7(a) and 7(c). Under the proposed strategy, they can be reduced to only half of the input voltage: they are 140 V and 210 V under the mode I and II respectively, as shown in Figs. 7(b) and 7(d).

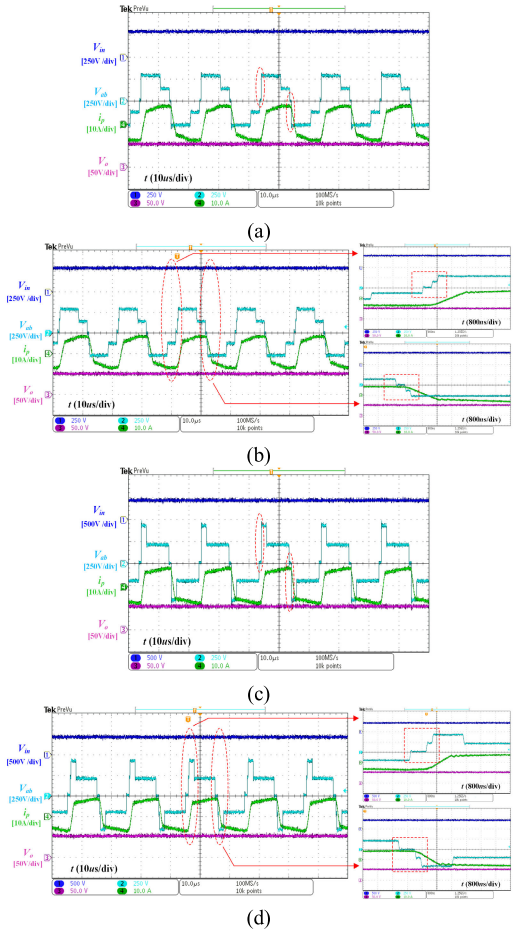

FIGURE 7. Experimental results. (a) Three-level mode of DPS strategy (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (b) Mode I of proposed strategy (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (c) Two-level mode of DPS strategy (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW). (d) Mode II of proposed strategy (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW).

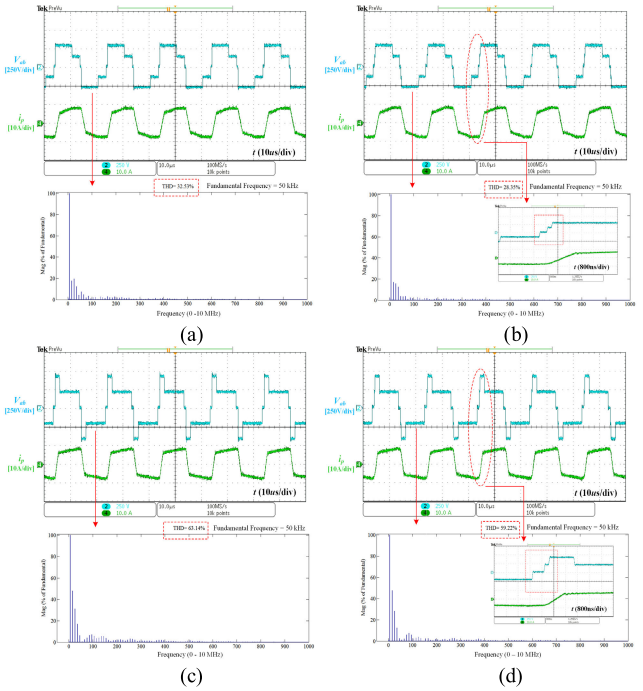

FIGURE 8. Experimental analysis about voltage harmonics on the transformer. (a) Three-level mode of DPS strategy (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (b) Mode I of proposed strategy (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (c) Two-level mode of DPS strategy (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW). (d) Mode II of proposed strategy (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW).

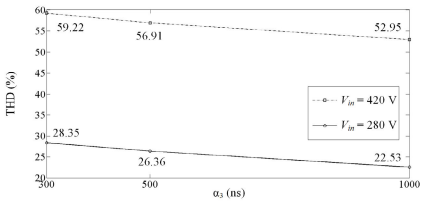

FIGURE 9. Experimental results about voltage harmonics on the transformer with various α_3 when P_o = 1 kW and V_o = 50 V.

Fig. 8 shows the experimental results of the total harmonic distortion (THD) of the transformer's primary-side voltage under the DPS and proposed strategy. Under the DPS strategy, the THD is 32.53% and 63.14% in the tree-level and two-level mode respectively (as illustrated in Figs. 8(a) and 8(c)). Under the proposed strategy, the THD can be reduced to 28.35% and 59.22% under the mode I and II (as illustrated in Figs. 8(b) and 8(d)) thanks to the multi-level voltage [31].

Fig. 9 presents the THD values with the various α_3. Under the working condition that V_{in} is 280 V, V_o is 50 V, and P_o is 1 kW, the THD can be reduced from 28.35% to 22.53% while α_3 increases from 300 ns to 1000 ns. Under the working condition that V_{in} is 420 V, V_o is 50 V, and P_o is 1 kW, the THD can be reduced from 59.22% to 52.95% while α_3 increases from 300 ns to 1000 ns. Consequently, voltage harmonics can be further improved by adjusting α_3 to produce second-level voltages ($V_{in}/2$ and $-V_{in}/2$).

Figs. 10(a) and 10(b) demonstrate the ZVS performances about the lagging switch S_3 under the mode I and II when V_o is 50 V and P_o is 500 W, in which $V_{DS}\_S_3$, $V_{GS}\_S_3$ are the drain-source and driving voltage of S_3 and $i_{DS}\_S_3$ are the drain-source current on S_3. Figs. 10(c) and 10(d) demonstrate the ZVS performances about the lagging switch S_3 under the mode I and II when V_o is 50 V and P_o is 1 kW.

Figs. 11(a) and 11(b) demonstrate the ZVS performances about the leading switch S_5 under the mode I and II when V_o is 50 V and P_o is 500 W, in which $V_{DS}\_S_5$, $V_{GS}\_S_5$ are the drain-source and driving voltage of S_5 and $i_{DS}\_S_5$ are the drain-source current on S_5. Figs. 11(c) and 11(d) demonstrate the ZVS performances about the leading switch S_5 under the mode I and II when V_o is 50 V and P_o is 1 kW.

Figs. 12(a) and 12(b) demonstrate the ZVS performances about the lagging switch S_6 under the mode I and II when P_o is 500 W and V_o is 50 V, in which $V_{DS}\_S_6$, $V_{GS}\_S_6$ are the drain-source and driving voltage of S_6 and $i_{DS}\_S_6$ are the drain-source current on S_6. Figs. 12(c) and 12(d) demonstrate the ZVS performances about the lagging switch S_6 under the mode I and II when V_o is 50 V and P_o is 1 kW.

From Figs. 10 - 12, it can be observed that the leading switch S_5 and lagging switches S_3, S_6 achieve the ZVS under

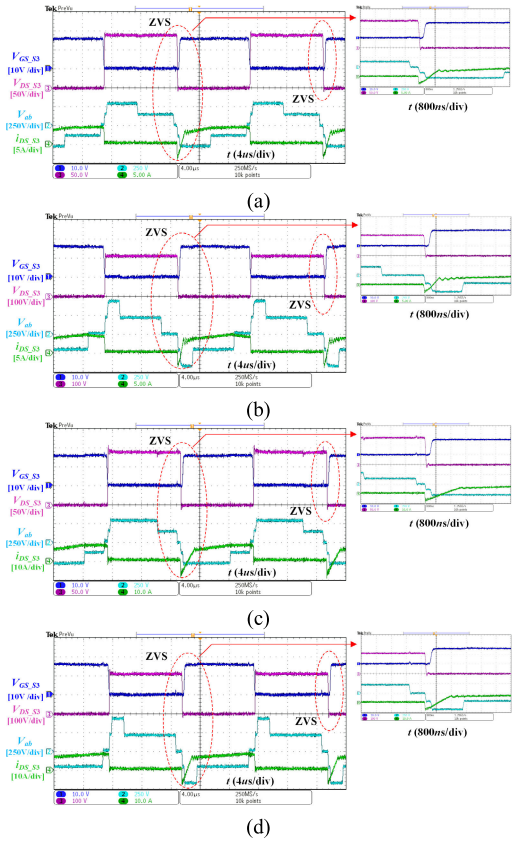

FIGURE 10. ZVS performances of lagging switch S_3. (a) Mode I (V_{in} = 280 V, P_o = 500 W, V_o = 50 V). (b) Mode II (V_{in} = 420 V, P_o = 500 W, V_o = 50 V). (c) Mode I (V_{in} = 280 V, P_o = 1 kW, V_o = 50 V). (d) Mode II (V_{in} = 420V, P_o = 1 kW, V_o = 50 V).

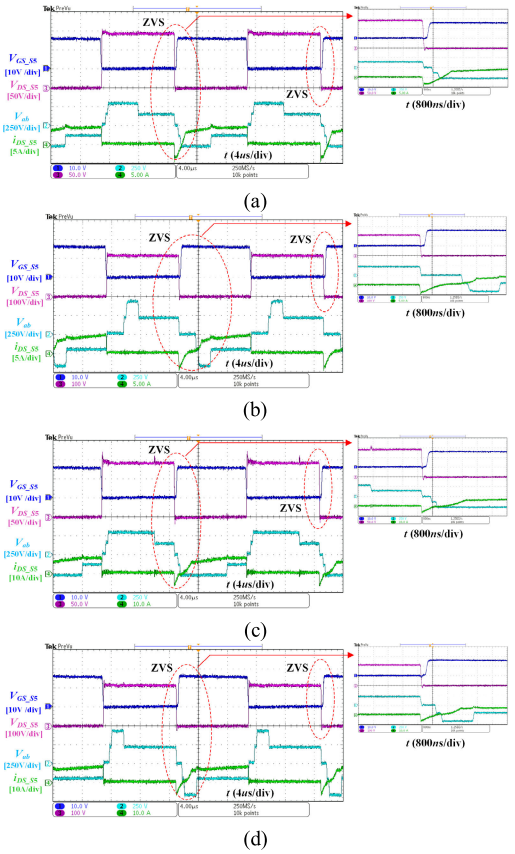

FIGURE 11. ZVS performances of leading switch S_5. (a) Mode I (V_{in} = 280 V, P_o = 500 W, V_o = 50 V). (b) Mode II (V_{in} = 420 V, P_o = 500 W, V_o = 50 V). (c) Mode I (V_{in} = 280 V, P_o = 1 kW, V_o = 50 V). (d) Mode II (V_{in} = 420 V, P_o = 1 kW, V_o = 50 V).

the proposed strategy, which would thus reduce the switching losses and noises.

Fig. 13 presents the experimental results about transition performances between the two operating modes, which includes the input voltage (V_{in}), voltages on the two input capacitors (V_1, V_2), and ac component of the output voltage $V_o^{\sim}$. In Fig. 13, V_{in} steps up from 280 V to 450 V and is finally set back to 280 V when V_o is 50 V and P_o is 1 kW. It can be observed that there is no abnormal voltage spike on the two input capacitors and output voltage during the transitions.

Fig. 14 presents the experimental results of the efficiencies between the conventional and proposed strategy. From Fig. 14, the following points can be observed as follows.

1) The efficiencies under mode I are almost the same as that under the three-level mode in the high load.

2) The efficiencies under mode II become a little lower than that under the three-level mode with the load decreasing because the used primary switches in the laboratory prototype are MOSFET.

When using MOSFET, the primary-side current i_p would go through two switches and two clamping diodes in the TPS strategy but go through four switches under the DPS strategy during free-wheeling periods. Accordingly, the TPS strategy would cause extra conduction losses because the MOSFET's conduction loss is normally smaller than that of the diode when having same current. However, for the high-power applications, IGBT is the preferable choice for the primary switches. When using IGBT, the efficiencies under

TABLE 1. Parameters of simulation model.

Component	Description
Turns Ratio of the Transformer T_r (n : 1)	4 : 1
Input Capacitors C_1 and C_2 (uF)	4700
Flying Capacitors C_{s1} and C_{s2} (uF)	1000
Output Filter Inductor L_o (uH)	1000
Output Filter Capacitor C_o (uF)	4700
Output Voltage V_o (V)	800
Output Power (kW)	64
Switching Frequency (kHz)	5

TABLE 2. Circuit parameters of laboratory prototype.

Component	Description
Power Switches S_1 - S_4	SPW47N60C3
Power Diodes D_1 - D_8	DSEI30-10AR
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of Transformer n	25 : 8
Leakage Inductance L_r (uH)	47.7
Input Capacitors C_1 and C_2 (uF)	470
Flying Capacitors C_{s1} and C_{s2} (uF)	100
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Switching Frequency (kHz)	50

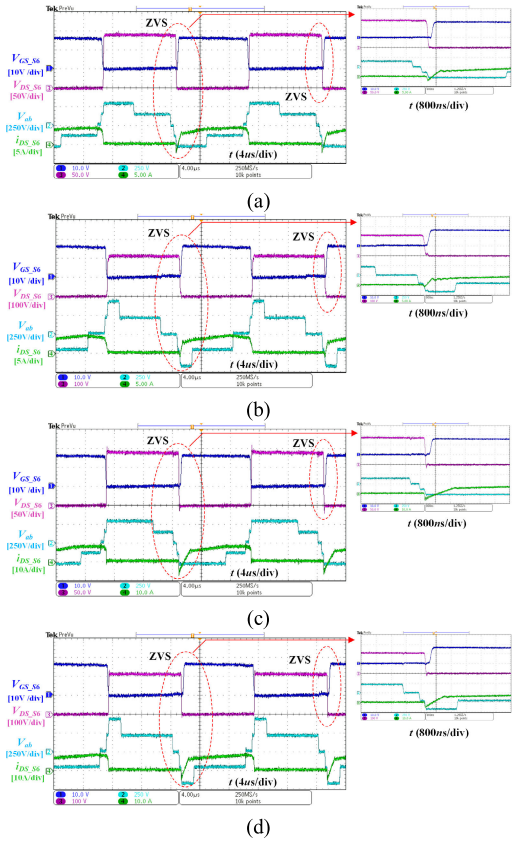

FIGURE 12. ZVS performances of lagging switch S_6. (a) Mode I (V_{in} = 280 V, P_o = 500 W, V_o = 50 V). (b) Mode II (V_{in} = 420 V, P_o = 500 W, V_o = 50 V). (c) Mode I (V_{in} = 280 V, P_o = 1 kW, V_o = 50 V). (d) Mode II (V_{in} = 420 V, P_o = 1 kW, V_o = 50 V).

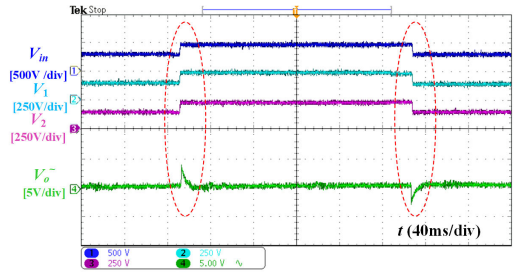

FIGURE 13. Experimental results about transition performances between two operating modes when V_o = 50 V and P_o = 1 kW.

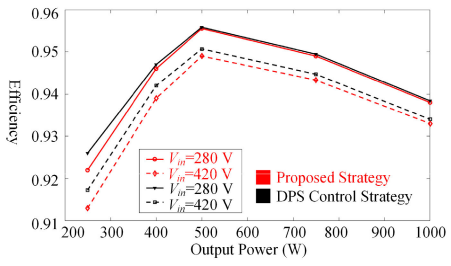

FIGURE 14. Efficiency curves with various input voltages when V_o = 50 V.

the DPS and TPS strategy would become almost the same because the primary-side current i_p would go through two switches and their body diodes under the DPS strategy.

V. CONCLUSION

This paper proposes a triple-phase-shift (TPS) modulation strategy for the diode-clamped FB TL-IDC to improve the transformer's voltage stress. By employing the three phase-shift delays, the transformer's voltage changes can be kept at only half of the input voltage (V_{in}/2) under the proposed strategy. Consequently, the voltage stress, voltage change rate (dv/dt), and voltage harmonics on the transformer can be reduced when comparing with the conventional strategies. Additionally, the proposed strategy is composed of two operating modes that can not only achieve ZVS but also fulfill the wide input voltage range. The transition between these two operating modes is seamless. Finally, the simulation and experimental results validate the proposed strategy.

APPENDIX

See Tables 1 and 2.

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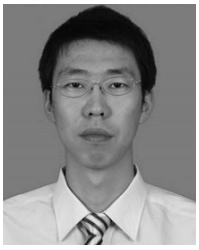

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