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High Performance Amorphous IGZO Thin-Film Transistor Based on Alumina Ceramic

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ABSTRACT Ceramic materials are high-temperature resistant materials with promising prospects. In some applications, semiconductor devices need to be integrated with a ceramic substrate. Herein, we report on the stable operation of an Al_2O_3 ceramic-based amorphous-Indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) at room temperature up to 523 K. Scanning electron microscopy (SEM) and X-ray photoelectron spectroscopy (XPS) were used to characterize the a-IGZO film. A mixed solution was printed on the surface of an insulating layer of alumina. After the combustion reaction, the metal electrode was printed on the surface of a-IGZO to obtain a TFT. The I_{ON}/I_{OFF} ratio was 6.04×10^6 at 293 K, and it was maintained at 1.44×10^5 at 523 K. It was demonstrated that the parameters of a-IGZO TFTs such as the subthreshold swing (SS), g_m and μ_{sat} changed at different temperatures. As such, they can be used as building blocks for integrated circuits that can operate at high temperatures. The fabrication of TFT-based inverters, NAND and NOR gate circuits facilitate the exploration of the possibility of more complex digital circuits that operate at high temperatures, based on hybrid circuit design.

INDEX TERMS Al_2O_3 ceramic, a-IGZO, TFT, high temperature.

I. INTRODUCTION

Thin-film transistors (TFTs) are the fundamental building blocks of advanced flat panel displays (FPDs) that are extensively used in consumer electronic products such as smartphones, portable laptops, and wearable devices [1]–[6]. With the continuous development of TFT processing technology, TFT devices have been widely used in a wide variety of fields. These devices can be integrated into sensors and tested in harsh environments such as in high-temperature environments. As such, the high-temperature resistance requirements of TFT devices are more stringent [6]–[9]. To maintain excellent properties at high temperatures, the selection of base material is of great significance. Ceramic materials are high-temperature resistant materials. They also exhibit stable properties, efficacious mechanical characteristics, wear, and corrosion resistance, in addition to low cost [10], [11]. Therefore, they are potentially ideal substrate material.

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The results of several studies have indicated that the defects of silicon materials have been effectively addressed in several wide-bandgap semiconductor materials. Funaki *et al.* prepared SiC JFET and Schottky barrier diodes (SBD) that can operate at temperatures ranging from 25 °C to 450 °C [12]. The current characteristics of SiC SBD does not change with temperature, but the JFET current decreases with an increase in temperature. A 100 V, 25 W DC-DC converter was used as an example of a high-temperature power-electronics circuit. It was determined that the conduction loss of the SiC JFET increases slightly with increasing temperature, however, its switching characteristics hardly changed. Petrosyants *et al.* researched submicron SOI CMOS technology ranging from room temperature to 300 °C and obtained reliable I-V characteristics test and stability results [13]. Zhang *et al.* improved on the preparation process of the 4H-SiC substrate and designed a temperature sensor based on an NPN type BJT (bipolar junction transistor) using a MEMS etching process [14]. The voltage and current transmission curves of the BJT were investigated at different temperatures.

In recent years, with the rapid development of printing electronic technology, solution inkjet printing has received significant attention because of its low cost and high-volume manufacturing in the field of FET and TFT manufacturing research [15], [16]. In addition, IGZO is a high-performance material for TFT semiconductor layers [17], [18] because of its high electron mobility, simple manufacturing process, robust stability and uniformity [19]–[22]. The a-IGZO semiconductor is N-type, and has a wide band gap with a value greater than 3.2 eV. Therefore, it has a high inherent breakdown voltage and desirable high-temperature characteristics [23]. The a-IGZO semiconductor is also an amorphous material that possesses isotropic internal physical properties. The carrier concentration n of a-IGZO $>10^{17}$ cm^{-3}. When the temperature changes, the carrier concentration is nearly constant. A Hall voltage signal can be detected in the a-IGZO film, indicating that the carrier is not localized [24]. However, in the range of 10^{17} cm^{-3} $<$ n $<$ 10^{16} cm^{-3}, the carrier concentration is not related to the temperature, and Hall mobility still exhibits thermal activation characteristics, which means that there is a barrier layer above the mobility side [25], [26].

Herein, we present a thin film type FET that is fabricated using inkjet printing technology. The a-IGZO semiconductor, which possesses excellent electrical properties as an oxide semiconductor material, is used as the channel material of the TFT. High-temperature resistant Al_2O_3 ceramics were selected as the substrate in the fabrication process. To verify the performance of the TFT at high temperature, it was measured at different temperatures in the range from 293 K to 523 K. The characteristic parameters of the TFT such as the $I_{DS}-V_{GS}$ and I_{ON}/I_{OFF} ratio, SS, μ and g_m were measured at different temperatures. More importantly, we prepared a digital logic circuits such as NAND and NOR gates, and inverters, using this method. We also performed measurements of the logic circuits at high temperatures. The results revealed that alumina ceramics-based a-IGZO TFTs still exhibit logic functions at high temperatures. Therefore, the TFTs and electronic devices fabricated in this investigation are potential candidates for high-temperature applications in the future.

II. PREPARATION AND CHARACTERIZATION OF MATERIALS

A. PREPARATION OF IGZO NANOPARTICLE INK

In the preparation of the IGZO ink, hydrated indium nitrate, gallium nitrate, and zinc nitrate were dissolved in 10 mL 2-methoxyethanol. A solution of 0.1 M was prepared by vigorous stirring using a magnetic stirrer. The mixture was continuously stirred and an appropriate amount of acetylacetone was added as an accelerant. This was followed by the addition of 25 % ammonium hydroxide to adjust the PH of the mixed solution. This solution was heated to 45 °C and stirred overnight to produce a uniform mixed solution that is suitable for inkjet printing.

B. CHARACTERIZATION of THE MATERIAL

As shown in Fig. 1(a), it is evident that the transparent solution of IGZO exhibits the Tyndall effect, suggesting that the IGZO is well-distributed in the solution. Fig. 1(b)–(e) depicts images of the IGZO film at different magnifications. It is evident that IGZO forms small grains with a size of approximately 30 nm. In Fig. 1(f)–(i), the energy dispersive spectrometer mapping (EDS mapping) indicates that the elements In, Ga, Zn, O are homogeneously distributed. In addition, the amount of Zn element is less than the other elements. As a result, it is reasonable to consider that a homogeneous film is formed.

To investigate the chemical state and structure of the IGZO, XPS was used to characterize the IGZO film. In Fig. 2(a), the peaks of Ga located at 1117.848 eV and 1144.781 eV are attributed to Ga 2 $P_{3/2}$ and Ga 2 $P_{1/2}$. The peaks of In are located at 444.982 eV and 452.576 eV and are attributed to In 3 $d_{5/2}$ and In 3 $d_{3/2}$. As shown in Fig. 2(d), for oxygen in different chemical states, the peaks of O at 531.697 eV, 532.569 eV, 533.232 eV are attributed to M-O-M, M-OH, and M-O-R, respectively.

C. TFT DESIGN AND FABRICATION

The proposed device structure of the a-IGZO TFT consisted of an a-IGZO channel (with several layers), an Al_2O_3 dielectric layer, and an Au gate on the Al_2O_3 substrate. The enlarged image of a-IGZO shows the schematic of the connections between In, Ga, Zn and O in Fig. 3(a). In Fig. 3(b), the fabrication process of the TFT is shown. Firstly, the Al_2O_3 substrate was ultrasonically cleaned in acetone, alcohol, and deionized water for 15 min. Ti-Au electrodes (10–50 nm) were deposited via RF sputtering at 80 W in pure argon. A layer of 15 nm of Al_2O_3 was then deposited on the electrodes using atomic layer deposition at 200 °C [27] to form a dielectric layer for the circuits. Al_2O_3 is a high k material compatible with CMOS (Complementary Metal Oxide Semiconductor) with dielectric constant k=9.5 material. It also has a high field-breakdown, which is theoretically expected to exceed 11 mV/cm [28]. In the experiments, wet etching was used to strip the deposited dielectric layer. We prepared solutions of H_3PO_4 (80%), CH_3COOH (5%), HNO_3 (5%) and H_2O (10%). These solutions were then heated to 45 °C to corrode the dielectric layer at a corrosion rate of 16 s/nm. The prepared IGZO ink was printed using an inkjet printer (Microplotter proto, Sonoplot, Middleton, WI, USA). Finally, the circuits were completed by patterning the electrodes for the a-IGZO TFTs and metallization of Ag using inkjet printing. The particle size of Ag commercial ink is 50 nm, solid content is 60%, and the viscosity is 100 cp, INNOVATION co. LTD. The $I_{DS}-V_{GS}$, and $I_{DS}-V_{DS}$ characteristics were obtained using a Keithley 4200A-SCS semiconductor analyzer and a Lakeshore Model CRX-6.5K versatile cryogen-free micro-manipulated probe station in the temperature range of 20 K to 675 K.

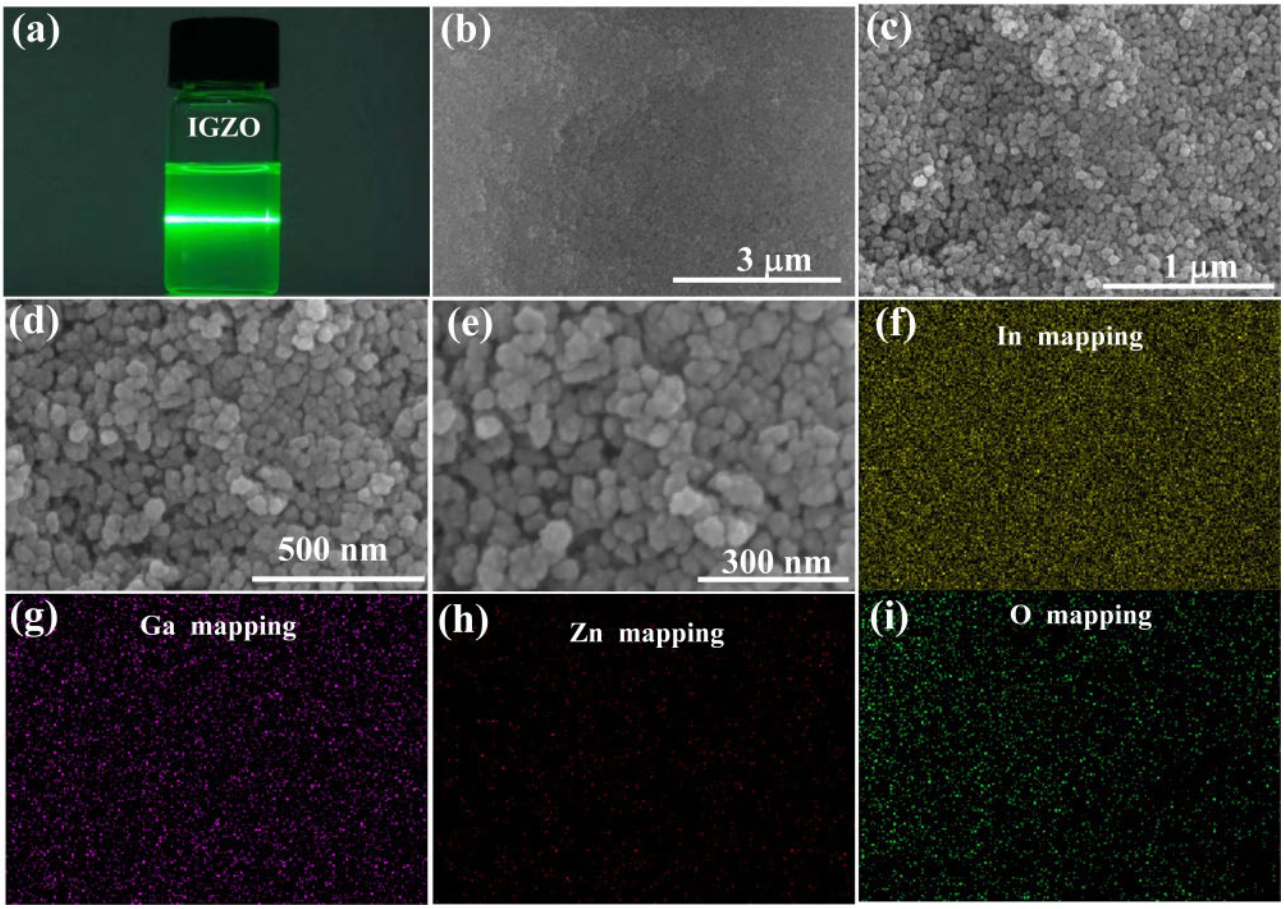

FIGURE 1. (a) Tyndall effect of the a-IGZO suspension. (b)-(e) SEM images of IGZO under different magnifications. (f)-(i) EDS mapping of IGZO.

III. RESULTS AND DISCUSSION

A. TEMPERATURE CHARACTERISTICS OF A-IGZO TFTS

In the TFT device, the semiconductor plays an important role as an active layer. However, given that the oxide semiconductor has intrinsic defects, the carrier concentration is high, and for a TFT device with excellent performance, the carrier concentration of the active layer should be minimized while the Hall mobility should be as high as possible. The a-IGZO material is composed of In_2O_3, Ga_2O_3, and ZnO. When $V_{DS} \ll V_{GS}$, the device is in the linear region, and the ON region formula is given by:

$$I_{DS} = \frac{WC_i}{L}\mu(V_{GS} - V_{TH})V_{DS}. \quad (1)$$

When $V_{DS} > V_{GS} - V_{TH}$, the transmission mode of the ON region is mainly the transmission of the tunneling effect. At this point, the device is in the saturation region, and the formula for the ON region for saturation is given as:

$$I_{DS} = \frac{WC_i}{2L}\mu(V_{GS} - V_{TH})^2. \quad (2)$$

$\mathbf{I_{ON}/I_{OFF}}$ is the ratio of the maximum value to the minimum value of I_{DS}. The minimum I_{DS} is usually determined by the noise level of the measuring device or the gate leakage current (I_{GS}), while the maximum I_{DS} depends on the semiconductor material. A high on/off current ratio is required for the successful application as electronic switches. When the device transitions from depletion to inversion, this is a critical conduction state in which time the gate voltage V_{GS} of the device is the threshold voltage. There are different methods for obtaining the threshold voltage V_{TH} including linear extrapolation of the $I_{DS} - V_{GS}$ map (low V_{DS}) or $I_{DS}1/2 - V_{GS}$ map (high V_{DS}). At a certain drain voltage, I_{DS} increases by an order of magnitude to increase the gate voltage V_{GS}. There are many factors that affect SS, such as defects in the interface between the active layer and the gate dielectric layer, gate bias, and operating temperature.

$$SS = \left(\frac{d\log(I_D)}{dV_G}|_{\max}\right)^{-1} \quad (3)$$

The mobility μ is affected by a variety of scattering mechanisms such as lattice vibration, ionized impurities, grain boundaries, and other structural defects. The field-effect mobility μ_{sat} that was extracted from the saturation region as a critical parameter for the advantages and disadvantages of the device.

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{\frac{1}{2}C_i\frac{W}{L}}. \quad (4)$$

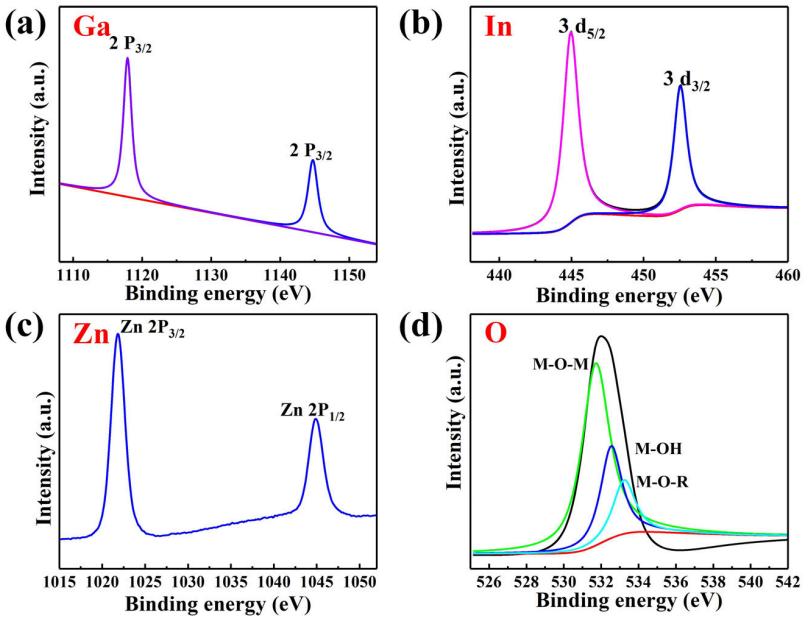

FIGURE 2. XPS spectra of a-IGZO. (a) The binding energy of Ga 2p. (b) The binding energy of In 3d. (c) The binding energy of Zn 2p. (d) The binding energy of O.

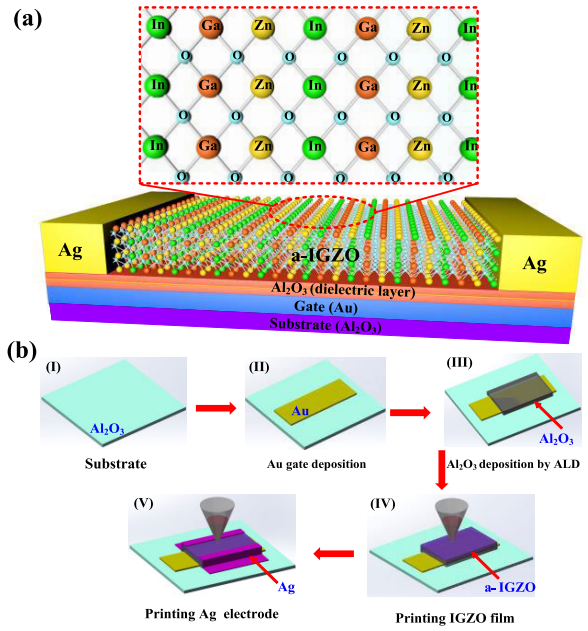

FIGURE 3. The schematic and fabrication process of the A-IGZO TFT. (a) The schematic of the a-IGZO TFT and the bonding between different atoms. (b) The fabrication processes for the TFT. (I) Ceramic substrate material with a clean and flat surface. (II) Au gate was deposited on the surface of the ceramic. (III) Al_2O_3 dielectric layer was deposited via atomic layer deposition (ALD) (IV) Inkjet printing of a-IGZO as a semiconductor layer. (V) Inkjet printing of Ag electrode.

The TFT Length to width ratio of channel of L:W=20 μm: 50 μm, and the Al_2O_3 dielectric layer with a thickness of 15 nm were tested at different temperatures. Fig. 4(a) shows the I_{DS}–V_{GS} characteristics of the TFT in the temperature range of 293–523 K (V_{GS} = 3 V). As the temperature increases, certain effects are readily observed: (i) the V_{TH} transitions to a negative value; (ii) the mobility moves in a negative direction [29]; (iii) the I_{ON}/I_{OFF} negative movement. The output and the transfer characteristic of an individual n-type IGZO TFT with a channel length of 20 μm and a channel width of 50 μm can also be observed for different temperatures. The TFT can be fully saturated and the device can be operated over the entire test temperature range. It is evident from Fig. 4(b) that the gate voltage V_{GS} exhibits effective control of the leakage current, and it also has good clamping characteristics. The leakage current I_{DS} in the saturation region is relatively stable, which indicates that the device has good electrical characteristics in the test temperature range. The variation of the threshold voltage was evaluated at different temperatures, and the V_{TH} of the TFTs can be obtained based on the $\sqrt{I_{DS}} - V_{GS}$ characteristics. Fig. 4(c) shows the relationship between these two parameters. The negative drift of V_{TH} occurs because the intrinsic carriers in the oxide semiconductor layer increase with an increase of the temperature. In addition, the drain current increases with temperature, and the ambient temperature increases at the tunnel junction. The tunneling efficiency was enhanced due to the band bending at lower gate biases, resulting in a lower V_{TH} of the device as the temperature increased. Fig. 4(d) shows the current variation of the ON and OFF states with temperature for the device. As shown in Fig. 4(e), when the temperature increases from 293 K to 523 K, the I_{OFF} increases from 10^{-15} A to 10^{-12} A, and the I_{ON} increases from 10^{-8} A to 10^{-7} A. The turn-on resistance R_{ON} decreases with temperature, and is reduced from 104.6 kΩ (293 K) to 93.7 kΩ (523 K). The trend of V_{TH} and I_{DS} can attributed to an increase in the available free carrier concentration, which escapes from the

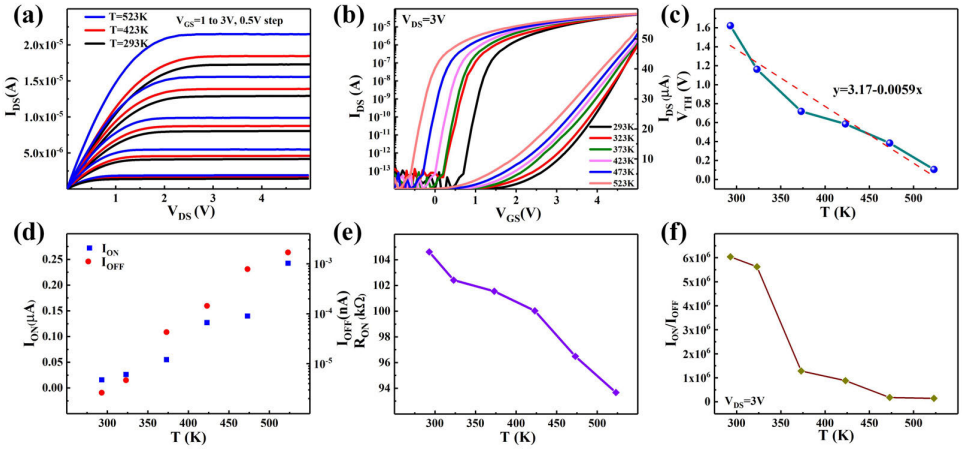

FIGURE 4. (a) The output characteristic curve of TFT at 293 K, 423 K and 523 K. (b) The transfer characteristic curve of TFT in the temperature range of 293–523 K. (c) V_{TH} decreases linearly with increasing temperature. (d) Relationship between I_{ON} and I_{OFF} with temperature. (e) Relationship between R_{ON} with temperature. (f) The I_{ON} /I_{OFF} ratio of TFT decreases with increasing temperature.

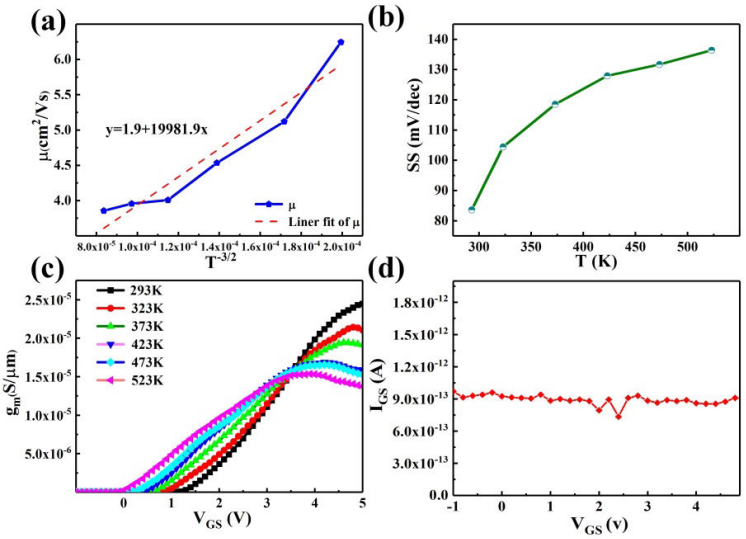

FIGURE 5. (a) The relationship between μ and $T^{-3/2}$ (423–523 K). (b) The subthreshold swing of TFT increases with increasing temperature. (c) Curves of g_m of TFT with temperature. (d) The gate leakage I_{GS} values of TFT under different V_{GS}.

local state as the temperature increases [30], [31]. The switch current ratio I_{ON}/I_{OFF} decreases from 6.04×10^6 (293 K) to 1.44×10^5 (523 K), as shown in Fig. 4(f). The reason for this phenomenon is that a temperature rise causes thermal fluctuations of the lattice atoms, resulting in vacancies and interstitial atoms. As the temperature increases, the point defects also increase, including oxygen vacancies and interstitial oxygen, which leads to a pronounced increase in the current.

Fig. 5(a) shows the variation of μ_{sat} at different temperatures. The mobility represents the conductivity of the carrier. In this experiment, the mobility μ_{sat} decreased from 6.25 cm^2/Vs (293 K) to 3.86 cm^2/Vs (523 K), the TFT channel conductivity was reduced by the temperature increase. It is also shown that the relationship between μ_{sat} and $T^{-3/2}$ is such that $\mu_{sat} \propto T^{-3/2}$ [32]. In general, the magnitude of the mobility is determined based on impurity defect scattering and lattice vibration scattering. When the device is in a low-temperature atmosphere, impurity defects and lattice vibration in the material are the main influencing factors. When the temperature is gradually increased, the scattering due to impurities in the material is substantially reduced. Therefore, the mobility in the high-temperature region is mainly affected by phonon scattering caused by the lattice vibration, and the mobility region is mainly affected by lattice vibrations at high temperatures. As the temperature increases, the lattice vibration increases, the number of phonons increases, and the effect of scattering carriers also increases, resulting in a decrease in enhanced mobility at high temperatures. The SS is an important parameter when the TFT is used as a logic switch for operation at the subthreshold state. It indicates the device's OFF state to ON state switching capability, which is

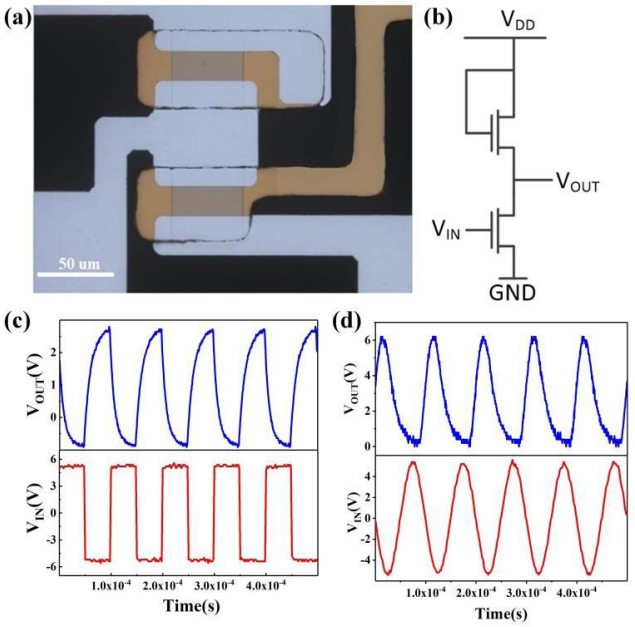

FIGURE 6. (a) Optical micrograph of a-IGZO TFTs. (b) The equivalent circuit of an inverter. (c) A 10 kHz input square wave signal (red) and the corresponding output waveform (blue). (d) A 10 kHz input sine wave signal (red) and the corresponding output waveform (blue).

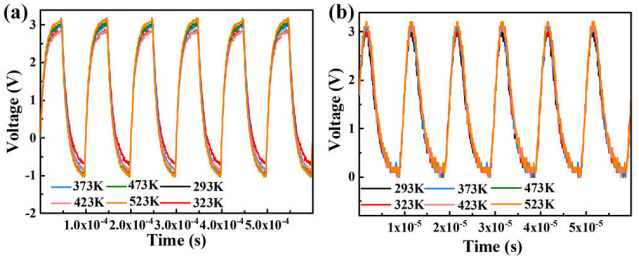

FIGURE 7. Test results for the inverter in the temperature range of 293–523 K. (a) The input signal is a square wave. (b) The input signal is a sine wave.

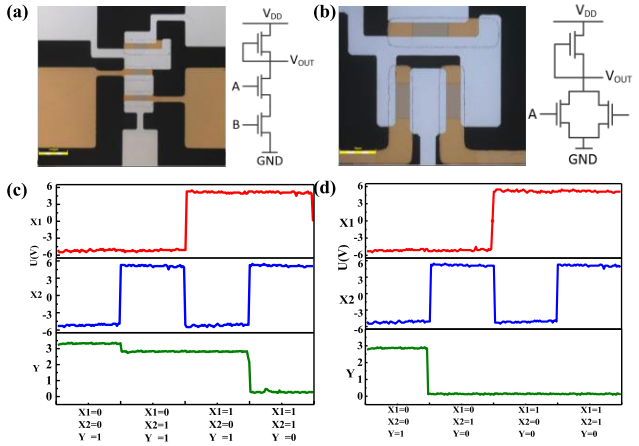

FIGURE 8. (a) Schematic diagram of the NAND gate circuit. (b) Optical image of the NAND gate circuit. (c) Schematic diagram of the NOR gate circuit. (d) Optical image of the NOR gate circuit. (e) The test results for the NAND gate circuit. (f) The test results for the NOR gate circuit.

extracted from the maximum slope of the V_{GS}–I_{DS} characteristic plot. Fig. 5(b) shows that the SS is a function of temperature. This parameter increased from 83.59 mV/dec (293 K) to 136.39 mV/dec (523 K). The density of defect states in the a-IGZO film increases at high temperatures, including the oxygen vacancies generated by the oxygen atoms that leave their initial positions due to thermal excitation. The interstitial oxygen formed by the excitation of the oxygen atoms, and the increase in the number of these intrinsic point defects caused by thermal excitation, result in an increase of SS. It is evident that with the increase of temperature, the device switching performance deteriorates [33]. Fig. 5(c) shows the relationship between g_m and temperature. This parameter g_m represents the change of the gate-source voltage to control the change of the drain-source current. Initially, at a lower V_{GS}, g_m increases with V_{GS} due to the current drive capability. However, when V_{GS} is high, it begins to decline due to reduced mobility. It is evident from the figure that g_m has a small positive change as the temperature increases [34]. The gate–source leakage current I_{GS} is always smaller than 10^{-7} μA. According to the review comment, we have measured the gate leakage I_{GS} values as shown in Fig. 5(d), it shows that the I_{GS} is about 9.0×10^{-13} A under different V_{GS}.

Fig. 6(a) represents an optical micrograph of the inverter composed of a-IGZO TFT. It can be observed that a-IGZO is transparent. Fig. 6(b) depicts the equivalent circuit of the inverter. In Fig. 6(c), a square wave signal with an input of 10 kHz and a corresponding output waveform is shown for a supply voltage $V_{DD} = 5$ V, input peak voltage of -5 to 5 V, wherein the ground (GND) of the inverter is connected to 0 V. It is evident that both waveforms can achieve a 180° phase flip, and the circuit returns the correct output signal according to the corresponding input logic. When the input signal frequency is 10 kHz, the square wave signal inverter has a propagation delay when the signal is inverted. The delay time is approximately 2.05×10^{-5} s, and the sine wave signal is not distorted, as shown in Fig. 6(d). Subsequent experiments can be performed by changing the fan-out capacitance and adjusting the channel width-to-length ratio W: L to optimize the propagation delay.

As shown in Fig. 7(a)–(b), the output waveform of the inverter at the test temperature ranged from 293 K to 523 K. It is evident that the inverter composed of the TFT can operate stably, the square wave signal inverter has a certain change in the output amplitude, the peak-to-peak value increases 1.18 times, and the sine wave signal exhibits better stability in both phase and amplitude.

In addition, to demonstrate the excellent performance of the a-IGZO TFT, we also fabricated NAND and NOR gate circuits. These circuits are composed of three TFT units. Fig. 8(a) shows optical images of a NAND gate circuit composed of three TFT interconnections, and the equivalent circuit is presented in Fig. 8(b). To demonstrate the robust performance of this circuit, it was tested at 523 K and the output result is shown in Fig. 8(e). It is evident that the circuit outputs

TABLE 1. Test result of NAND gate circuit (523 K).

Input voltage	X1= -5, X2= -5	X1= -5, X2= 5	X1= 5, X2= -5	X1= 5, X2= 5
Logic level (In)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Output voltage	3.28V	2.87V	2.84V	0.27V
Logic level (Out)	1	1	1	0

TABLE 2. Test result of NOR gate circuit (523 K).

Input voltage	X1= -5, X2= -5	X1= -5, X2= 5	X1= 5, X2= -5	X1= 5, X2= 5
Logic level (In)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Output voltage	2.90V	0.18V	0.12V	0.14V
Logic level (Out)	1	0	0	0

the correct signal according to the corresponding input logic. In addition, the optical NOR gate is shown in Fig. 8(c) and the equivalent circuit is shown in 8(d). Fig. 8(f) shows the output signal of the NOR circuit at 532 K, which exhibits the desired properties.

The results for the NAND and NOR gate circuits at 523 K are shown in Table 1 and Table 2, these circuits yielded correct output signals according to the corresponding input logic.

IV. CONCLUSION

In this report, a high-performance a-IGZO TFT based on alumina ceramic was fabricated, and the properties of an Al_2O_3-based a-IGZO TFT was investigated in the temperature range of 293–523 K. The measured DC characteristics show that the threshold voltage V_{TH} of a-IGZO TFT decreased with increasing temperature (1.62 V to 0.11 V). As the scattering processes of the channel carriers were intensified, the energy of the scattering loss increased. Therefore, the saturation velocity of channel carriers also decreased with an increase in temperature. I_{ON}, I_{OFF} increased with temperature. In addition, the I_{ON}/I_{OFF} ratio (6.04×10^6 to 1.44×10^5) and R_{ON} (104 kΩ to 94 kΩ) decreased. The saturated mobility μ_{sat} decreased (6.25 cm^2/Vs at 293 K to 3.86 cm^2/Vs at 523 K). The device switching speed decreased with an increase of the temperature because of the gradual increase of the SS of the device (83.59 mV/dec to 136.39 mV/dec). The results for the inverters, NAND, NOR gate circuits composed of multiple thin-film transistors demonstrated their reliability and stability at high temperatures, further demonstrating the potential applications of a-IGZO thin-film transistors.

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