IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received November 15, 2019, accepted December 12, 2019, date of publication December 16, 2019,
date of current version December 26, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2960092

Digital Predistorter for Short-Wave Power Amplifier with Improving Index Accuracy of Lookup Table Based on FPGA

JIJUN REN, (Member, IEEE)
School of Communications and Information Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, China
e-mail: renjijun@xupt.edu.cn

This work was supported in part by the National Natural Sciences Foundation of China under Grant 61701399.

ABSTRACT The method of function approximation to improve index accuracy of the lookup table (LUT) of digital predistortion (DPD) is proposed in this paper. The algorithm utilizes Taylor Series method for LUT approximation. The power value of a forward signal is divided into an integer and a decimal to index corresponding LUT respectively, and the indexed predistortion value of the forward signal is approached by fitting according to Taylor series, which makes the LUT index precision obviously increased. Experiment shows that comparing with the traditional Memory Polynomial Model (MPM) DPD LUT method, this model can improve Adjacent Channels Power Ratio (ACPR) over 15 dB for high frequency (HF) power amplifier's output signal, compensate for short-wave power amplifier nonlinear distortion effectively, and improve the short-wave radio communication quality greatly.

INDEX TERMS Short-wave, power amplifier, digital predistortion, look-up table, Taylor series.

I. INTRODUCTION

In recent years, the development of short-wave communication has attracted more and more attention because of its strong anti-destructive ability and autonomous communication ability. It can realize signal transmission of hundreds to tens of thousands of kilometers. As the only remote communication that is not constrained by network hub and active relay system. The main factor affecting the performance of HF communication is the nonlinearity of HF power amplifier, so it is very important for the development of HF communication to maintain high efficiency and improve the linearity of HF power amplifier at the same time.

DPD in HF power amplifier can meet the needs of high-quality voice and high-speed data transmission in HF radio. Because the memory effect of short-wave power amplifier is not strong and belongs to class AB, considering the reliability and realizability, using the look-up table digital predistortion model to linearize the short-wave power amplifier [1] can suppress the parasitic interference signal out of band and avoid interference to adjacent channels.

DPD is an effective solution for linearizing power amplifiers. Especially for power amplifiers with strong memory effect, Volterra series description is a widely used method [2]–[5]. However, due to the large number coefficient of its polynomial terms, it is hard to use it for implementation directly. In practical engineering applications, the Volterra series needs to be simplified, such as Memory Polynomial Model (MPM) [6].

By evaluating polynomial functions with evenly spaced amplitude values and then these values stored, the LUT structure is the effective implementing method [7], [8]. Although the complexity of MPM model based on LUT structure is greatly reduced, and it is more suitable for engineering applications, this traditional LUT implementation method cannot always meet the strict requirements of higher performance in actual communication systems accurately. For example, In the short-wave system, especially in the airborne radio, the requirement of the efficiency of the short-wave power amplifier is higher and higher, which makes us have to study more efficient DPD method. In the last two decades, many researchers have conducted detailed research on DPD [9]–[12].

In this paper, a real-time LUT predistorter with high-precision of the Taylor series approximation for short-wave power amplifier is proposed and herein practical FPGA implementation issues are presented. This paper is organized as follows. Section II presents the DPD algorithm and

The associate editor coordinating the review of this manuscript and approving it for publication was Xiaofei Wang.

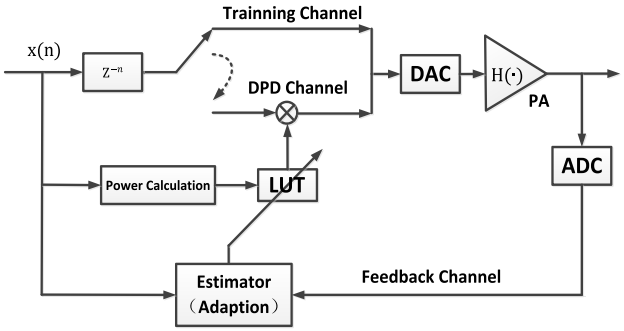


FIGURE 1. Schematic diagram of the DPD system.

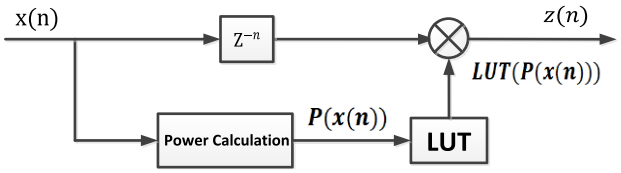


FIGURE 2. Memoryless diagram block with LUT.

architecture. Section III presents the method of Taylor series approximation to improve the index accuracy of DPD LUT. Section IV discusses issues about the experimental results, a brief conclusion is followed as Section V.

II. DPD ALGORITHM AND ARCHITECTURE

By using control algorithms operating in the digital domain, DPD acts as an open loop control system [13], [14], which means the system requires a feedback path where the PA output is compared with the input to make output of the PA to the certain level. The coefficient of the DPD estimation is carried out in the digital domain.

Fig. 1 is a schematic diagram of the DPD system. As shown in Fig. 1, it contains two channels, one is a loop structure as data training channel, the other is the DPD channel, in which the core of estimator is used to adapt the LUT of DPD.

A. LUT PREDISTORTER

The basic method is to approximate the inverse of AM-AM (gain) and AM-PM (phase) characteristics of PA by using complex gain-based LUT [15]. Recently, several LUT methods have been applied to the predistortion of PA with memory effect [16].

B. MEMORYLESS MODEL BASED ON LUT

As shown in Fig. 2, the LUT is a memoryless gain response model to describe the nonlinear system for different input powers.

$P(x(n))$ means the instant power calculation of $x(n)$, which is the index of the LUT of $LUT\ (P(x(n)))$ containing the corresponding polynomial coefficients.

Therefore, the instant output signal $z\,(n)$ of memoryless DPD model is obtained as follows:

$$z\,(n) = x\,(n) * LUT\ (P(x(n)))$$

III. MPM MODEL BASED ON LUT

The expression of Volterra series is given by

$$\begin{aligned} z\,(n) &= h_0 + \sum_{i_1=0}^{Q-1} h_1\,(i_1)\,x\,(n-i_1) \\ &+ \sum_{i_1=0}^{Q-1}\sum_{i_2=0}^{Q-1} h_2\,(i_1,i_2)\,x\,(n-i_1)\,x\,(n-i_2) \\ &+ \ldots + \sum_{i_1=0}^{Q-1}\cdots\sum_{i_k=0}^{Q-1} h_k\,(i_1,i_2\ldots i_k)\,x\,(n-i_1) \\ &\quad x\,(n-i_2)\ldots x\,(n-i_k) + \ldots \end{aligned} \tag{1}$$

MPM can be expressed as:

$$z(n) = \sum_{k=0}^{K-1}\sum_{q=0}^{Q} a_{k,q}x(n-q)\,|x(n-q)|^k \tag{2}$$

where

$$\mathrm{x\,(n)} = I_{in}\,(n) + jQ_{in}\,(n) \tag{3}$$

$$\mathrm{z\,(n)} = I_{out}\,(n) + jQ_{out}\,(n) \tag{4}$$

In Eq. (2), $a_{k,q}$ express the polynomial coefficients of $\mathrm{k^{th}}$ polynomial order and $\mathrm{q^{th}}$ memory depth. When $\mathrm{Q} = 0$, Eq. (2) can be expressed as:

$$z(n) = \sum_{k=1}^{K-1} a_{k,0}x\,(n)\,|x\,(n)|^k \tag{5}$$

Equivalently, Eq. (2) can be rewritten as

$$z\,(n) = \sum_{q=0}^{Q} x\,(n-q)\sum_{k=1}^{K-1} a_{k,q}\,|x\,(n-q)|^k \tag{6}$$

Eq. (6) is simplified as follows:

$$z\,(n) = \sum_{q=0}^{Q} x\,(n-q)\sum_{k=1}^{K/2-1} a_{k,q}\,|x\,(n-q)|^{2k} (K = \text{even})$$

$$z\,(n) = \sum_{q=0}^{Q} x\,(n-q)\sum_{k=1}^{(K-1)/2} a_{k,q}\,|x\,(n-q)|^{2k} (K = \text{odd})$$

Define

$$LUT_q\,(|x\,(n-q)|) = \sum_{k=0} a_{k,q}\,|x\,(n-q)|^{2k}$$

Therefore, we get

$$z\,(n) = \sum_{q=0}^{Q} x\,(n-q)\,LUT_q\,(|x\,(n-q)|) \tag{7}$$

$x\,(n-q)$ means the address for delay q of the $LUT_q\,(|x\,(n-q)|)$,which containing the corresponding polynomial coefficients.

The MPM model based on LUT only needs $Q+1$ time multiplications. The diagram block of the MPM model based on LUT is illustrated in Fig. 3.

Obviously, the approximation of PA model will be more accurate when the order number K and memory depth Q increase, and the complexity of model will increase considerably.

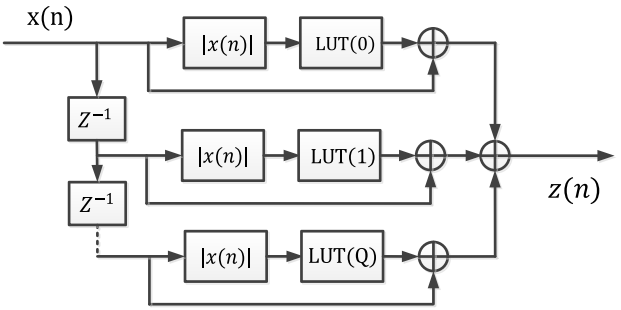


FIGURE 3. MPM model diagram block with LUT.

IV. IMPROVED INDEX ACCURACY OF LUT WITH TAYLOR SERIES METHOD

In mathematics, the function approximation of Taylor series has the following power series

$$\sum_{n=0}^{\infty} \frac{f^{(n)}(a)}{n!}(x-a)^n \tag{8}$$

From Eq. (8), we can obtain the integral and derivation of power series one by one to approximate the value of a function, which is the basic principle of the Taylor series for us to use to approximate the actual predistortion value.

Based on the 1st-order approximation function of Taylor series, the corresponding predistortion value f(x) can be expressed as Eq. (9):

$$\mathrm{f}(\mathrm{x}) \approx f(\mathrm{x}_{k-1}) + f^{(1)}(\mathrm{x}_{k-1})(\mathrm{x}_{k-1} - x) \tag{9}$$

As shown in Eq. (10), the 2nd-order approximation function of Taylor series is used to improve the approximation accuracy,

$$\begin{aligned}\mathrm{f}(\mathrm{x}) \approx{}& f(\mathrm{x}_{k-1}) + f^{(1)}(\mathrm{x}_{k-1})(\mathrm{x}_{k-1} - x) \\ &+ \frac{1}{2!}f^{(2)}(\mathrm{x}_{k-1})(\mathrm{x}_{k-1} - x)^2\end{aligned} \tag{10}$$

Based on the above theoretical basis, the n^{th}-order approximation function of Taylor series can be further used.

Taking the memoryless DPD model as an example, the method to improve the index accuracy of LUT is illustrated. On this basis, it is easy to obtain the memory DPD model.

The memoryless DPD LUT model is shown in Eq. (11):

$$\begin{aligned}\mathrm{LUT}(\mathrm{x}) = {}& \mathrm{a}_0 + \mathrm{a}_1 x + \mathrm{a}_2 x^2 + \mathrm{a}_3 x^3 \\ &+ \mathrm{a}_4 x^4 + \mathrm{a}_4 x^5 + \cdots\end{aligned} \tag{11}$$

$LUT^{(n)}(x)$ is n^{th}-order derivative of LUT(x), Eq. (12) of $LUT^{(1)}(x)$ and Eq. (13) of $LUT^{(2)}(x)$ can be obtained:

$$\begin{aligned}LUT^{(1)}(x) = {}& \mathrm{a}_1 + 2\mathrm{a}_2 x + 3\mathrm{a}_3 x^2 + 4\mathrm{a}_4 x^3 \\ &+ 5\mathrm{a}_5 x^4 + 6\mathrm{a}_6 x^5 + \cdots\end{aligned} \tag{12}$$

$$\begin{aligned}LUT^{(2)}(x) = {}& 2\mathrm{a}_2 + 6\mathrm{a}_3 x + 12\mathrm{a}_4 x^2 \\ &+ 20\mathrm{a}_5 x^3 + 30\mathrm{a}_6 x^5 + \cdots\end{aligned} \tag{13}$$

LUT(x) is the integer LUT in Fig. 4, $LUT^{(1)}(x)$ and $LUT^{(2)}(x)$ express the 1st-order and 2nd-order Taylor series

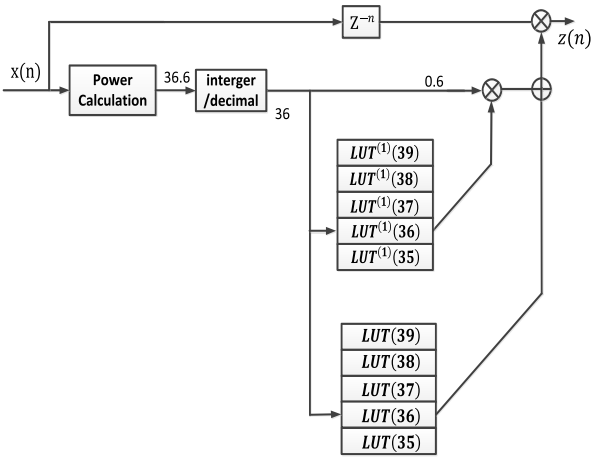


FIGURE 4. Schematic diagram of the look up table with 1st-order Taylor series.

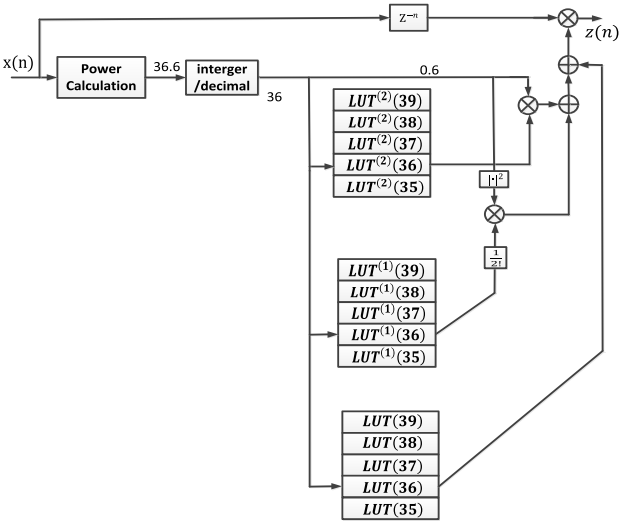


FIGURE 5. Schematic diagram of the look up table with 2nd-order Taylor series.

of LUT respectively. As shown in Eq. (9), if the power calculation value is 36.6, $\mathrm{x}_{k-1} = 36.6$, the LUT(x) can be obtained as follows:

$$\mathrm{LUT}(\mathrm{x}) \approx LUT(36) + f^{(1)}(36)(36.6 - 36)$$

As shown in Fig. 5, we can obtain the 2nd-order Taylor series based on Eq. (14)

$$\begin{aligned}\mathrm{LUT}(\mathrm{x}) \approx{}& LUT(36) + LUT^{(1)}(36)(36.6 - 36) \\ &+ \frac{1}{2!}LUT^{(2)}(36)(36.6 - 36)^2\end{aligned} \tag{14}$$

FPGA implementation of DPD LUT with Taylor approximation to improve the index accuracy of LUT is shown in Fig. 6. We use the binary truncation to realize $\frac{1}{2!}$, and in the power calculation, we use the 'square LUT' to calculate the square of decimal part.

In Fig. 6, the contents of the $\mathrm{LUT}^{(2)}$ are stored according to Eq. (15),

$$\mathrm{LUT}^{(2)}(\mathrm{m}\Delta) = \sum_{\mathrm{k}=2}^{\mathrm{K}} \frac{\mathrm{K}(\mathrm{K}-1)}{2!}\mathrm{a}_{\mathrm{k}}(\mathrm{m}\Delta)^{\mathrm{k}-2} \tag{15}$$

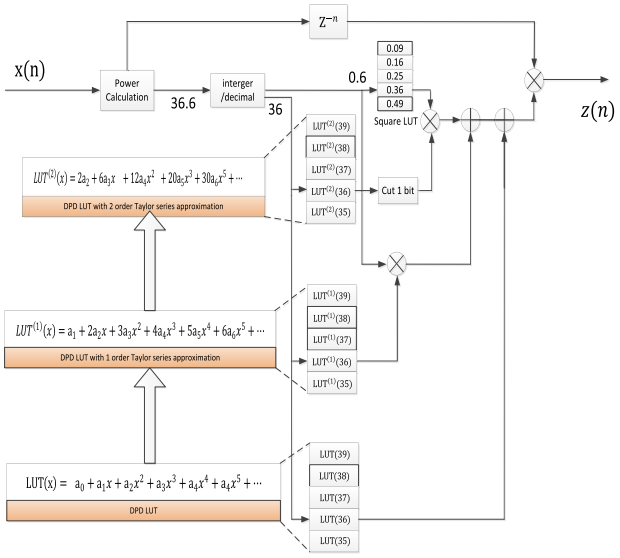


FIGURE 6. FPGA implementation of DPD LUT with Taylor series approximation.

$$\begin{array}{l} Addr\ 1 \\ Addr\ 2 \\ Addr\ 3 \\ \vdots \\ Addr\ 128 \end{array} \begin{bmatrix} a_2 + 3a_3\Delta + 6a_4\Delta^2 + 10a_5\Delta^3 + \cdots + \dfrac{K(K-1)}{2!}a_K\Delta^{K-2} \\ a_2 + 3a_3(2\Delta) + 6a_4(2\Delta)^2 + 10a_5(2\Delta)^3 + \cdots + \dfrac{K(K-1)}{2!}a_K(2\Delta)^{K-2} \\ a_2 + 3a_3(3\Delta) + 6a_4(3\Delta)^2 + 10a_5(3\Delta)^3 + \cdots + \dfrac{K(K-1)}{2!}a_K(3\Delta)^{K-2} \\ \vdots \\ a_2 + 3a_3(128\Delta) + 6a_4(128\Delta)^2 + 10a_5(128\Delta)^3 + \cdots + \dfrac{K(K-1)}{2!}a_K(128\Delta)^{K-2} \end{bmatrix}$$

FIGURE 7. Structure diagram of LUT$^{(2)}$.

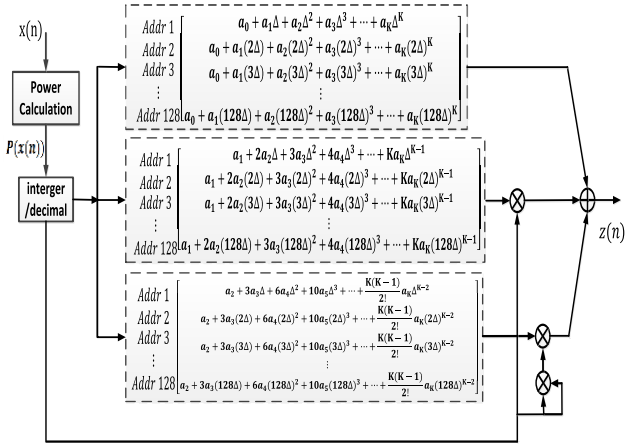


FIGURE 8. Structure diagram of LUT with 2nd-order Taylor series.

$\Delta = 1/128$, m =1,2,3…,128, and the storage content and specific structure are shown in Fig. 7.

Fig. 6 can be further expressed as Fig. 8.

FPGA implementation of DPD LUT with 3rd-order Taylor approximation to further improve the index accuracy of LUT is shown in Fig. 9.

V. EXPERIMENTAL VALIDATION

In order to verify the digital predistortion effect of HF power amplifier, the AB class HF power amplifier with a central

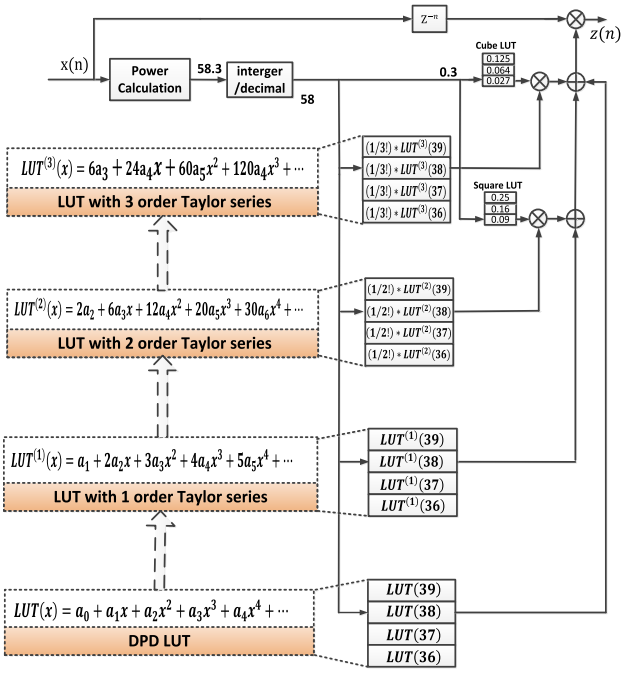


FIGURE 9. Structure diagram of LUT with 3rd-order Taylor series.

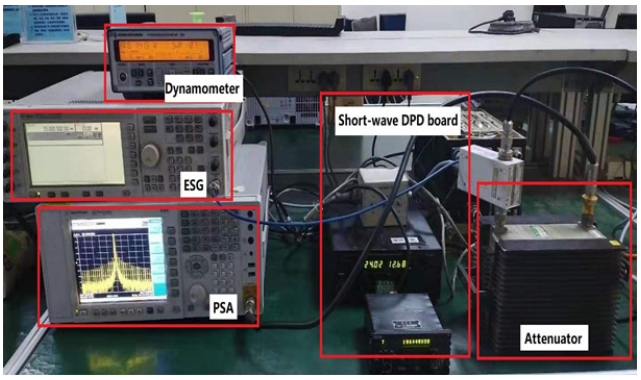


FIGURE 10. Diagram of experimental testbed.

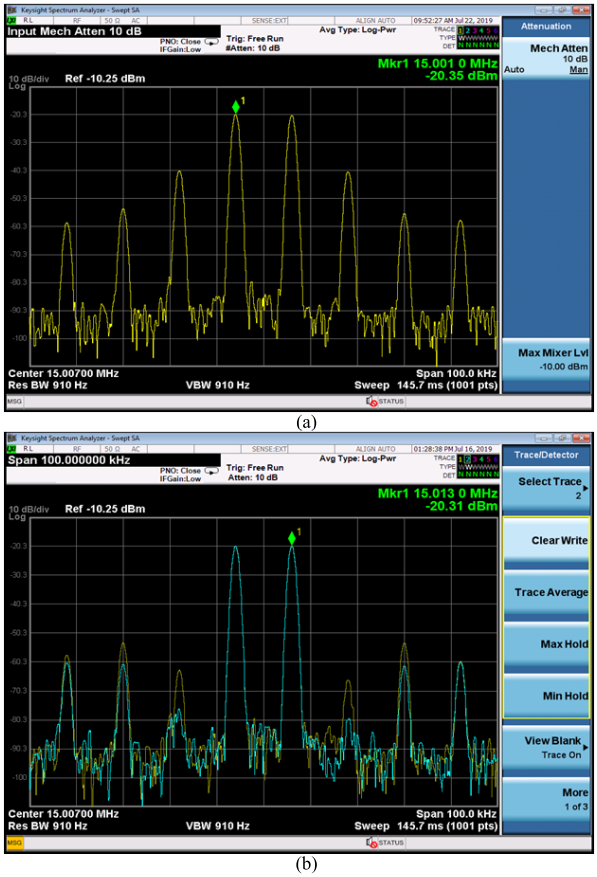
frequency of 1.6∼30 MHz and a power output of 140 W are used to test, as shown in Fig. 10.

According to the test standard of HF system, the two-tone signal with an interval of 12KHz is used as the test verification signal. We also can see that the maximum allowable levels of noise and distortion as a function of the frequency offset in Fig. 11(a). Fig. 11(b) shows that comparing with the traditional MPM DPD LUT method (k = 5, Q = 3, yellow line), the LUT of Taylor series approximation (blue line) we mentioned can improve the ACPR more than 15dB.

The normalized mean-squared error (NMSE), defined by the Eq. (16), was used to validate the performance of DPD with this work.

$$NMSE_{dB} = 10log_{10}\left(\frac{\sum_{n=1}^{N}|z(n)-\tilde{z}(n)|^2}{\sum_{n=1}^{N}|z(n)|^2}\right), \quad (16)$$

where $z(n)$ is the desired output and $\tilde{z}(n)$ is the simulated output. The results are reported in Table 1.



(a)

(b)

FIGURE 11. DPD LUT with Taylor series approximation in real HF system. (a) Spectra of PA outputs, (b) Spectra of DPD MPM LUT method w/o Taylor series approximation (blue line w/o yellow line).

TABLE 1. Accuracy of models using different method.

Quantity	NMSE/dB [a]
without DPD	-33.74
DPD with MPM (K=5, Q=3)	-46.25
DPD with this work	-53.12

VI. CONCLUSION

We present the method to improve index accuracy of LUT of digital predistorter in this paper. The predistortion values of the integer LUT and the N decimal LUTs is calculated corresponding to the power value of the forward signal based on the method of Taylor series. We divide the power value of a forward signal into an integer and a decimal to index corresponding LUTs respectively and approach a real predistortion value of the forward signal by fitting according to Taylor series formula, which makes the index precision of DPD LUT obviously increased, and the performance of DPD in HF system is improved more than 15dB.

REFERENCES

[1] K.-F. Liang, J.-H. Chen, and Y.-J. E. Chen, "A quadratic-interpolated LUT-based digital predistortion technique for cellular power amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 3, pp. 133–137, Mar. 2014.

[2] E. G. Lima, T. Cunha, H. M. Teixeira, M. Pirola, and J. C. Pedro, "Baseband derived volterra series for power amplifier modeling," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jul. 2009, pp. 1361–1364.

[3] J. C. Nuñez-Perez, J. R. Cardenas-Valdez, C. Gontrand, J. A. Reynoso-Hernandez, F. I. Hirata-Flores, R. Jauregui-Duran, and F. J. Perez-Pinal, "Flexible test bed for the behavioural modelling of power amplifiers," *Compel Int. J. Comput. Math. Electr. Electron. Eng.*, vol. 33, no. 1, pp. 355–375, Jan. 2014.

[4] J. R. Cárdenas-Valdez, J. C. Núñez-Pérez, J. A. Galaviz-Aguilar, A. Calvillo-Téllez, C. Gontrand, J. A. Reynoso-Hernández, and E. Tlelo-Cuautle, "Modeling memory effects in RF power amplifiers applied to a digital pre-distortion algorithm and emulated on a DSP-FPGA board," *Integration*, vol. 49, pp. 49–64, Mar. 2015.

[5] M. Rawat, K. Rawat, F. M. Ghannouchi, S. Bhattacharjee, and H. Leung, "Generalized rational functions for reduced-complexity behavioral modeling and digital predistortion of broadband wireless transmitters," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 2, pp. 485–498, Feb. 2014.

[6] R. N. Braithwaite, "Digital predistortion of an RF power amplifier using a reduced volterra series model with a memory polynomial estimator," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 10, pp. 3613–3623, Oct. 2017.

[7] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *IEEE Trans. Signal Process.*, vol. 54, no. 10, pp. 3852–3860, Oct. 2006.

[8] P. L. Gilabert, A. Cesari, G. Montoro, E. Bertran, and J.-M. Dilhac, "Multi-lookup table FPGA implementation of an adaptive digital predistorter for linearizing RF power amplifiers with memory effects," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 2, pp. 372–384, Feb. 2008.

[9] A. M. Belabad, S. Sharifian, and S. A. Motamedi, "An accurate digital baseband predistorter design for linearization of RF power amplifiers by a genetic algorithm-based Hammerstein structure," *Analog Integr. Circuits Signal Process.*, vol. 95, pp. 231–247, Apr. 2018.

[10] Q. Zhang, W. Chen, and Z. Feng, "Reduced cost digital predistortion only with in-phase feedback signal," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 257–259, Mar. 2018.

[11] K. J. Muhonen, M. Kavehrad, and R. Krishnamoorthy, "Look-up table techniques for adaptive digital predistortion: A development and comparison," *IEEE Trans. Veh. Technol.*, vol. 49, no. 5, pp. 1995–2002, Sep. 2000.

[12] M. Rawat, P. Roblin, C. Quindroit, K. Salam, and C. Xie, "Concurrent dual-band modeling and digital predistortion in the presence of unfilterable harmonic signal interference," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 625–637, Feb. 2015.

[13] D. Psaltis, A. Sideris, and A. A. Yamamura, "A multilayered neural network controller," *IEEE Control Syst. Mag.*, vol. 8, no. 2, pp. 17–21, Apr. 1988.

[14] F. M. Ghannouchi and O. Hammi, "Behavioral modeling and predistortion," *IEEE Microw. Mag.*, vol. 10, no. 7, pp. 52–64, Dec. 2010.

[15] Q. A. Pham, D. Lopez-Bueno, T. Wang, G. Montoro, and P. L. Gilabert, "Multi-dimensional LUT-based digital predistorter for concurrent dual-band envelope tracking power amplifier linearization," in *Proc. IEEE Top. Conf. RF/Microw. Power Amplif. Radio Wireless Appl. (PAWR)*, Jan. 2018, pp. 47–50.

[16] A. Molina, K. Rajamani, and K. Azadet, "Concurrent dual-band digital predistortion using 2-D lookup tables with bilinear interpolation and extrapolation: Direct least squares coefficient adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 4, pp. 1381–1393, Apr. 2017.

JIJUN REN received the B.Sc. and M.Sc. degrees *(cum laude)* in electronics information engineering and the Ph.D. degree in wireless communication from Northwestern Polytechnical University, China, in 2002, 2005, and 2010, respectively.

Since 2007, he has been with ZTE Communications, Xi'an, China, with a dissertation on linearity and efficiency enhancement of mobile communication power amplifiers. His research interests include wireless communications, nonlinear system modeling and linearization, and RF power amplifiers. He is currently involved in research work in related fields with the Xi'an University of Posts and Telecommunications, undertaking and participating in a number of national and provincial research topics, and cooperating with enterprises in related fields.