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A 2.35/2.4/2.45/2.55 GHz Low-Noise Amplifier Design Using Body Self-Biasing Technique for ISM and LTE Band Application

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ABSTRACT This paper presents a quadruple-band low noise amplifier (LNA) which utilizes a differential pair common-source (CS) cascode amplifier to drive a LC-tank loading. The capacitors array are parallel with the LC-tank to implement the central frequency selection. The band-selection switch employs the binary voltage controlling to alter the equivalent capacitance of capacitors array of the loading LC-tank, which results in the central frequency of the LNA is switched. The body self-biasing technique is designed to minimize the noise contribution caused by the body effect of the MOS devices. In addition, the analysis of the transistors dimension ratio versus output referred 1-dB compression point (OP_{1-dB}) is presented to describe the design of the linearity optimization in CS cascode LNA. The $|S_{21}|$ is 16.8, 16.63, 16.78, 16.39 dB at 2.35, 2.4, 2.45, 2.55 GHz, respectively. The noise figure (NF) is under 2.75 dB between the quadruple-band mode. This proposed LNA is simulated by 55 nm RF CMOS process and consumes 3.75 mW excluding output buffer from 1.25 V supply.

INDEX TERMS CMOS, RFIC, low-noise amplifier (LNA), quadruple-band, common-source, cascode, body biasing.

I. INTRODUCTION

Due to the increasing demands for many wireless communication applications and standards nowadays, for examples, 802.11 WLAN, LTE, and BLE. Band-selection has been an important function in RF transceivers. There are many methodologies which have been proposed for the design of dual-band LNAs [1]–[10]. However, it is more difficult than dual-band LNAs to design the multi-band LNAs due to the more complicated methodologies and challenges [11]–[17]. One approach utilizes the series of LC-ladder configuration to achieve the tapped capacitors configuration to realize a switched multi-band resonators [11]–[13]. Tzeng *et al.* proposed a tapped capacitor topology between two loading inductors to realize a switched tri-band resonators [11]. However, this topology occupies larger area than single-band LC-tank loading impedance. In addition, the bandwidth is also restricted by the operation frequency because it is inversely proportional to the equivalent loading capacitance of the resonator [18]. Although C. C. Chen et al. proposed a gain-bandwidth product (GBW) optimization technique to extend the bandwidth of the tuned amplifier, the linearity weakens due to the dc bias near the triode region boundary [6], [12]. Yu *et al.* proposed a switched multi-tap transformer utilized in the input matching network of an inductively degenerated CS amplifier [13]. However, it also needed a mutual inductance with larger area than single-band input impedance matching network, which results in more manufacture cost. Another approach employs the notch filters to achieve multi-band performance in a LNA [14], [15]. Although this approach can achieve good noise figure and stopband rejection ratios, it is based on the design of the wide bandwidith including multi-band notch filter. Therefore, this topology needs the costs of high power consumption and large area occupation. The other approach involves the use of the RF switches to achieve band-selection by the time division duplex (TDD) technique [16], [17]. However, this approach needs to utilize several LNAs with different output resonant

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frequency, and switch between each other. Hence, the area and cost are much higher several times than single LNA.

Additionally, researchers presented the performance of the operation characteristic corresponding to the forward body biasing (FBB) of MOS [19]–[23]. H. Rashtian et al. proposed the analysis results of the gain, linearity, and input matching with FBB technique, which indicates that the linearity was improved by the forward bias of the body in CS amplifier [19]. T. P. Wang proposed a methodology to minimize the junction leakage current and noise contribution by connecting high impedance between the device bulks and forward bias [20]. In [21], H. Rashtian also proposed the analysis results of the optimized noise figure by altering the voltage V_{BS} between the device bulks and forward bias. By this method, the forward bias V_{BS} could be found with the best noise performance. B. K. Kim et al. presented the third-order distortion cancelling methodology by FBB technique in a CMOS CS amplifier [22]. However, this approach needs to dissipate high current to maintain the power gain of the amplifier. M. Parvizi et al. proposed the use of FBB to mitigate output conductance degradation due to short channel effects [23]. This approach could enhance the intrinsic gain of LNAs. However, it needs to use a higher voltage supply.

Hence, in order to improve the drawback of high power dissipation of multi-band LNAs, a capacitance array is used to achieve a band-selection function in this proposed LNA, which consumes lower power than LNAs with notch filter technique. In addition, the body self-biasing technique is employed to minimize the noise contribution of the transistors in the proposed CS cascode LNA without sacrificing the linearity. The band of ISM and LTE has been applied for wireless communication application due to the increasingly growing of mobile device demand. According to the definition of Industrial Scientific Medical (ISM) Band by ITU Radio-communication Sector (ITU-R), there is a common unlicensed wireless spectrum during 2.4−2.4835 GHz for open worldwide communication [24]. For examples, both of WLAN IEEE 802.11 b/g/n and Bluetooth are located at 2.4 GHz ISM band. In addition, by the definition of LTE standard of Universal Mobile Telecommunications System (UMTS) by The 3rd Generation Partnership Project (3GPP), the operating band of TDD-LTE contains 2300−2400 MHz (Band 40) and 2496−2690 MHz (Band 41) [25]. Therefore, the proposed LNA is suitable for use in the RF receiver frontend integrating 2.4/2.45 GHz ISM band as well as 2.35/2.55 GHz TDD-LTE band.

The remainder of this paper is organized as follows. Section II introduces the proposed noise minimization using body self-biasing technique, input impedance matching, linearity design in CS cascode amplifier, noise analysis of the proposed quadruple-band CS cascode CMOS LNA. Section III presents the simulation results demonstrating the feasibility of the proposed technique. Section IV provides conclusions.

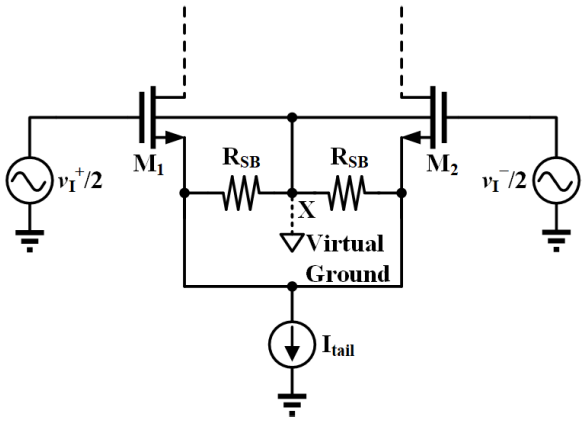

FIGURE 1. The differential CS amplifier with body self-biasing schematic.

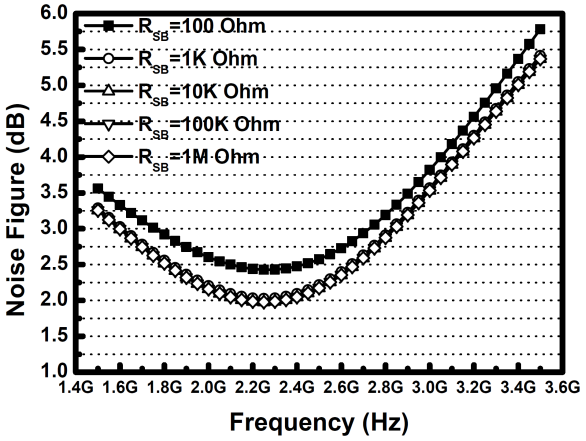

FIGURE 2. The simulated noise analysis about resistor R_{SB} dimension of the body self-biasing amplifier schematic.

II. PRINCIPLES OF LNA DESIGN

A. NOISE MINIMIZATION USING BODY SELF-BIASING TECHNIQUE

Fig. 1 shows the differential input CS amplifier schematic with body-self biasing, where the model of all MOS transistors was applied with triple-well configuration including deep n-well. The noise contribution from the bulk of MOS cannot be ignored due to the distributed physical bulk resistance [20]. Additionally, the voltage V_{SB} between source and body causes the body-effect which decreases the transconductance of MOS. Therefore, the input-referred drain-current noise factor of MOS would increase because the noise factor is inversely ratio to the transconductance g_m of MOS [26], which is expressed as follows:

$$F_{drain-current} = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s} \quad (1)$$

where

$$g_m = k_n' \cdot \frac{W}{L} \cdot (V_{GS} - V_t) \quad (2)$$

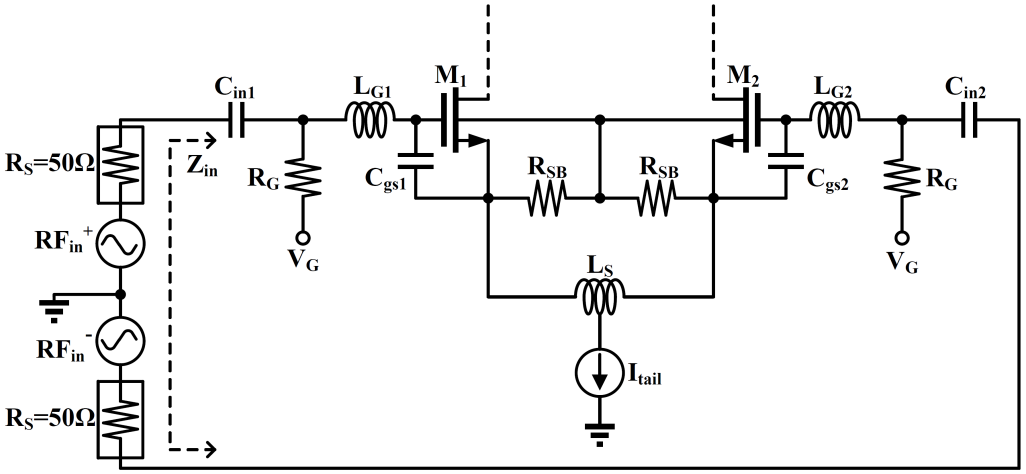

FIGURE 3. The differential common-source amplifier topology with input impedance matching network.

and

$$V_t = V_{t0} + \sigma\left(\sqrt{|2\phi_f + V_{SB}|} - \sqrt{|2\phi_f|}\right) \tag{3}$$

where $g_m = g_{m,M1} = g_{m,M2}$, $\alpha = g_m/g_{d0}$, g_{d0} is the drain-source conductance at $V_{DS} = 0$, γ is the measured noise coefficient of CMOS process technology, k_n' is equal to $\mu_n C_{ox}$ of the MOS, W/L is the ratio of MOS dimension, V_t is the threshold voltage of the MOS, V_{t0} is the threshold voltage for zero substrate bias, σ is the fabrication-process parameter, and ϕ_f is the substrate Fermi potential, respectively. By substituting (3) into (2), we could obtain that the g_m would lower while V_{SB} raises. Hence, the body-self biasing is employed to make $V_{SB} = 0$ in order to minimize the noise contribution corresponding to the body-effect [21].

As seen from Fig. 1, node X which is the body terminals of both the MOS transistors connects to the source terminals of M_1 and M_2 with resistors R_{SB}. Hence, V_{SB} is equal to zero under common-mode condition and the node X could be seen as a virtual ground in differential-mode. As above mentioned, there is noise contribution due to the bulk resistance of MOS transistor. Therefore, the junction leakage current and noise figure could be reduced effectively by connecting the resistors R_{SB} [20]. Fig. 2 shows the simulated noise analysis about the resistor R_{SB} dimension of the proposed paper. When R_{SB} is designed to be KΩ level so that the noise contribution from body resistance could be minimized.

B. INPUT IMPEDANCE MATCHING NETWORK

Fig. 3 presents the differential CS amplifier topology including input impedance matching network. The C_{gs1} and C_{gs2} are the designed capacitors including the parasitical capacitance between gate and source terminals. Hence, the source degeneration differential inductor L_S and the C_{gs1} and C_{gs2} would form a real part impedance with MOS conductance $g_m = g_{m1} = g_{m2}$, where the gate inductors L_{G1} and L_{G2} provide a imaginary part reactance to make the resonant frequency locate at 2.45 GHz. The transfer function of input impedance is expressed as follows:

$$Z_{in}(s) = \frac{1}{sC_{in}} + R_G \parallel \left[\frac{s^2 C_{gs}\left(\frac{L_S}{2} + L_G\right) + s g_m \frac{L_S}{2} + 1}{sC_{gs}}\right] \tag{4}$$

where $C_{in} = C_{in1} = C_{in2}$, $C_{gs} = C_{gs1} = C_{gs2}$, $L_G = L_{G1} = L_{G2}$, and R_G is a KΩ level resistor which is much larger than 100Ω differential characteristic impedance Z_S. Therefore, the input impedance could be expressed approximately as follows:

$$\begin{aligned} Z_{in}(s) &\approx \frac{1}{sC_{in}} + \frac{s^2 + s\frac{g_m}{C_{gs}} \cdot \frac{L_S/2}{(L_S/2+L_G)} + \frac{1}{C_{gs}(L_S/2+L_G)}}{\frac{s}{L_S/2+L_G}} \\ &= \frac{1}{sC_{in}} + \frac{s^2 + s\frac{\omega_{oi}}{Q_{in}} + \omega_{oi}^2}{\frac{s}{L_S/2+L_G}} \end{aligned} \tag{5}$$

where

$$\begin{cases} Q_{in} = \dfrac{2}{g_m L_S} \cdot \sqrt{C_{gs}\left(\dfrac{L_S}{2} + L_G\right)} \\ \omega_{oi} = \dfrac{1}{\sqrt{C_{gs}\left(\dfrac{L_S}{2} + L_G\right)}} \end{cases} \tag{6}$$

substituting $s = j\omega$ into (5), the input impedance transfer function could be expressed as real part and the imaginary part respectively as follows:

$$\begin{cases} R\{Z_{in}\} = \dfrac{g_m}{C_{gs}} \cdot \dfrac{L_S}{2} = \omega_T \cdot \dfrac{L_S}{2} \\ X\{Z_{in}\} = \dfrac{C_{gs} + C_{in}\left[1 - \omega^2 C_{gs}\left(\frac{L_S}{2} + L_G\right)\right]}{j\omega C_{in} C_{gs}} \end{cases} \tag{7}$$

Therefore, the imaginary part $X\{Z_{in}\}$ is equal to $1/(j\omega_{oi}C_{in})$ when $\omega = \omega_{oi}$. Additionally, C_{in} is a pF level capacitor which

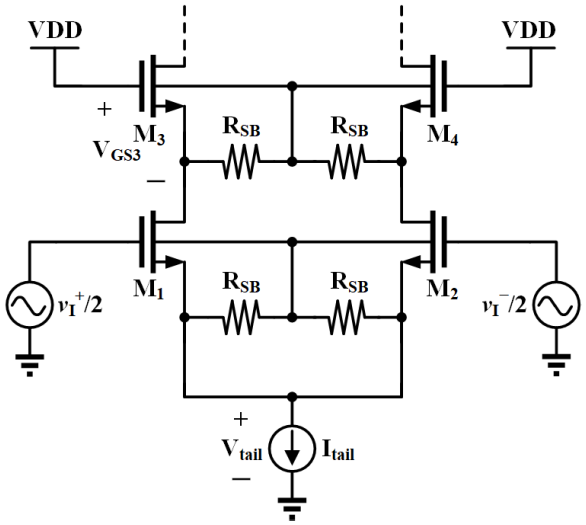

FIGURE 4. The differential CS cascode amplifier topology schematic.

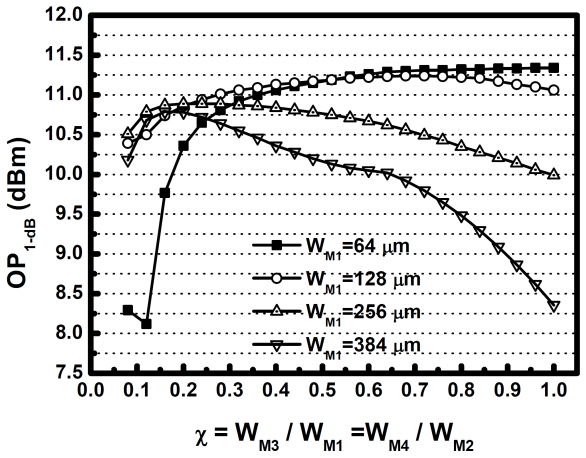

FIGURE 5. The OP_{1-dB} analysis of cascode transistors width ratio.

is almost a very small impedance in high frequency circuit. Hence, the signal path through C_{in} could be seen as a short circuit so that the input impedance is approximately purely resistive at the middle frequency 2.45 GHz. The real part of Z_{in} is shown as $R\{Z_{in}\}$ in (6). By substituting the design parameters of $g_m = 21.8$ mS, $C_{gs} = 400$ fF, and $L_S = 4.12$ nH into (6), the input impedance $Z_{in} = 112.3\Omega$. Hence, the differential half-circuit input impedance 56.15Ω was obtained, which is close to the characteristic impedance 50Ω.

C. CASCODE TOPOLOGY AND LINEARITY DESIGN

Fig. 4 shows the differential CS cascode amplifier topology schematic. Comparing with the single-stage CS amplifier, the cascode amplifier could optimize the gain-bandwidth product(GBW) by shrinking the dimension of M_3 and M_4 [6]. However, in order to keep all of the transistors to operate at saturation region that must conform the characteristic function conditions as follows:

$$\begin{cases} v_{DS} \geq v_{GS} - V_t \\ i_D = \dfrac{1}{2} k_n' \cdot \dfrac{W}{L} \cdot (v_{GS} - V_t)^2 \end{cases} \tag{8}$$

Hence, for example, the V_{GS3} increases while W_{M3} is reduced under the conditions of constant tail current source I_{tail}. However, the DC operation condition of cascode amplifier in Fig. 4 is as follows:

$$V_{DS1} = V_{DD} - V_{tail} - V_{GS3} \tag{9}$$

Here, V_{tail} is the voltage produced by current source I_{tail}, and $V_{DD} - V_{tail}$ is a constant. Therefore, V_{DS1} must decrease while V_{GS3} raises. It means that the headroom of V_{DS1} is easily compressed to make M_1 enter the triode region while large signal inputs the cascode LNA. Therefore, the DC operation conditions and the dimension of cascode transistors influence seriously the linearity performance of amplifier. Fig. 5 shows the simulated CS cascode LNA OP_{1-dB} analysis results versus the ratio χ of transistors dimension in Fig. 4. According to the analysis results, if χ is smaller than 0.2, the linearity would decrease. It is because that M_1 and M_2 enter triode region. However, when the width of M_1 and M_2 is larger, the linearity also reduces intensely under the same conditions of ratio of χ and current. It is because that $V_{DS3} + V_{DS1} + V_{tail} \approx V_{DD}$ in this proposed LNA, and there is a dc voltage trade-off between V_{DS1} and V_{DS3}. Oppositely, the headroom of V_{DS3} would be compressed to make linearity decrease while the width of M_3 increases. Especially, the dimension of M_1 and M_2 is larger, the attenuation of linearity is more obvious. From the results of Fig. 5, we choose $W_{M1} = 128$ μm because that the linearity is more stable than other conditions, where $\chi = 0.89$ and $W_{M3} = 114$ μm, so do M_2 and M_4. The channel length of all NMOS transistors is 60 nm.

D. FREQUENCY RESPONSE OF NOISE

Fig. 6 presents the equivalent circuit of the proposed differential CS cascode LNA half-circuit including the input impedance matching network in Fig. 4 for noise calculation. In this section, the gain of LNA is assumed to be large enough at resonant frequency, and all of the transistors are designed in saturation region. Hence, the noise contribution of the resonator loading can be disregarded. The noise factor F_{LNA} of the LNA is expressed as follows, (10)–(15), as shown at the bottom of the next page, where $i_{n,out}$ represents the total output noise current composed by the noise current components i_{so}, i_{lgo}, i_{rgo}, i_{lso}, i_{nd1o}, and i_{nd3o}, which are produced by the noise sources e_{Rs}, e_{lg}, e_{rg}, e_{ls}, i_{nd1}, and i_{nd3}, respectively. These noise generators are from the parasitical resistance R_{lg}, R_{rg}, and R_{ls} of the circuit components as well as channel thermal noise of transistors. $F_{M1} = \overline{|i_{nd1o}^2|}/\overline{|i_{so}^2|}$ and $F_{M3} = \overline{|i_{nd3o}^2|}/\overline{|i_{so}^2|}$ represent the noise factor contributions of i_{nd1o} and i_{nd3o} corresponding to the transistors.

By analyzing the output noise current of the LNA of Fig. 6. $\overline{|i_{so}^2|}$, $\overline{|i_{nd1o}^2|}$, and $\overline{|i_{nd3o}^2|}$ could be obtained as the top of this page, where α_1 and α_3 represent the ratio of g_m to g_{d0} of M_1 and M_3, $\omega_{T1} = g_{m1}/C_{gs1}$, and $\omega_{T3} = g_{m3}/C_{gs3}$, respectively.

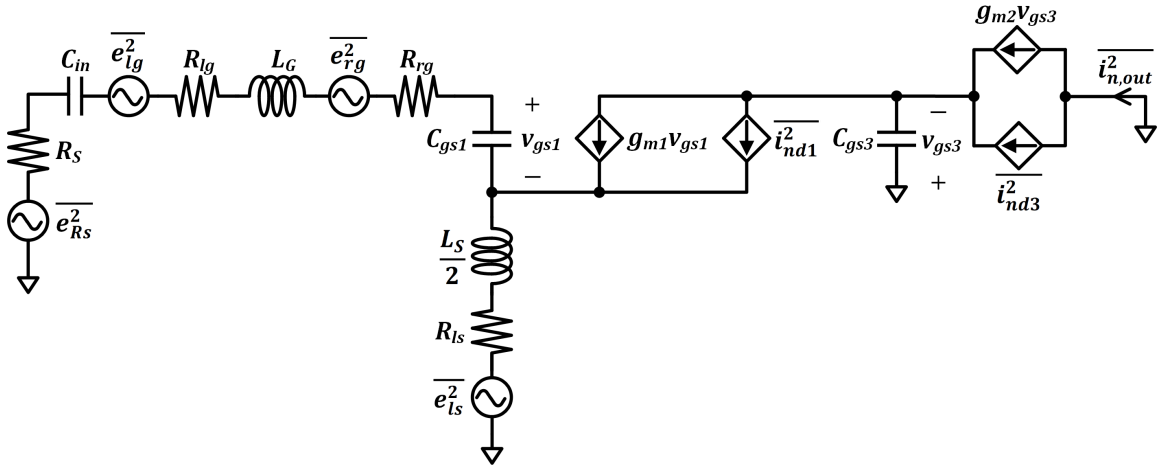

FIGURE 6. The equivalent circuit of the proposed differential CS cascode LNA half-circuit for noise calculation.

The g_{d0} is the drain−source conductance of MOS at $V_{DS} = 0$. Substituting (11)−(13) into (10), F_{M1} and F_{M3} could be derived as (14)−(15). Finally, F_{LNA} could be obtained by calculating the parameters.

E. PROPOSED QUADRUPLE-BAND COMMON-SOURCE CASCODE LNA

Fig. 7 depicts the proposed quadruple-band LNA schematic including the LC-tank loading with the capacitance array of band-switching by body self-biasing technique, where the LC-tank loading impedance provides four resonant frequencies by switching the capacitance array. The loading resonant frequency f_{res} is expressed as follows:

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{load} \cdot \left(C_{load} + C_{array}\right)}} \tag{16}$$

where C_{array} is the equivalent capacitance of the loading capacitance array, and the function is represented as follows:

$$C_{array} = \begin{cases} 0; & when\ SW_0 = off,\ SW_1 = off \\ C_L; & when\ SW_0 = on,\ SW_1 = off \\ 2C_L; & when\ SW_0 = off,\ SW_1 = on \\ 3C_L; & when\ SW_0 = on,\ SW_1 = on \end{cases} \tag{17}$$

$$\begin{aligned} F_{LNA} &= \frac{\overline{\left|i_{n,out}^2\right|}}{\overline{\left|i_{so}^2\right|}} \\ &\approx \frac{\overline{\left|i_{so} + i_{lgo} + i_{rgo} + i_{lso} + i_{nd1o} + i_{nd3o}\right|^2}}{\overline{\left|i_{so}^2\right|}} \\ &= 1 + \frac{\overline{\left|i_{lgo}^2\right|}}{\overline{\left|i_{so}^2\right|}} + \frac{\overline{\left|i_{rgo}^2\right|}}{\overline{\left|i_{so}^2\right|}} + \frac{\overline{\left|i_{lso}^2\right|}}{\overline{\left|i_{so}^2\right|}} + \frac{\overline{\left|i_{nd1o}^2\right|}}{\overline{\left|i_{so}^2\right|}} + \frac{\overline{\left|i_{nd3o}^2\right|}}{\overline{\left|i_{so}^2\right|}} \\ &= 1 + \frac{R_{lg} + R_{rg} + R_{ls}}{R_S} + F_{M1} + F_{M3} \end{aligned} \tag{10}$$

$$\overline{\left|i_{so}^2\right|} = 4KTR_S\Delta f \cdot \left| \frac{g_{m1} \cdot \omega_{T3} \cdot C_{in}}{(s + \omega_{T3})\left[s^2\left(\frac{L_S}{2} + L_G\right)C_{in}C_{gs1} + s \cdot \left(\frac{\omega_{T1}L_S}{2} + R_S\right)C_{in}C_{gs1} + C_{in} + C_{gs1}\right]} \right|^2 \tag{11}$$

$$\overline{\left|i_{nd1o}^2\right|} = 4KT\frac{\gamma}{\alpha_1}g_{m1}\Delta f \cdot \left| \frac{\omega_{T3}}{s + \omega_{T3}} \right|^2 \tag{12}$$

$$\overline{\left|i_{nd3o}^2\right|} = 4KT\frac{\gamma}{\alpha_3}g_{m3}\Delta f \cdot \left| \frac{s}{s + \omega_{T3}} \right|^2 \tag{13}$$

$$F_{M1} = \frac{\gamma}{g_{m1}\alpha_1 R_S C_{in}^2} \cdot \left| s^2\left(\frac{L_S}{2} + L_G\right)C_{in}C_{gs1} + s \cdot \left(\frac{\omega_{T1}L_S}{2} + R_S\right)C_{in}C_{gs1} + C_{in} + C_{gs1} \right|^2 \tag{14}$$

$$F_{M3} = \frac{\gamma}{g_{m3}\alpha_3 R_S C_{in}^2} \cdot \left| \left(\frac{sC_{gs3}}{g_{m1}}\right) \cdot \left[s^2\left(\frac{L_S}{2} + L_G\right)C_{in}C_{gs1} + s \cdot \left(\frac{\omega_{T1}L_S}{2} + R_S\right)C_{in}C_{gs1} + C_{in} + C_{gs1}\right] \right|^2 \tag{15}$$

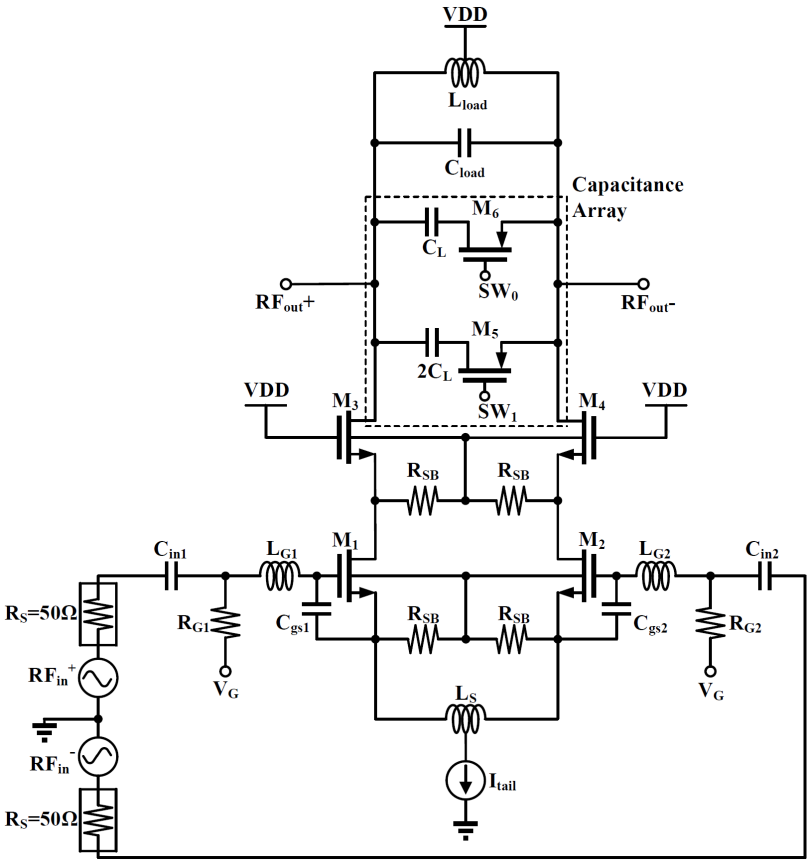

FIGURE 7. The proposed quadruple-band common-source cascode LNA schematic.

The capacitance array utilizes binary controlling technique to alter the loading equivalent capacitance. The method of two switch controlling could be used to realize four resonant frequencies, where the switches are applied by deep N-well (DNW) RF PMOS device. The PMOS switches of M_5 and M_6 are conducted by supplying the gate voltage between 0 V or 1.25 V. Therefore, the resonant frequency will follow a difference of capacitance C_L while the capacitance switch is adjusted step by step. The quadruple frequencies is realized from (16)−(17) in this proposed LNA. In addition, we also need to select the suitable dimension of loading inductor L_{load} with the maximum Q-value at the middle resonant frequency 2.4 GHz in order to maximize the equivalent loading resistance and voltage gain of the LNA [27]. It is because that the spiral inductor is not ideal at present CMOS process technology. Therefore, we found the loading inductor L_{load} size, where the inner radius = 90 μm, coil turns = 4, line width = 8 μm, and the inductance value = 6.13 nH. Then, the capacitance C_{load} = 371.9 fF, and C_L = 49.84 fF.

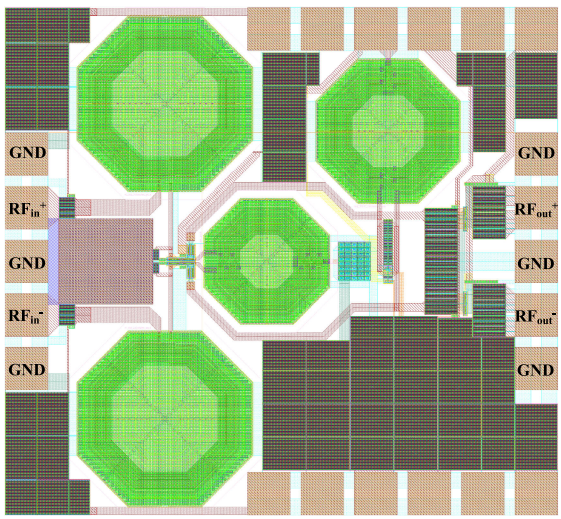

FIGURE 8. The layout graph of the proposed quadruple-band LNA.

III. SIMULATION RESULTS

The proposed LNA was designed in a 55 nm RFCMOS process. Fig. 8 depicts the layout graph including the buffer for measurement. The area of layout occupies 0.83 mm^2 excluding pads. The testing phase considers on-wafer measurements using ground-signal-ground-signal-ground (GSGSG) on differential input/output and DC probes. Fig. 9−12 present the post-simulation results of the proposed LNA. Fig. 9 presents the post-simulated $|S_{21}|$ in dB. The post-simulated maximum $|S_{21}|$ of the proposed LNA achieves 16.8, 16.63, 16.78, and 16.39 dB, which locate at 2.35, 2.4, 2.45, and 2.55 GHz, respectively. Fig. 10 shows the post-simulated $|S_{11}|$ of the proposed LNA, which is under −12.5 dB during 2.35−2.55 GHz. Fig. 11 presents the calculated and

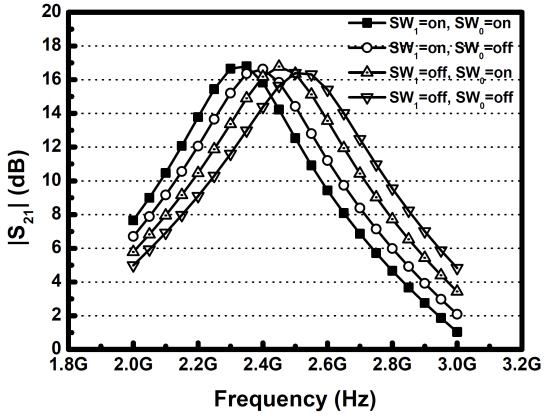

FIGURE 9. The post-simulated $|S_{21}|$ of the proposed quadruple-band LNA.

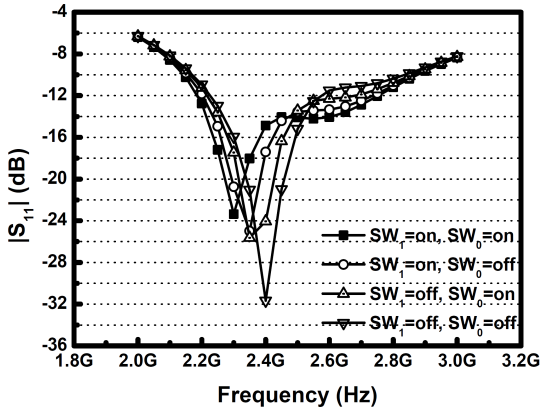

FIGURE 10. The post-simulated $|S_{11}|$ of the proposed quadruple-band LNA.

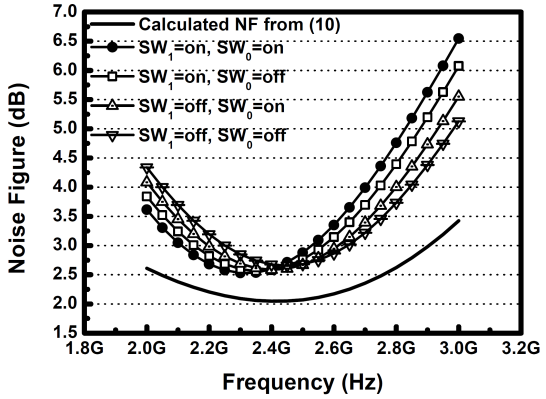

FIGURE 11. The calculated and post-simulated noise figures of the proposed quadruple-band LNA.

post-simulated NFs of the LNA, where the NFs of the four switch modes are 2.54, 2.58, 2.6, and 2.75 dB at 2.35, 2.4, 2.45, and 2.55 GHz, respectively. There is a difference about 0.5 dB of NF between calculation and post-simulation due to the parasitical resistance in signal and ground path of the post-layout model. The frequency response of NF during 2.35−2.55 GHz is more similar between calculation and post-simulation due to the enough gain. Fig. 12 shows the post-simulated input referred 1-dB compression point

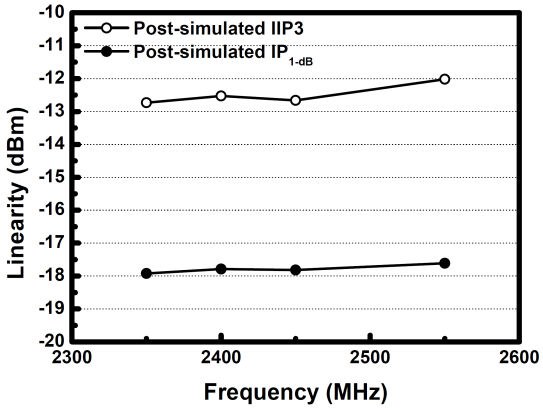

FIGURE 12. The post-simulated IP_{1-dB} and IIP3 of the proposed quadruple-band LNA.

TABLE 1. Performance summary of the proposed Quadruple-Band LNA.

Cap. Array Function	Operation Frequency	$\|S_{21}\|$ (dB)	$\|S_{11}\|$ (dB)	NF (dB)	IP_{1-dB} (dBm)	IIP3 (dBm)
SW_1=on, SW_0=on	2.35 GHz	16.8	−18.04	2.54	−17.92	−12.73
SW_1=on, SW_0=off	2.4 GHz	16.63	−17.41	2.58	−17.79	−12.53
SW_1=off, SW_0=on	2.45 GHz	16.78	−16.37	2.6	−17.82	−12.66
SW_1=off, SW_0=off	2.55 GHz	16.39	−12.53	2.75	−17.61	−12.02
Current Dissipation	3 mA @ 1.25 V					

(IP_{1-dB}) and third-order intermodulation characteristics of the proposed LNA including output buffer with two-tone frequencies of 2350±20 MHz, 2400±20 MHz, 2450±20 MHz, and 2550±20 MHz, respectively. The post-simulated IP_{1-dB} points are −17.92 dBm at 2.35 GHz, −17.79 dBm at 2.4 GHz, −17.82 dBm at 2.45 GHz, and −17.61 dBm at 2.55 GHz, respectively. The post-simulated input-referred third-order intercept points (IIP3) are −12.73 dBm at 2.35 GHz, −12.53 dBm at 2.4 GHz, −12.66 dBm at 2.45 GHz, and −12.02 dBm at 2.55 GHz, respectively. In this post-simulated case, it is applied by 1.25 V supply voltage, and dissipates 3 mA. Summing up the above results, the performance summary of each switched band in this proposed LNA is presented as Table 1.

Table 2 summarizes the performances of the recently published dual-band, triple-band, and quadruple-band LNAs. The figure of merit (*FoM*) factor listed in the last row represents the comprehensive performance of the references. Here, the *FoM* is expressed as follows:

$$FoM = \frac{|S_{21}|_{(Abs.)} \cdot IIP3_{(mW)}}{P_{diss(mW)} \cdot (F-1)_{(Abs.)}} \quad (18)$$

where $|S_{21}|_{(Abs.)}$ represents the average voltage gain of the referred LNA in magnitude, and $(F-1)_{(Abs.)}$ represents the excess noise factor in magnitude. From (18), the *FoM* is normalized to the voltage gain, IIP3, power consumption, and

TABLE 2. Performance summary of the developed Dual-Band LNAs and Tri-Band LNAs.

Reference	Technology	Band-Selection Topology	Frequency (GHz)	$\|S_{21}\|$ (dB)	$\|S_{11}\|$ (dB)	NF (dB)	IIP3 (dBm)	Power Consumption (mW)	FoM
[1] MWCL 2010[c]	CMOS 90nm	Dual Band	1.8	15	-15	4	+11	28	1.68
			2.0	16	-15	3.5	+11		2.29
[3] TCSI 2012[b]	CMOS 0.13μm	Dual Band	2.45	13	-12.62	1.76	-4.3^{c}	2.79 w/o Buff.[c]	1.185
			6	9	-4.8	5.3	-5.6^{c}		0.116
[5] IEEE ACCESS 2017[a]	CMOS 0.13μm	Dual Band	2.4	19.3	−16.8	3.2	−20.1	2.4	0.034
			5.2	17.5	−19.4	3.3	−18.1		0.041
[6] CSSP 2017[b]	CMOS 0.18μm	Dual Band	4	13.74	−16.91	4	-10^{c}	9.1 w/o Buff.[c]	0.035
			8.4	13.23	−10.74	5.62	-12^{c}		0.012
[7] TMTT 2017[b]	CMOS 0.13μm	Dual Band	3	22	−15.4	1.75	-12.5^{c}	7.2 w/o Buff.[c]	0.197
			5	27	−13.5	2.1	-13.8^{c}	3.6 w/o Buff.[c]	0.42
[8] TCSI 2018[b]	SiGe 0.18μm	Dual Band	21.5	24.5	−11	3.9	-14.1^{c}	73.8[c]	0.006
			36	24	−12	3.9	-16.1^{c}		0.004
[10] TCSI 2019[c]	CMOS 0.18μm	Dual Band	2.4	9.7	−12	1.6	+2	11.7	0.92
			5	11	−19	2.6	+5		1.17
[11] TCSII 2008 TC LNA[b]	CMOS 0.13μm	Triple Band	4.9	11	−35	3.8	-2.2^{c}	1.02[c]	1.499
			5.2	12.5	−18.5	3.45	-5.6^{c}		0.937
			5.8	15.7	−18	3.25	-6.7^{c}		1.149
[11] TCSII 2008 TI LNA[b]	CMOS 0.13μm	Triple Band	4.9	14	−20	2.35	-1.5^{c}	5.28[c]	0.936
			5.2	15	−24.5	2.2	-3.4^{c}		0.737
			5.8	17	−25.5	2.05	-5.9^{c}		0.571
[12] CSSP 2017[b]	CMOS 0.18μm	Triple Band	2.4	12.47	−22.53	4.1	-7^{c}	3.6 w/o Buff.[c]	0.149
			5.2	15.78	−19.87	4.39	-16^{c}		0.024
			5.8	15.34	−20.11	4.51	-16^{c}		0.022
[13] TMTT 2013[b]	CMOS 0.13μm	Triple Band	2.8	17	−20	1.95	-4^{c}	6.4 w/o Buff.[c]	0.776
			3.3	14.2	−9.7	2.8	-2^{c}		0.559
			4.6	14.2	−12	3.2	-3.2^{c}		0.353
[15] TMTT 2013[b]	SiGe 0.18μm	Triple Band	13.5	21.2	−10.5	3.3	-13.5^{c}	36[c]	0.013
			24	21.8	−14.5	3.1	-17.1^{c}		0.006
			35	19.7	−13.8	3.7	-16.1^{c}		0.005
[16] JSSC 2014[c]	CMOS 45nm SOI	Quadruple Band	1.91	15.8[d]	N.A.	5	−6	6 w/o Buff.	0.12
			2.31	14.8[d]		5	−5.2		0.13
			2.6	14.2[d]		5	−4.8		0.13
			3.41	14.6[d]		2.6	−6.5		0.24
[28] TMTT 2016[c]	GaAs 0.15μm	Dual Band	2.4	20	−10	2.2	−8.5	33	0.064
			5	15	−7	2	−4		0.12
This work[b]	**CMOS 55nm**	**Quadruple Band**	**2.35**	**16.8**	**−18.04**	**2.54**	**−12.73**	**3.75 w/o Buff.**	**0.124**
			2.4	**16.63**	**−17.41**	**2.58**	**−12.53**		**0.124**
			2.45	**16.78**	**−16.37**	**2.6**	**−12.66**		**0.122**
			2.55	**16.39**	**−12.53**	**2.75**	**−12.02**		**0.125**

[a] Pre-Simulated Results
[b] Post-Simulated Results
[c] Measured Results
[d] Voltage Gain

noise factor, which is introduced to reveal the importance of the proposed quadruple-band LNA.

Comparing with other published multi-band LNAs, the proposed LNA achieves good *FoMs* in the four bands. Although the cross-coupled CG LNA [1] achieves excellent linearity, it dissipates up to 24 mA DC current in the output buffer to maintain the highest linear output signal power. From [3], a very high *FoM* is shown in both band mode, however, the gain variation of $|S_{21}|$ is up to 9.5 dB due to the low equivalent parallel resistance of the resonator load when the LNA is switched to low-band mode. Although [10] performs the excellent NF using integrated passive device (IPD) configuration, the area of the dual-band LNA occupies up to 3.9 mm^2. It means that the cost would increase very much. Hence, the proposed LNA presents a good *FoM* including the comprehensive consideration of gain, noise figure, and power consumption to be suitable for multi-band SDR application.

IV. CONCLUSION

This paper presented a 2.35, 2.4, 2.45, and 2.55 GHz quadruple-band differential CS cascode CMOS LNA with a single band-selection switch. A body self-biasing technique was employed to minimize the noise contribution due to the transconductance degradation caused by the body-effect. In other words, the better noise performance could be achieved with less current. In addition, the resistor connected between the terminals of source and body of MOS could block effectively the junction leakage as well as noise current due to bulk resistance. The linearity of the CS cascode amplifier could be optimized by analyzing the DC characteristics. It is helpful for circuit designers to find the most suitable MOS dimension of the cascode amplifier configuration by utilizing the proposed optimization technique. To realize the multi-band LNA for SDR application, the binary switch of capacitor array was utilized at the loading resonator of the proposed LNA. Hence, by the binary switch method,

the capacitor array could be used to plan the required communication band more efficiently.

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