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A Voltage-Balancer-Based Cascaded DC–DC Converter With a Novel Power Feedforward Control for the Medium-Voltage DC Grid Interface of Photovoltaic Systems

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ABSTRACT DC–DC converters with output-series cascaded submodules (SMs) are required for the medium-voltage direct current (MVDC) grid interface of photovoltaic (PV) systems. However, the mismatched power of PV arrays can cause an imbalance among the output voltages of SMs. In order to address this problem, in this paper, a multi-port cascaded DC–DC converter is established on the basis of a voltage balancer (VB) with a novel power feedforward voltage-balancing control strategy. The converter has multiple input terminals for the PV arrays and an output terminal connected to the MVDC grid. The differential power is regulated from one SM to another through the VB, ensuring that the SM output voltages are equalized. Simulation and experimental results suggest that the proposed converter has an excellent voltage-balancing capacity and dynamic performance.

INDEX TERMS Photovoltaic, voltage balancing, power feedforward control, MVDC, power mismatch.

I. INTRODUCTION

In recent years, photovoltaic (PV) power technology has attracted a lot of attention due to its sustainable-energy features. Although the majority of PV systems adopt AC methods for energy collection and transmission [1]–[4], DC means have better stability and lower power losses [5], [6]. In medium-voltage distribution networks, a DC–DC converter is necessary to collect the power generated by PV panels [7]. In particular, a high step-up ratio DC–DC converter is required because the majority of commercial PV modules are designed to withstand no more than 1 kV between the active part and the grounded frame [5], [6], and the voltage of the DC bus is usually much higher than this value. This inconsistency can be addressed by using cascaded multiple submodules (SMs) to achieve a high voltage output, of which there are three main types: input-independent output-series (IIOS) type, low-voltage bus based (LVBB) type, and two-stage conversion (TSC) type.

The structure of the IIOS type [8]–[11] is shown in Fig. 1(a). This type has a simple structure as well as the benefits of modularity and low associated costs. However, it has the weakness of PV power mismatch when employed in DC systems. In particular, the sum of the output voltages of cascaded SMs is restricted by the DC grid, whereas the SMs are responsible for controlling the maximum power point tracking (MPPT). Since the output currents for SMs are identical because of the cascaded structure, their output voltages are positively related to the power they transfer. The power mismatch of PV installations can be attributed to a number of factors, such as varying irradiance conditions in the distributed network, uneven array shading, dirt accumulation, and manufacturing processes [11]. In essence, power mismatch means that the SMs that transfer excessive amounts of energy receive high voltages (and vice versa), causing an imbalance among the voltages. Obviously, this is contrary to the standardized multi-module design of the

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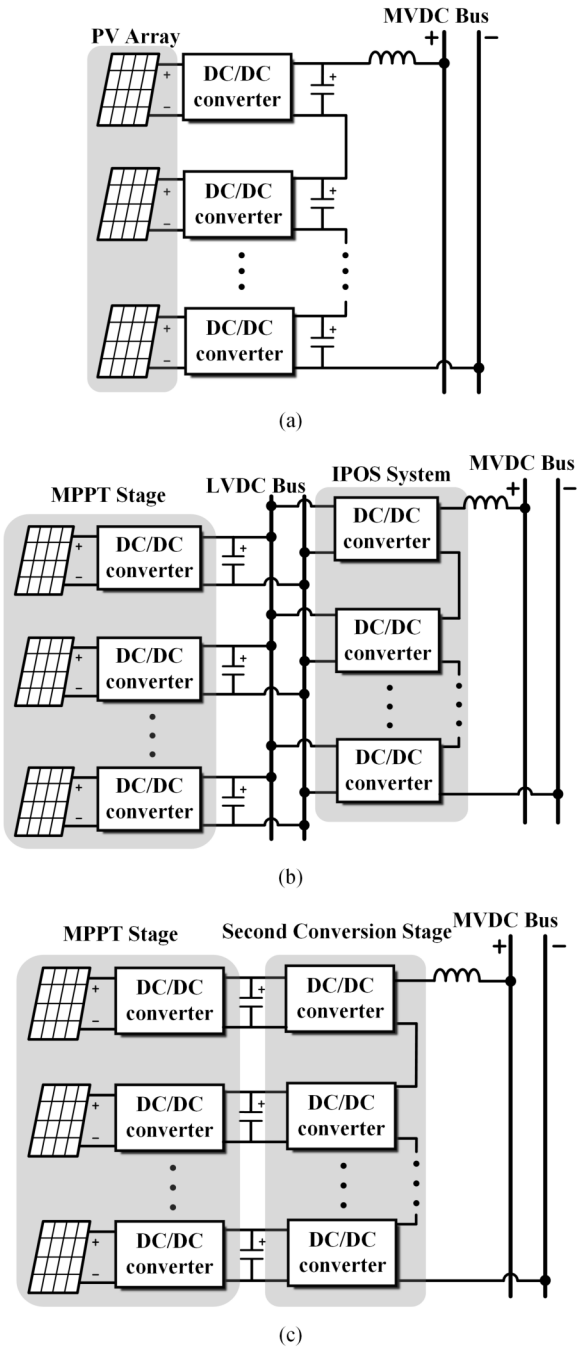

FIGURE 1. Main topologies of multi-port cascaded converter for the MVDC grid interface of a PV system: (a) IIOS type, (b) LVBB type, and (c) TSC type.

converter in question. In order to address this problem, [9], [10] propose the concept of global power optimization and its corresponding control strategy, wherein the voltage stability is guaranteed by limiting the output power of PV arrays.

The LVBB type shown in Fig. 1 (b) employs a low-voltage DC bus to collect the PV power, completing the energy conversion between the low-voltage DC bus and the medium-voltage DC bus with an input-parallel output-series (IPOS) system [12], [13]. In this way, the power mismatch problem can be solved. However, the input currents and output voltages of the SMs would still be different due to the difference in parameters of the switches and the passive components [13]. Furthermore, the majority of current-sharing or voltage-balancing control strategies of modularized converters are proposed for input-series output-parallel (ISOP) systems [14], [15], which cannot be directly used in IPOS systems. Additionally, distributed MPPT converters are needed to connect the PV arrays with the low-voltage DC bus, which is not conducive to the unified control of the system. In order to solve these problems, a three-port converter (TPC)-based distributed DC grid-connected PV system is proposed by [6], which solves the power mismatch problem with the help of a low-voltage DC bus. Herein, extra MPPT converters are not required because MPPT and SM output voltage balancing are both achieved by the TPC, which, in turn, reduces the associated costs. Unfortunately, the low-voltage DC bus reduces system reliability, which is a common problem for LVBB-type topologies.

The TSC type shown in Fig. 1 (c) adds a second conversion stage to the foundation of the IIOS type, which, in turn, widens the voltage-regulation range. References [16], [17] employ a DC–DC modular multilevel converter (MMC) as the second conversion stage. The duty cycles of the SMs in the MMC are regulated in order to ensure that the output voltage is balanced in the MPPT stage. Accordingly, the power mismatch problem is addressed to a certain degree, but the capacity of MMC for voltage balancing is limited. Similarly, a quasi Z-source converter (QZSC) is employed as the second conversion stage by [18], [19] in order to address the power mismatch problem. Indeed, the QZSC has a technically superior voltage-balancing ability compared with the MMC; however, it requires a greater number of passive components.

The key factor in solving the power mismatch problem is attaining a voltage balance, which has been explored by a number of researchers for cascaded systems. Reference [15] establishes a method for ISOP systems by regulating the peak current, which is effective when input voltages have a wide range of values or when the equivalent input capacitances are severely mismatched. According to [20], an equalizing strategy based on a master–slave structure sacrifices balancing accuracy for controlling simplicity in the ISOP system. Moreover, [21] proposes a way to equalize the voltages with the aid of a sliding-mode control, which effectively addresses unbalanced voltage resulting from the transformer leakage inductance mismatch of dual active bridge topology. In general, many means have been employed to achieve capacitor voltage balancing with respect to MMCs, such as the sorting method [22] and power feedforward control [23]. Unfortunately, voltage imbalances manifest differently according to the system in question; for instance, in MMC topology, non-ideal drive pulse and stray parameters of varied devices result in a voltage imbalance [24], but, in PV IIOS systems, differential input power is responsible. Accordingly, the aforementioned methods cannot be applied to the PV interface system directly.

Another alternative to solve voltage imbalance is to harness a voltage balancer (VB). The concept of a VB has been used by a number of researchers as a power differential processing converter in order to address the P–V curve mismatch problem for the PV array [25]–[28]. A VB ensures that the MPPT for series-connected PV arrays under partial-shadow conditions; however, it is limited by insulation technology, and accordingly, it cannot be applied to high- and mid-voltage-level DC grids. In addition, VB has also been used to achieve balanced voltages in series-connected battery systems [29], [30]. Modularized VBs and distributed-control methods ensure that entire systems are integrated. Reference [31] also uses VBs as current diverters to balance the voltages of cascaded SMs; however, only an open-loop constant duty-cycle voltage-control strategy is adopted, which results in low control efficiency, especially for applications where a large inductance and a large number of SMs are required. In this paper, a VB-based multi-port cascaded DC–DC converter for the medium-voltage direct current (MVDC) grid interface of a PV system is introduced, which guarantees the output voltage balance of the cascaded SMs. In doing so, a novel power feedforward voltage-balancing control strategy is proposed, which has a rapid dynamic response. The converter has multiple input terminals for the PV arrays, and the output terminal is connected to the MVDC grid. Compared with existing control strategies, the proposed voltage-balancing control method is more suitable with respect to addressing the voltage imbalances caused by differential PV powers. In particular, in contrast to the method used by [31], it can eliminate static errors and reduce current surges. Additionally, it features a better dynamic performance than a normal closed-loop method.

The remainder of this paper is structured as follows: Section II introduces the configuration of the VB-based cascaded DC–DC converter and its operating principles; Section III illustrates the novel power feedforward voltage-balancing control strategy in detail; circuit design and efficiency analysis are presented in Sections IV and V, respectively, followed by the verification of the simulation and experimental studies in Section VI, with conclusions drawn thereafter in Section VII.

II. SYSTEM CONFIGURATION AND ANALYSIS

A. CONFIGURATION OF THE VB-BASED CASCADED DC–DC CONVERTER

The configuration of the VB-based multi-port DC–DC converter is shown in Fig. 2. PV arrays are interfaced with the isolated DC–DC converters in order to independently achieve MPPT. The isolated DC–DC converters ensure electrical isolation among the PV arrays as well as between the PV arrays and the voltage-balancing stage, which makes it easy to design the insulation parameters. The output ports of the SMs are connected in series to a MVDC bus through the filter inductor. VBs, through which the mismatched power can be transferred, are placed and connected between every two adjacent SMs, thereby addressing the unbalanced capacitor voltages with respect to their outputs.

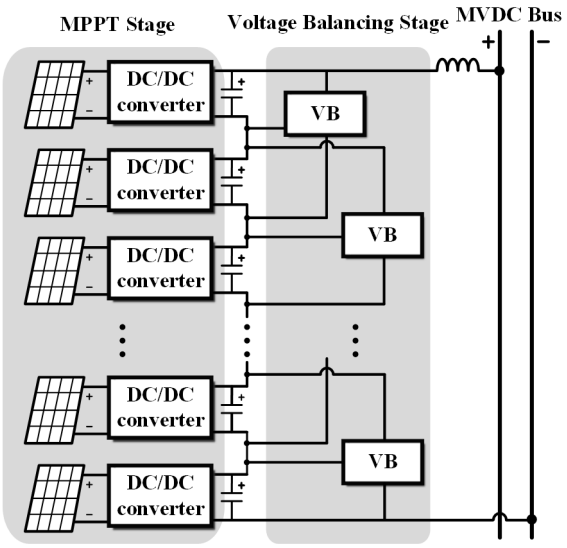

FIGURE 2. The configuration of the VB-based multi-port DC–DC converter.

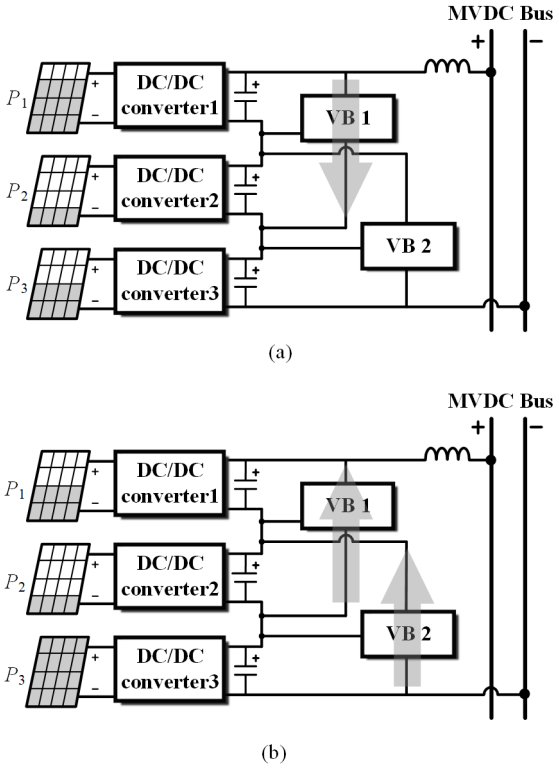

FIGURE 3. Power flow of VBs: (a) $P_1 = 300$ W, $P_2 = 100$ W, and $P_3 = 200$ W; (b) $P_1 = 200$ W, $P_2 = 100$ W, and $P_3 = 400$ W.

Despite the fact that a single VB is only linked to the two adjacent converter modules, the direction of the transferred mismatched power concerns the output power for all the SMs. Each VB module can divide the converters into two groups according to location in the system. If the average

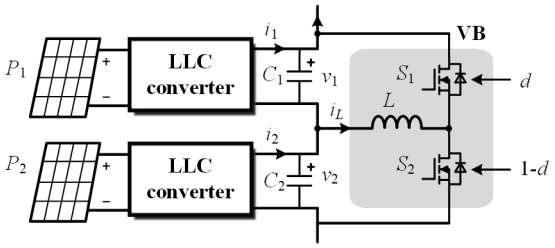

FIGURE 4. Detailed structure of a single VB.

power of the top group surpasses that of the bottom group, the mismatched power moves downwards through the VB; otherwise, it moves upwards. If the average power of the two groups is equal, then there will be no mismatched power flow. Fig. 3 illustrates specific examples for the transferred directions in different cases of a three-SM cascaded converter. P_i ($i = 1, 2, 3$) is the output power of the converters at the maximum power point. In Fig. 3 (a), the relational expressions are assumed as

$$\begin{cases} P_1 > \dfrac{1}{2}(P_2 + P_3) \\ \dfrac{1}{2}(P_1 + P_2) = P_3 \end{cases} \tag{1}$$

according to which it can be known that VB 1 transfers mismatched power downward and that there is no power transferred through VB 2.

In contrast, in Fig. 3 (b), it is assumed that

$$\begin{cases} P_1 < \dfrac{1}{2}(P_2 + P_3) \\ \dfrac{1}{2}(P_1 + P_2) < P_3 \end{cases} \tag{2}$$

Accordingly, both VB 1 and VB 2 transfer power upwards, thereby balancing the power and output voltages of the SMs.

B. OPERATING PRINCIPLES OF VB

There are many options for the isolated DC–DC converters in Fig. 2, such as a flyback converter, a full-bridge circuit, and an LLC resonant converter. Among all of them, the LLC resonant converter features the ability of soft-switching and is used in a number of applications. Thus, it is adopted in this paper. The working principle of the LLC converter has been outlined by [32], so it will not be discussed here.

The detailed structure of a single VB along with two MPPT converters is shown in Fig. 4. With two switches (S_1 and S_2) turned on in complementary, the inductor (L) absorbs energy from one converter as the load and supplies it to the other as the source. The capacitors (C_1 and C_2) are the output filters of the two adjacent converters linked to the VB. The inductor current (i_L) passes through C_1 when S_1 is turned on, with the voltage of the inductor equal to $-v_1$; moreover, i_L passes through C_2 when S_2 is turned on, with the voltage of the inductor equal to v_2. Supposing that the duty cycles of S_1 and S_2 are d and $1 - d$, respectively, the average value of

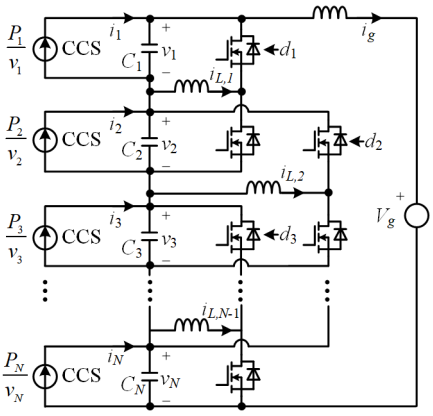

FIGURE 5. The equivalent circuit of the VB-based multi-port cascaded converter.

the inductor voltage within one cycle can be expressed as

$$v_L = -v_1 d + v_2(1 - d). \tag{3}$$

Accordingly, i_L can be regulated by adjusting the duty cycle (d). The power-flow direction depends on the corresponding i_L: when i_L runs from left to right, the power is transferred upwards, and C_1 is charged and C_2 is discharged; when i_L runs from right to left, the power is transferred downwards, and C_1 is discharged and C_2 is charged. In other words, the voltage balance of the adjacent modules can be achieved by controlling i_L. By balancing the voltages of every two adjacent SMs, it is possible to achieve voltage balance for the entire system.

C. CONVERTER MODELING

Since a single VB can only balance voltages for the adjacent modules, it cannot perform rapid dynamic property when applied to a system with a large number of modules [6]. The extreme situation happens when mismatched power exists between the first and the last module, with $N - 1$ iterations for the voltage-balancing process. Another example is shown in Fig. 3 (b), wherein VB 1 initially passes the power downwards, reversing the direction once the energy delivered upwards by VB 2 is detected. Hence, if the information of all modules on the VB is imposed and used to implement the regulation in advance, an optimal control method will be established. In order to establish an appropriate strategy, it is necessary to model the entire topology of the system in question.

A strong relationship exists between the inductor current of VB and the mismatched power, which can be used to establish a reasonable method for the controller design. On the basis of the independence of control strategies, MPPT converters are regarded as controlled-current sources in the following analysis; the equivalent circuit of the VB-based multi-port cascaded converter is shown in Fig. 5. The total number of converters is set as N, so there are $N - 1$ sets of VBs. The output voltage and current of the k-th SM are v_k and i_k, respectively. The inductor current of the k-th VB is defined

as $i_{L,k}$, and the duty cycles of the switches are defined as d_k and $1-d_k$. The capacitances and inductances are the same for all VBs, valued as C and L. The inductor current and capacitor voltages are selected as state variables using the state–space averaging method:

$$\begin{cases} C\dfrac{dv_1}{dt} = i_1 + d_1 i_{L,1} - i_g \\ C\dfrac{dv_k}{dt} - C\dfrac{dv_{k-1}}{dt} = i_k + d_k i_{L,k} \\ \quad + (1-d_{k-2})\, i_{L,k-2} - i_{k-1} - i_{L,k-1}, \\ \quad k = 2, 3, \cdots, N \\ L\dfrac{di_{L,k}}{dt} + d_k v_k = (1-d_k)\, v_{k+1}, \\ \quad k = 1, 2, \cdots, N-1 \\ \sum_{k=1}^{N} v_k - L_g\dfrac{di_g}{dt} = V_g. \end{cases} \tag{4}$$

According to (4), the steady-state forms of the variables satisfy

$$\begin{cases} I_g = I_1 + D_1 I_{L,1} \\ I_{k-1} + I_{L,k-1} = I_k + D_k I_{L,k} + \\ \quad (1-D_{k-2})\, I_{L,k-2}, \\ \quad k = 2, 3, \cdots, N \\ D_k V_k = (1-D_k)\, V_{k+1}, k = 1, 2, \cdots, N-1 \\ \sum_{k=1}^{N} V_k = V_g. \end{cases} \tag{5}$$

The control objective is to balance the output voltages in order to derive

$$V_1 = V_2 = \cdots = V_N. \tag{6}$$

Solving the third equation of (5), $D_k = (1-D_k)$ can be obtained as

$$D_1 = D_2 = \cdots = D_{N-1} = 0.5. \tag{7}$$

Assuming that the output power of the k-th SM equals P_k and the power of the DC grid equals P_g with power loss ignored in the circuit, then

$$\begin{cases} P_k = V_k I_k, k = 1, 2, \cdots, N \\ P_g = V_g I_g \\ \sum_{k=1}^{N} P_k = P_g. \end{cases} \tag{8}$$

Substituting (6), (7), and (8) into (5), inductor current can be obtained as

$$I_{L,k} = \frac{2k\,(N-k)}{V_g}\left(\frac{\sum_{j=k+1}^{N} P_j}{N-k} - \frac{\sum_{j=1}^{k} P_j}{k}\right). \tag{9}$$

Equation (9) quantifies the relation between the inductor current and the power differences of the SMs. Indeed, the inductor current of the k-th VB is directly proportional to the difference between the average power value of the first k SM and that of the last $N-k$ SMs. This equation can also be used to verify the power direction discussed in part A of this section.

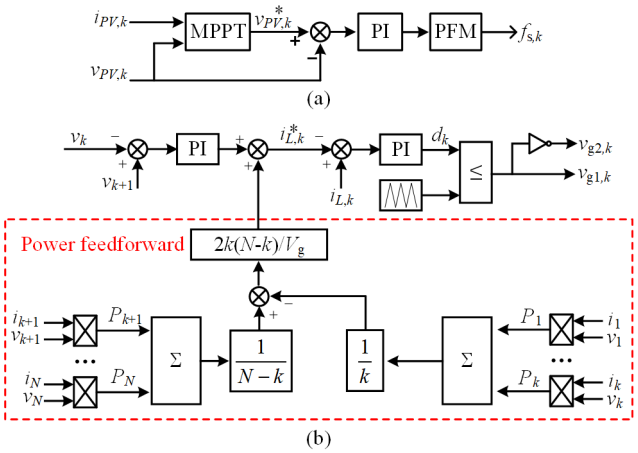

FIGURE 6. The control diagram of the VB-based multi-port converter: (a) MPPT control and (b) the power feedforward voltage-balancing control.

III. CONTROL STRATEGY

A. MPPT CONTROL

MPPT control is realized by the LLC converter. All LLC converters adopt pulse-frequency modulation, operating in the inductive region in order to achieve soft-switching. With the switching frequency set in the inductive region, the input voltage of the LLC converter varies monotonously with respect to the switching frequency when used to connect a PV array with a DC grid. This monotone relationship is conducive to the realization of MPPT. The perturbation and observation method is used as the MPPT algorithm to calculate the input voltage reference. Here, a proportional integral (PI) controller is used to control the input voltage for the LLC converter. The control block diagram is shown in Fig. 6 (a).

B. POWER FEEDFORWARD VOLTAGE-BALANCING CONTROL

Voltage-balancing control is independent of MPPT control. Accordingly, the output voltages of SMs are analyzed with respect to being controlled directly by the inductor currents of the VBs, as discussed in Section II. The currents are controlled by the duty cycles of the switches in VB. Therefore, a voltage and current double closed-loop control is adopted. The voltages of the adjacent SMs are identified, and their difference is sent to the input of the voltage-loop controller, the output of which is used as the current-loop reference.

Obviously, power always flows from high-power SMs to low-power SMs through the VB, which maintains voltage balance. The results of the distributed controllers for every control period result in the converter, ensuring that voltage balance is maintained. Therefore, the voltages are balanced

after initial disturbances. However, if the number of SMs is large, dynamic performance deteriorates. Consider the k-th VB, for example, where, if the input power of the k-th SM is higher than that of the $k+1$ SM, whereas the average input power of the first $k+1$ SM is lower than that of the last $N-k$ SM (see Fig. 3 (b)), the power can be controlled to flow from the k-th SM to the $k+1$ SM, which constitutes local balancing in the wrong direction for global balancing to take place. Therefore, extra time is required for the controller to correct the direction. This suggests that the direction of the power flow for global balancing should be pre-judged. Therefore, VB current is calculated in advance according to (9), and a power feedforward control is employed in order to improve the dynamic performance of the controller. The control diagram is shown in Fig. 6 (b).

C. SYSTEMATIC STABILITY ANALYSIS OF THE CONTROL STRATEGY

With small perturbations of the variables in (4) and Fig. 6 (b), the small-sign model expressions of the controller can be obtained as

$$\begin{cases} sC\hat{v}_1 = \hat{i}_1 + D_1\hat{i}_{L,1} + I_{L,1}\hat{d}_1 - \hat{i}_g \\ sC\hat{v}_k - \quad sC\hat{v}_{k-1} = (1-D_{k-2})\,\hat{i}_{L,k-2} - \hat{i}_{L,k-1} \\ \quad +D_k\hat{i}_{L,k} + \hat{i}_k - \hat{i}_{k-1} - I_{L,k-2}\hat{d}_{k-2} \\ \quad +I_{L,k}\hat{d}_k, k = 2, 3, \cdots, N \\ (1-D_k)\,\hat{v}_{k+1} \quad - D_k\hat{v}_k - sL\hat{i}_{L,k} \\ \quad = (V_{k+1}+V_k)\,\hat{d}_k, \\ \quad k = 1, 2, \cdots, N-1 \\ \sum_{k=1}^{N}\hat{v}_k - sL_g\hat{i}_g = \hat{v}_g \\ \hat{i}^*_{L,k} \quad = \left(k_{vp} + \dfrac{k_{vi}}{s}\right)\left(\hat{v}_{k+1} - \hat{v}_k\right) \\ \quad + \dfrac{2k}{V_g}\sum_{j=k+1}^{N}\left(I_j\hat{v}_j + V_j\hat{i}_j\right) \\ \quad - \dfrac{2\,(N-k)}{V_g}\sum_{j=1}^{k}\left(I_j\hat{v}_j + V_j\hat{i}_j\right), \\ \quad k = 1, 2, \cdots, N-1 \\ \hat{d}_k \quad = \left(k_{ip} + \dfrac{k_{ii}}{s}\right)\left(-\hat{i}^*_{L,k} + \hat{i}_{L,k}\right), \\ \quad k = 1, 2, \cdots, N-1 \end{cases} \tag{10}$$

where I_k, V_k, D_k, and $I_{L,k}$ represent the stationary solutions for i_k, v_k, d_k, and $i_{L,k}$, respectively. In total, there are $6N-2$ variables in (10), among which v_1–v_N, i_g, $i_{L,1}$–$i_{L,N-1}$, d_1–d_{N-1}, and $i^*_{L,1}$–$i^*_{L,N-1}$ are set as state variables and i_1– i_N and v_g are set as input variables. Taking the state variables as unknown numbers, there are $4N-2$ equations with $4N-2$ unknown numbers. After solving these, the following can be obtained:

$$\begin{cases} \hat{v}_j = \sum_{i=1}^{N}\left(T_{i,j}(s)\,\hat{i}_i\right) + T_{g,j}(s)\,\hat{v}_g, \\ \quad j = 1, 2, \cdots, N \\ \hat{i}_g = \sum_{i=1}^{N}\left(G_{i,g}(s)\,\hat{i}_i\right) + G_{g,g}(s)\,\hat{v}_g \\ \hat{i}_{L,j} = \sum_{i=1}^{N}\left(H_{i,j}(s)\,\hat{i}_i\right) + H_{g,j}(s)\,\hat{v}_g, \\ \quad j = 1, 2, \cdots, N-1 \\ \hat{i}^*_{L,1} = \sum_{i=1}^{N}\left(H^*_{i,j}(s)\,\hat{i}_i\right) + H^*_{g,j}(s)\,\hat{v}_g, \\ \quad j = 1, 2, \cdots, N-1 \\ \hat{d}_j = \sum_{i=1}^{N}\left(F_{i,j}(s)\,\hat{i}_i\right) + F_{g,j}(s)\,\hat{v}_g, \\ \quad j = 1, 2, \cdots, N-1. \end{cases} \tag{11}$$

When considering the impact that $\hat{i}_i$ has on $\hat{v}_j$, the impact of $\hat{v}_k (k \neq i)$ and $\hat{v}_g$ is neglected. Assuming $\hat{i}_k = \hat{v}_g = 0 (k \neq i)$,

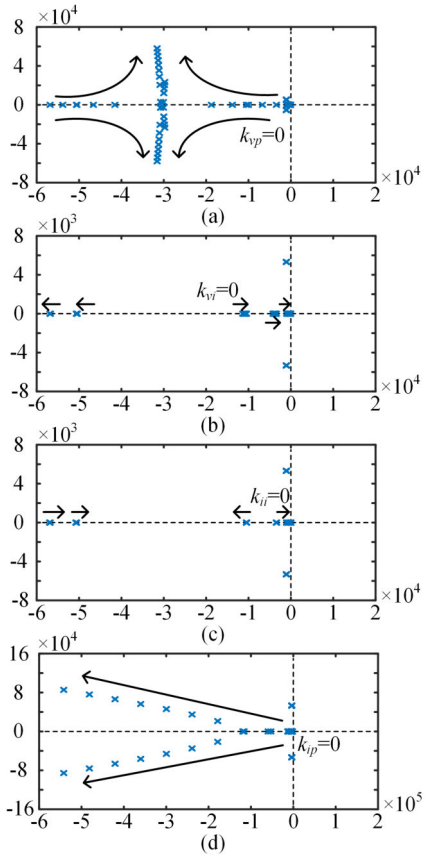

FIGURE 7. The pole distribution of $T_{1,1}(s)$ in a three-SM cascaded converter: (a) k_{vp} varies from 0 to 10, with $k_{vi} = 10$, $k_{ip} = 5$, and $k_{ii} = 2$; (b) k_{vi} varies from 0 to 1000, with $k_{vp} = 0.05$, $k_{ip} = 5$, and $k_{ii} = 2$; (c) k_{ip} varies from 0 to 10, with $k_{vp} = 0.05$, $k_{vi} = 10$, and $k_{ii} = 2$; and (d) k_{ii} varies from 0 to 10, with $k_{vp} = 0.05$, $k_{vi} = 10$, and $k_{ip} = 5$.

the following can be obtained:

$$\frac{\hat{v}_j}{\hat{i}_i} = T_{i,j}(s) = \frac{M_{i,j}(s)}{D_{i,j}(s)} \tag{12}$$

where $M_{i,j}(s)$ and $D_{i,j}(s)$ are high-order polynomials. Then the transfer function from the i-th controlled-current disturbance source to the j-th SM voltage ($T_{i,j}(s)$) can be calculated. The transfer function from the bus voltage disturbance to the j-th SM voltage ($T_{g,j}(s)$) can also be calculated following the same procedure. If the poles of $T_{i,j}(s)$ and $T_{g,j}(s)$ for any i and j are all on the left half of the complex plane, the system will be stable.

Taking $T_{1,1}(s)$ of a three-SM cascaded converter, for example, the effects of the controller parameters on the stability of the system are provided. Voltage-loop controller parameters (k_{vp} and k_{vi}) and current-loop controller parameters (k_{ip} and k_{ii}) are set as variables. The other parameters are shown in the fourth column of Table II in Section V.

Fig. 7 presents the pole distribution of $T_{1,1}(s)$ when the controller parameters vary, from which it is evident that the poles are on the left half of the complex plane and that the system is stable under the first controlled-current disturbance.

D. PERFORMANCE ANALYSIS OF POWER FEEDFORWARD CONTROL

In order to illustrate the performance of the proposed power feedforward control, the Bode diagrams of $T_{1,2}(s)$, $T_{2,3}(s)$, and $T_{3,1}(s)$ with and without power feedforward control are plotted in Fig. 8, from which it is apparent that the power feedforward control reduces the influence of input-current disturbance on the SM output voltage and accelerates the input transient response of the converter.

IV. VB CIRCUIT DESIGNS

A. VB INDUCTOR DESIGN

The major parameters of the inductor design include the value of the inductor (L) and the nominal inductor current ($I_{L,R}$). According to (9), a positive correlation exists between the steady-state current of the inductor and the differences in the generated power. The maximum value of the inductor current can be used as a reference to select appropriate devices. Supposing the full generating power of the PV array equals P_R, then the power transferred through the SMs satisfies $0 <= P_1, P_2, \ldots, P_N <= P_R$. In addition, $\sum_{j=k+1}^{N} P_j/(N-k)$ is taken as the average power of the last $N-k$ SM, and $\sum_{j=1}^{k} P_j/(N-k)$ is taken as the average power of the first k SM. Accordingly, it can be inferred that

$$\begin{cases} 0 \le \sum_{j=k+1}^{N} P_j/(N-k) \le P_R \\ 0 \le \sum_{j=1}^{k} P_j/k \le P_R. \end{cases} \tag{13}$$

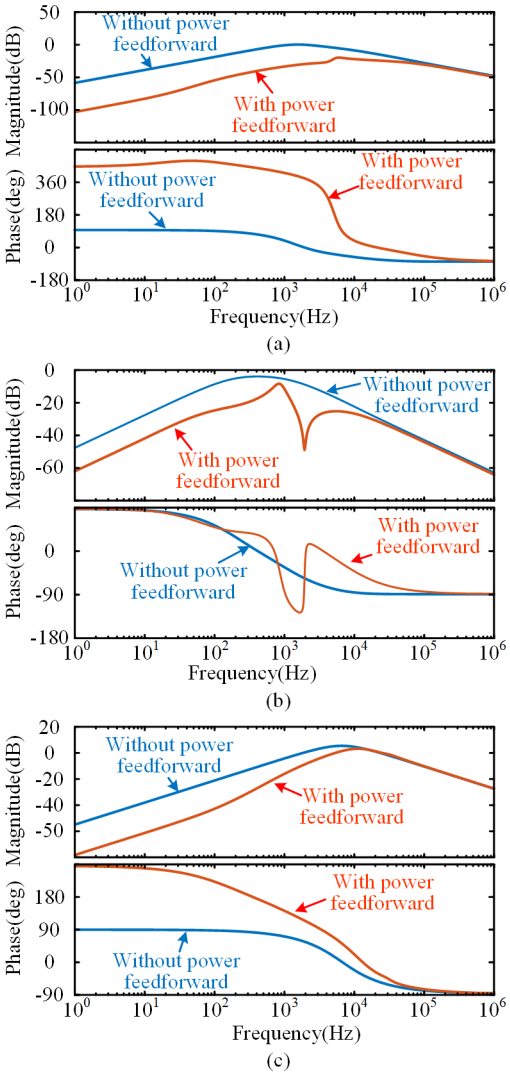

FIGURE 8. Bode diagrams of input-current to output-voltage transfer functions: (a) $T_{1,2}(s)$, (b) $T_{2,3}(s)$, and (c) $T_{3,1}(s)$.

Substituting (13) into (9), the following can be derived:

$$-\frac{2k(N-k)P_R}{V_g} \le I_{L,k} \le \frac{2k(N-k)P_R}{V_g}. \tag{14}$$

Accordingly, the maximum of $I_{L,k}$ can be obtained as

$$I_{L,k,\max} = \frac{2k(N-k)P_R}{V_g}. \tag{15}$$

From (15), and setting $dI_{L,k,\max}/dk = 0$, the following can be obtained:

$$\frac{2P_R}{V_g}(N-2k) = 0, \tag{16}$$

the solution of which is

$$k_0 = N/2. \tag{17}$$

Since k represents an integer, when k equals $[N/2]$ ($[x]$ represents the nearest integer to x), $I_{L,k,\max}$ reaches its peak

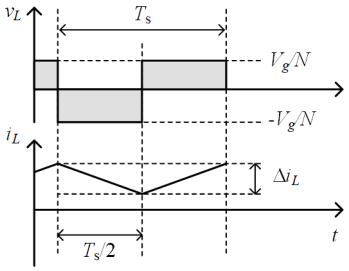

FIGURE 9. The voltage waveform and current waveform of the inductor at steady state.

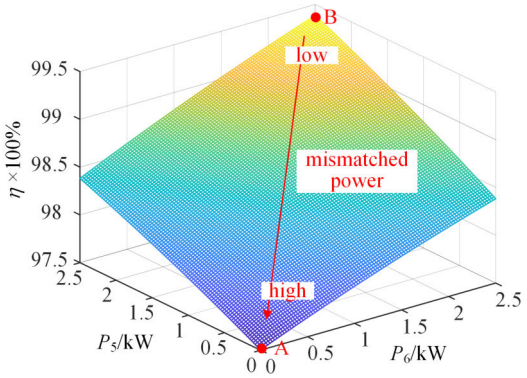

FIGURE 10. The relationship between converter efficiency and the input power.

value as

$$I_{L,\max} = \begin{cases} \dfrac{N^2 P_R}{2V_g}, & \text{when } N \text{ is even} \\ \dfrac{\left(N^2-1\right) P_R}{2V_g}, & \text{when } N \text{ is odd} \end{cases} \tag{18}$$

which sets the nominal current value ($I_{L,R}$) of the inductor.

In fact, VB configuration is equivalent to a bidirectional buck-boost converter. By means of adjusting inductance, its operating mode can be changed [33]. Given the fact that the operation takes place in the continuous-current mode, we can ignore the influence of different operating modes. Alternatively, the inductance is also related to the peak-to-peak value of the inductor current. The current and voltage of the inductor in the steady state are shown in Fig. 9. The expression of current increment (Δi_L) within a half period ($T_s/2$) can be described as

$$L\frac{\Delta i_L}{T_s/2} = V_g/N. \tag{19}$$

Then, the expression of the peak-to-peak value of current ripple can be described as

$$\Delta i_L = \frac{V_g}{2f_s LN}. \tag{20}$$

where f_s represents the switching frequency.

The overlarge ripple value will likely result in the core saturation of the inductor [34]. Accordingly, it is restricted to

TABLE 1. Component numbers of different topologies.

Component number	VB-based IIOS	TSC	LVBB
Switch	$2N-2$	$2N$	$4N$
Diode	0	N	$4N$
Inductor	$N-1$	$2N$	0
Capacitor	0	$2N$	N
Transformer	0	0	N

TABLE 2. Component numbers of different topologies.

Parameter	Symbol	Simulation	experiment
General Parameters			
Generated Power	P_N	25 kW	360 W
Grid voltage	V_g	5 kV	90 V
Number of SMs	N	10	3
Line inductance	L_g	1 mH	0.46 mH
LLC Converter Parameters			
Resonant inductance	L_r	96 μH	12 μH
Resonant capacitance	C_r	20 nF	440 nF
Magnetic inductance	L_m	300 μH	58 μH
Winding turns ratio of transformer	$N1$:$N2$	1:1	1:1
Output filtering capacitance	C_f	220 μF	220 μF
VB Parameters			
Switching frequency	f_s	100 kHz	100 kHz
Inductance	L_{VB}	1 mH	110 μHH
Proportion coefficient of the voltage loop	k_{vp}	2	0.05
Integration coefficient of the voltage loop	k_{vi}	3000	10
Proportion coefficient of the current loop	k_{ip}	0.01	5
Integration coefficient of the current loop	k_{ii}	1000	2

a value smaller than the nominal one [35]. The design value can be acquired with

$$L = \frac{V_g}{2f_s N \varepsilon I_{L,R}} \tag{21}$$

where ε is the ripple ratio.

B. DEVICE VOLTAGE RATING OF VB

Fig. 4 shows a diagram of a VB. Accordingly, the system is aware when one switch conducts and the other turns off with a terminal voltage of $v_1 + v_1$. Moreover, when the entire system reaches steady state, v_1 and v_2 satisfy

$$v_1 = v_2 = V_g/N \tag{22}$$

where v_g represents DC bus voltage and N represents the number of SMs. The maximum voltage of the switch is

$$V_{S,R} = 2V_g/N. \tag{23}$$

Equation (23) can be used to determine the nominal voltage of the VB switches.

C. DEVICE CURRENT RATING OF VB

S_1 and S_2 allow the inductor current to flow through itself for a half switching cycle, so the nominal current of each switch is half of the inductor current. The rated inductor current

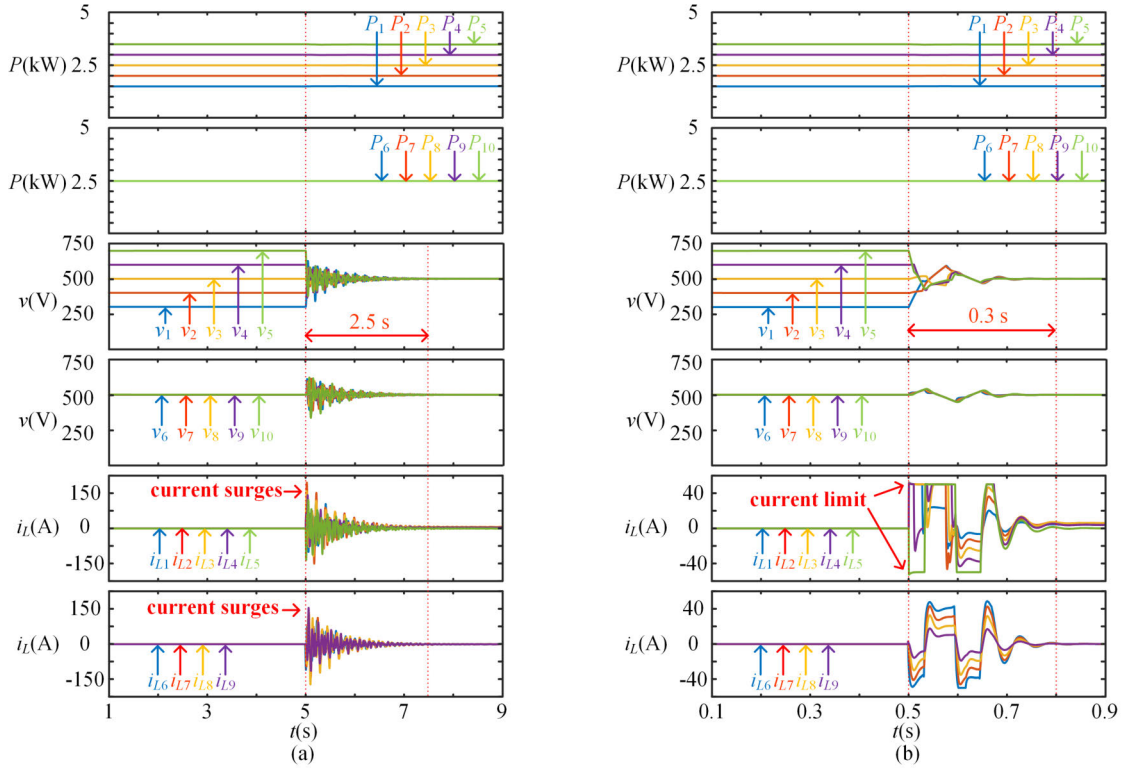

FIGURE 11. Simulation results of the 5 kV system with constant input power of the SMs in the MPPT stage: (a) constant duty cycle (50%) control and (b) voltage and current double closed-loop control combined with power feedforward control.

is determined by (18). Therefore, the rated current for the switches in VB can be derived as

$$I_{S,R} = \begin{cases} \dfrac{N^2 P_R}{4V_g}, & \text{when } N \text{ is even} \\ \dfrac{\left(N^2-1\right) P_R}{4V_g}, & \text{when } N \text{ is odd.} \end{cases} \tag{24}$$

V. CONVERTER EFFICIENCY AND TOPOLOGY COMPLEXITY ANALYSES

A. CONVERTER EFFICIENCY ANALYSIS

The power loss of the k-th VB includes copper loss of the inductor (L_k) as well as the switching loss and conduction loss of $S_{1,k}$ and $S_{2,k}$, the former of which can be calculated by

$$P_{L,k} = I_{L,k}^2 r_{L,k}. \tag{25}$$

A commonly used formula for estimating the MOSFET switching power loss [36] is given as

$$P_{SW,k} = \frac{1}{2} I_{D,k} V_{D,k} (t_{ON} + t_{OFF}) f_s + \frac{1}{2} C_{oss} V_D^2 f_s \tag{26}$$

where $I_{D,k}$ and $V_{D,k}$ are the drain-to-source current and voltage of the MOSFET, respectively; T_{ON} and T_{OFF} are the turn on and turn off times, respectively; f_s is the switching frequency; and C_{oss} is the output capacitance. According to the analysis in Section IV, the following can be obtained

$$\begin{cases} I_{D,k} = I_{L,k} \\ V_{D,k} = \left(2V_g\right)/N. \end{cases} \tag{27}$$

From (26) and (27), the following can be obtained:

$$P_{SW,k} = \frac{I_{L,k} V_g}{N} (t_{ON} + t_{OFF}) f_s + 2C_{oss} \frac{V_g^2}{N^2} f_s. \tag{28}$$

The conduction loss of a switch is expressed as

$$P_{con,k} = I_{RMS,k}^2 R_{ON} \tag{29}$$

where $I_{RMS,k}$ is the root-mean-square current of the drain current and R_{ON} is the on-state resistance. On the basis of the analysis in Section IV, the following can be obtained

$$P_{con,k} = I_{RMS,k}^2 R_{ON} = \frac{1}{2} I_{L,k}^2 R_{ON}. \tag{30}$$

The total power loss of the VBs is

$$P_{loss} = \sum_{k=1}^{N-1} \left(P_{L,k} + 2P_{SW,k} + 2P_{con,k}\right). \tag{31}$$

In order to analyze the efficiency of the balancing stage separately, the efficiency of the MPPT stage is assumed

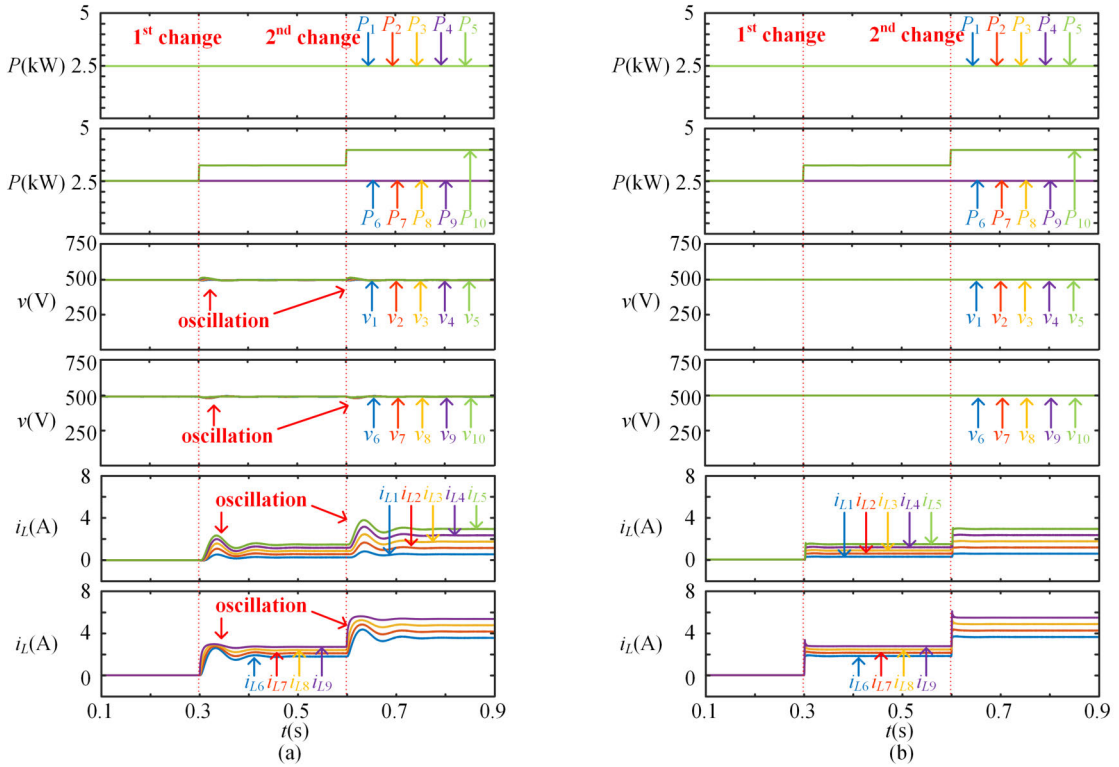

FIGURE 12. Simulation results of the 5 kV system with changing input power with respect to the last SM: (a) voltage and current double closed-loop control and (b) voltage and current double closed-loop control combined with power feedforward control.

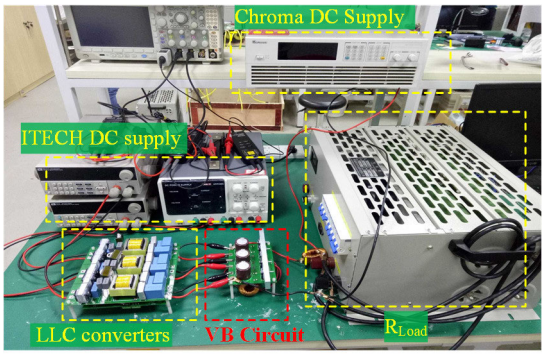

FIGURE 13. Small-scale experimental prototype.

as 100%. Then, the converter efficiency can be estimated by

$$\eta = \frac{\sum_{i=1}^{N} P_i - P_{loss}}{\sum_{i=1}^{N} P_i} \times 100\%. \tag{32}$$

The 10-SM converter can be used as an example for calculating the power efficiency. The power of the fifth and sixth SMs is variable, whereas that of the remaining SMs is constant at 2.5 kW. Simulation parameters shown in Table II are used for the calculation. The C2M0045170P (1700V/72A) is selected as the active switch. The relationship between converter efficiency (η) and the input power (P_5 and P_6) is shown in Fig. 10, from which it is evident that the converter efficiency is high when there is minimal SM differential power. When $P_5 = P_6 = 0$, or to put it another way, when the mismatched power is at its peak value, the system reaches a minimal efficiency of 97.5% at point A; when $P_5 = P_6 = 2.5$ kW, the system reaches a maximum efficiency of 99.38% at point B. In conclusion, the VB can only process differential power with minimal power losses, especially when the mismatched power is low.

B. TOPOLOGY COMPLEXITY ANALYSIS

In this section, the proposed converter, LVBB type, and the TSC type are compared in terms of how many semiconductor switches and passive components are required in each. Assuming that all three have the same configuration for their MPPT stage in Table I, the component numbers listed only cover a portion of those in the voltage-balancing stage.

Although extra $2N - 2$ switches and $N - 1$ inductors are adopted in this VB-based IIOS system, it still has the competitive advantage of being simple and economically sound compared with the other types of voltage-balancing topology.

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of the proposed converter with respect to its power feedforward voltage-balancing control, a 5 kV PV system was modeled in

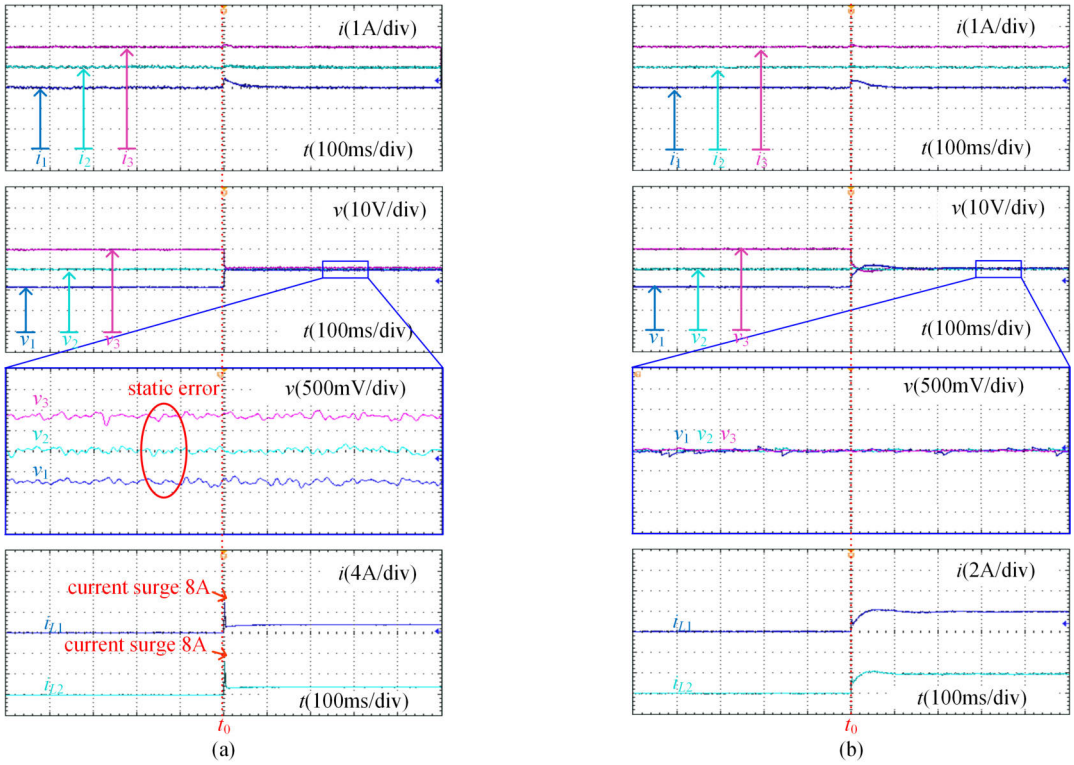

FIGURE 14. Simulation results of the 5 kV system with constant input power of the SMs in the MPPT stage: (a) constant duty cycle (50%) control and (b) voltage and current double closed-loop control combined with power feedforward control.

MATLAB/SIMULINK and a small-scale experiment was conducted. The relating parameters are shown in Table II.

A. SIMULATION VERIFICATION OF A 5 KV PV SYSTEM

The performance of the VB was tested by comparing the states of the SM voltages before and after the balancer was applied. The performances of the constant duty-cycle (50%) control [31] and that of the voltage and current double closed-loop control combined with the power feedforward control are compared in Fig. 11, from which it is evident that the output voltages of the SMs (v_1–v_{10}) are unbalanced because of having a different input power deriving from the PV arrays. At $t = 5$ s (or 0.5 s), the VBs start working and the input power of the SMs does not change. With the help of the VBs, voltage balancing is achieved. At the same time, current (i_{L1}–i_{L9}) passes through the inductors of the VBs. However, it takes time (2.5 s) for the constant duty-cycle control to reach steady state, and, simultaneously, current surges exist. From Fig. 11, the effectiveness of the VBs is verified; moreover, it is evident that a closed-loop control is necessary, rather than a constant duty-cycle control.

Fig. 12 presents the waveforms when the solar irradiance and the input power of the last SM change. Comparisons are made between dynamic performance without power feedforward control and dynamic performance with power feedforward control. The input power of the last SM (P_{10}) changes from 2.5 to 3.25 kW at $t = 0.3$ s and then from 3.25 to 4 kW at t = 0.6 s; the power of the remaining SMs (P_1–P_9) does not change. In addition, the output voltages of the SMs (v_1–v_{10}) are balanced regardless of whether the power feedforward control is adopted. However, from Fig. 12 (a), it is evident that there are oscillations in voltage and current waveforms, as well as current surges when the power changes, whereas in Fig. 12 (b), oscillations are not observed. Moreover, according to Fig. 12 (a), the system takes almost 200 ms to reach the stable state, which is a longer process than the regulation process, as shown in Fig. 12 (b). It should be noted that identical PI controller parameters are adopted in both cases. In light of this information, the validity and the advantages of power feedforward voltage-balancing control have been verified.

B. EXPERIMENTAL VERIFICATION OF A 90 V SYSTEM

A small-scale VB-based cascaded converter prototype was built to verify the voltage-balancing capacity for the converter and the effectiveness of the proposed novel power feedforward balancing control. The prototype consists of three SMs (LLC converters) and two VBs.

The inputs of the LLC converters were provided by three ITECH DC power supplies. An input-current loop was applied to the LLC converters in order to simulate MPPT. The DC bus voltage was afforded by Chroma 62100H-600S programmable DC power supply. A suitable resistor was connected in parallel to the Chroma DC power supply as a load

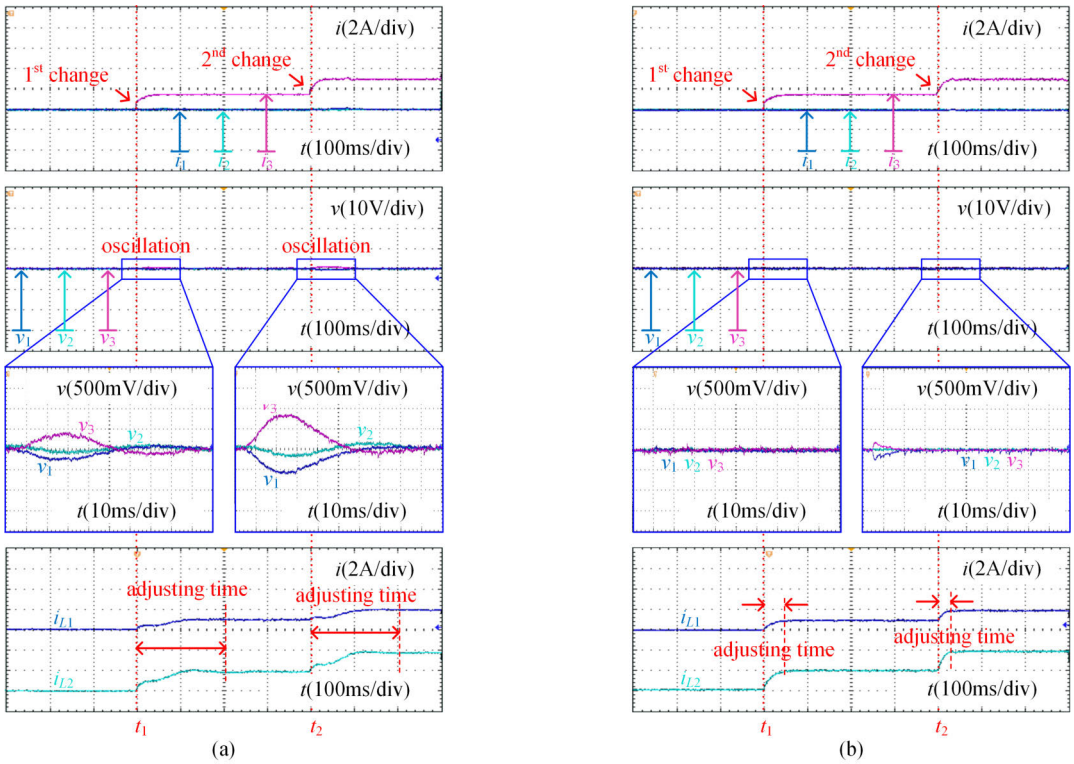

FIGURE 15. Simulation results of the 5 kV system with changing input power with respect to the last SM: (a) voltage and current double closed-loop control and (b) voltage and current double closed-loop control combined with power feedforward control.

to consume the energy, thereby ensuring safe operation of the system. The experimental prototype is presented in Fig. 13.

Fig. 14 (a) presents the waveforms of the system with constant duty-cycle (50%) control [31], and Fig. 14 (b) presents those with voltage and current double closed-loop control combined with power feedforward control. The input currents of the LLC converters (i_1–i_3) were kept constant throughout the process. Before the voltage-balancing control was applied, the voltages (v_1–v_3) suffered from significant imbalance. Thereafter, with the control applied at $t = t_0$, voltage balancing was realized.

From Fig. 14, it is evident that voltage-static errors and current surging are present when the constant duty-cycle control is employed. In contrast, these factors are not evident when the proposed voltage and current double closed-loop with power feedforward control is employed.

Fig. 15 presents the waveforms when the input current of the third LLC converter (i_3) changes from 4 to 5.5 A and then from 5.5 to 7 A, whereas those of the first and second LLC converters (i_1 and i_2) remain constant. The power feedforward control is not adopted in Fig. 15 (a), but it is adopted in Fig. 15 (b).

It can be seen that the output voltages of the LLC converters (v_1–v_3) remain balanced regardless of whether the power feedforward control is adopted. However, from Fig. 15 (a), oscillations can be seen in the voltage waveforms when the i_3 changes, whereas in Fig. 15 (b), no such oscillation can be observed. As a result, in Fig. 15 (a), the system takes almost 200 ms to reach the stable state, whereas in Fig. 15 (b), the regulation process is complete within a much shorter time period (50 ms).

According to the comparison, the effectiveness and advantages of the power feedforward voltage-balancing control have been verified.

By comparing Fig. 11 with Fig. 14, it is clear that considerable oscillations do not exist in the voltage and current waveforms of the experimental results. The same scan be said when comparing Fig. 12 and Fig. 15. This is because the inductors employed in the experiments provide a relatively large equivalent series resistance, which increases the damping of the whole system. However, this does not mean that the proposed control is not optimal under this condition.

VII. CONCLUSION

In this paper, a VB-based multi-port cascaded converter with a novel power feedforward voltage-balancing control for the MVDC grid interface of PV systems was introduced. The LLC converter was applied as the SM in the MPPT stage. Indeed, a high step-up ratio can be achieved by cascading the LLC converters. The VBs are placed between every two adjacent SMs in order to balance the voltages. The relationship between the current flowing through the VB and the power difference of the PV arrays was also analyzed. Simulation and experimental results verified the excellent voltage-balancing capacity and dynamic performance of the proposed converter and its control strategy.

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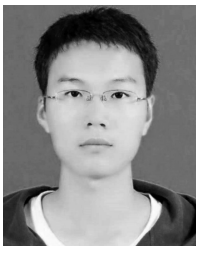

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