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A New Topology of Modular Multilevel Converter With Voltage Self-Balancing Ability

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ABSTRACT The modular multilevel converter (MMC) has been used in the field of HVDC transmission due to its many advantages, but its voltage imbalance problem of sub-module capacitors affects the stable operation of the system. There are two kinds of methods for solving the capacitor voltage imbalance of the MMC sub-module. The one is voltage balancing algorithm and the other one is improved topology. However, the complexity of the voltage balancing algorithm increases sharply when the number of voltage levels is high, which is not suitable for the MMC system with a high number of voltage levels. In this paper, a new topology with bidirectional voltage self-balancing capability is proposed. This topology adds the voltage balancing circuit between sub-modules on the conventional MMC topology, realizing voltage self-balancing without voltage balancing algorithm, and having a better effect of inhibition phase-to-phase circulation. The bidirectional voltage balancing capability, the voltage balancing effect and the circulation inhibition effect of the bidirectional voltage self-balancing topology are verified by MATLAB/Simulink simulation and experiment.

INDEX TERMS Modular multilevel converter (MMC), voltage balancing circuit, bidirectional voltage self-balancing, circulation inhibition.

I. INTRODUCTION

With the booming world economy, global electricity consumption continues to grow. Traditional thermal power generation has been unable to meet the demand for electricity growth brought about by economic development, and thermal power generation is widely considered to be the main cause of global warming. And sustainable energy, such as wind, solar, biomass, tidal, and geothermal, has become a promising solution for continuous fossil fuel depletion. China has a long coastline, a wide distribution of wind energy resources, and good wind energy quality, which can develop offshore wind resources on a large scale. At the same time, the coastal areas are scarce in mineral resources, but the demand for electricity is large. Offshore wind power can be absorbed nearby in coastal areas.

The modular multilevel converter (MMC) is a new topology of converter proposed by Lesnicar and Marquardt [1]–[3], having arisen as the leader and most competitive solution for voltage source converter applications operating in the range of high-power and high-voltage levels [4]–[7].

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Modular multilevel converter (MMC) adopts modular structure and has the advantages of easy expansion, good output waveform quality, comprehensive fault protection, strong recovery capability, low loss and strong unbalanced operation capability [8]–[13], used in the field of high voltage direct current transmission [14]–[18].

Although MMC has many advantages in the field of high voltage direct current transmission, there are still key problems that have not yet been broken, including sub-module capacitor voltage balancing problems and phase-to-phase circulation problems [19]–[22]. Because the MMC adopts a modular structure, the capacitors of the sub-modules are independent of each other, resulting in an imbalance of the sub-module capacitor voltage. Capacitor voltage imbalance is a serious threat to the reliable operation of HVDC systems based on MMC. Keeping the SM capacitor voltages balanced at their nominal values has become one of the main technical challenges for MMC [23]–[25].

In [22], the sub-module capacitor voltage direct sorting algorithm is used to collect the voltage of each sub-module, and the capacitor voltages are sorted in order from small to large. According to the sub-module capacitor voltage sorting result, The sub-module voltage direct sorting algorithm is

complexed. And it also need a lot of voltage sensors. Literature [26] proposed a voltage balancing method with less sensors. It has a better capacitor voltage balancing effect. But when the voltage levels is large the method would be more complex. In order to reduce the complexity of the sorting algorithm, the literature [27] proposed the mass factorization method and the Hill sorting algorithm. The algorithm uses mass factorization to divide the capacitor voltage in the bridge arm into several layers, and then uses the Hill sorting algorithm to arrange the capacitor voltages from small to large or from large to small. The trigger pulse is adjusted according to the arrangement result to realize the sub-module capacitor voltage balancing. The mass factorization method and the Hill sorting algorithm can effectively reduce the complexity of the sorting algorithm and improve the efficiency of the sorting algorithm.

Literature [28] proposed an MMC topology with self-balancing capability. The topology is connected in parallel with a diode on the basic of the conventional MMC structure, and each phase circuit includes four bridge arms, which can realize voltage self-balancing of the sub-module capacitor. But, it would increase the volume of MMC. Literature [29]–[31] achieves capacitor voltage balancing by increasing the voltage balancing loop. In [29], a method of equalizing the voltage of chopper circuit is proposed, which realizes effective voltage equalization through the switching scheme. Literature [30] presented a modular balancing bridge for series-connected voltage sources, where the voltage balancing is achieved across N cells using cascaded transformers with coupled windings. This method may be used in MMC systems, but requires a large number of transformers to add sub-modules design complexity. A voltage balancing circuit consisting of two unidirectional choppers and a single coupled inductor with two galvanically isolated windings were proposed in [31], where the phase-shift control is used to adjust the balancing circuit. For MMC systems, the hardware costs and the complexity of the system control for this method are significantly increased.

This paper proposes a bidirectional voltage self-balancing MMC topology, which balances the capacitor voltage of the sub-modules by increasing the voltage balancing loop, and modular structure of the MMC is not changed. It gets rid of the dependence on the balancing algorithm. The topology can realize bidirectional voltage balancing between sub-modules, having a better voltage balancing effect, and good circulation inhibition effect. In terms of project cost, the increased cost of the voltage balancing loop is limited, which will only increase the cost of the entire project by about 3%.

II. CONVENTIONAL MMC TOPOLOGY AND BIDIRECTIONAL VOLTAGE SELF-BALANCING TOPOLOGY

A. CONVENTIONAL MMC TOPOLOGY

The conventional MMC topology is shown in Fig.1. The conventional MMC topology is composed of three-phase circuits of A, B, and C. Each phase circuit includes upper and lower

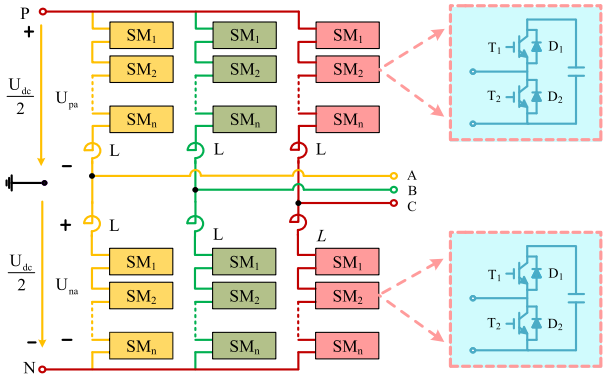


FIGURE 1. Conventional MMC topology.

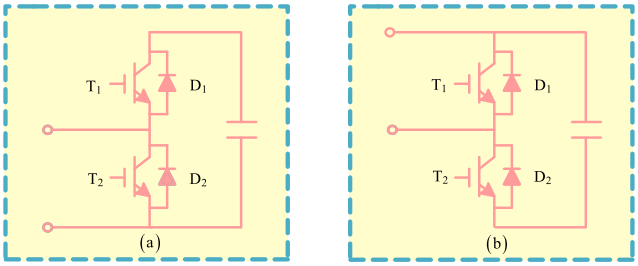


FIGURE 2. Conventional MMC submodule topology.

bridge arms and two bridge arm inductances, and each bridge arm is composed of n sub-modules.

The sub-modules of the MMC topology in Figure 1 adopt the half bridge structure. The half bridge sub-module is constructed in two ways, as shown in Fig.2, consisting of two insulated gate bipolar transistors (IGBTs) with the freewheeling diode D_1, D_2 and capacitor C. The difference between the two submodules is the location of the connection ports.

B. BIDIRECTIONAL VOLTAGE SELF-BALANCING TOPOLOGY

The MMC topology with bidirectional voltage self-balancing capability is shown in Fig.3. Compared with the conventional MMC topology, the MMC topology with bidirectional voltage self-balancing capability adds a voltage balancing circuit between adjacent submodules, so that the energy difference can be bidirectional transmitted between adjacent submodule capacitors, thereby achieving voltage self-balancing between adjacent submodule capacitors.

The sub-module of the bidirectional voltage self-balancing MMC topology is added a voltage balancing loop composed of an IGBT and an inductor L based on the conventional MMC sub-module. The improved sub-modules are divided into two categories: one is the sub-module within a single-phase circuit, and the other is a sub-module between two-phase circuits. The sub-module in the single-phase circuit is shown in Fig.4.

There are two types of sub-modules between two-phase circuits. One is a sub-module that connects the upper arm circuit between two-phase, as shown in Fig.5(a). One is a sub-module that connects the lower bridge arm circuit between

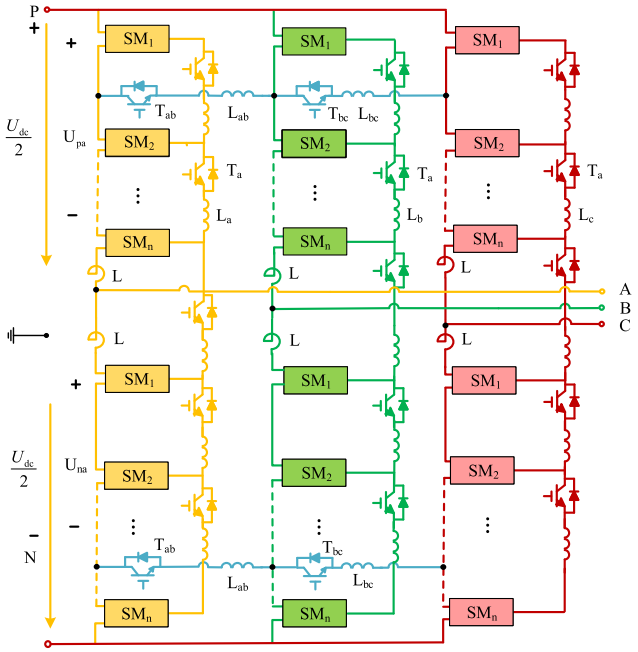


FIGURE 3. Bidirectional voltage self-balancing MMC topology.

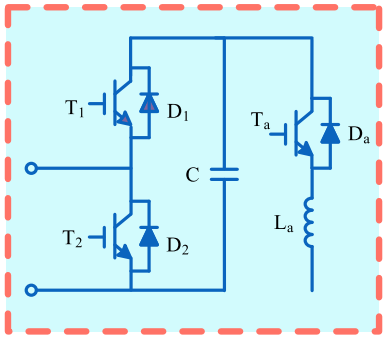


FIGURE 4. The sub-module within a single-phase circuit.

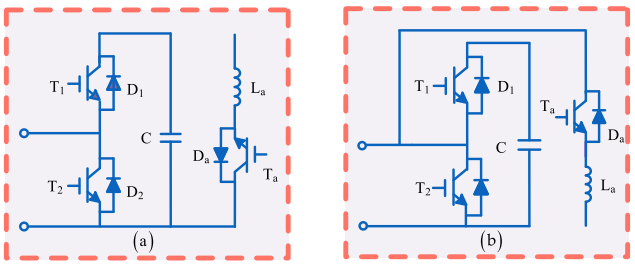


FIGURE 5. The sub-module between two-phases circuit.

two-phases, as shown in Fig.5(b). The voltage self-balancing MMC topology proposed in this paper still has a modular structure.

III. VOLTAGE BALANCING PRINCIPLE OF BIDIRECTIONAL VOLTAGE SELF-BALANCING TOPOLOGY

The bidirectional voltage self-balancing MMC topology is added the voltage balancing circuit on the conventional MMC topology to achieve the capacitor voltage self-balancing of

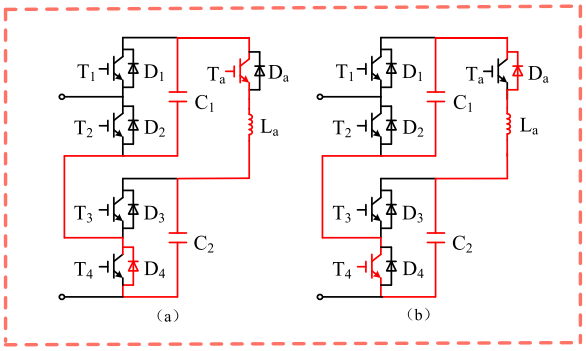


FIGURE 6. Adjacent sub-modules bidirectional voltage self-balancing.

sub-modules. The IGBT in the voltage balancing circuit can realize the bidirectional transmission of energy of the two sub-modules. The inductor can suppress the overcurrent generated during the voltage balancing process, and protect the capacitor in the sub-module and the IGBT in the voltage balancing loop.

Fig.6 is a schematic diagram of voltage balancing between adjacent two sub-modules, which is divided into two cases:

The first case is shown in Fig. 6(a): When the voltage of the capacitor C_1 is greater than that of the capacitor C_2, the energy different between the capacitors is transmitted from C_1 to C_2. At this time, T_a is turned on, and the current flows through the L_a and T_a to the capacitor C_2, and then passes through the freewheeling diode D_4 returns to C_1, forming a complete energy loop, completing the transfer of energy from C_1 to C_2, and the transmission path is marked by a red line. The voltage of the two capacitors are satisfied inequality (1) during the dynamic process:

$$U_{C1} \leq U_{C2} \tag{1}$$

The second case is shown in Fig.6(b): When the voltage of the capacitor C_2 is greater than that of the capacitor C_1, the energy different of the capacitors is transferred from C_2 to C_1. At this time, T_a is in the off state, and T_4 is in the on state. And the current passes through the freewheeling diode D_a and the inductor L_a, flowing to the capacitor C_1. And then return to C_2 through T_4, forming a complete energy loop, completing the transfer of energy from C_2 to C_1, and the transmission path is marked by a red line. The voltage of the two capacitors are satisfied inequality (2) during the dynamic process:

$$U_{C1} \geq U_{C2} \tag{2}$$

The physical meaning of inequality (1) can be described as follows: Capacitor C_1 is always in a tendency to make the voltage of capacitor C_2 greater than its own voltage. The physical meaning of inequality (2) can be described as: Capacitor C_2 is always in a tendency to make the voltage of capacitor C_1 greater than its own voltage.

The two capacitors interact, so that the energy difference is transmitted between the two capacitors, and finally realise the dynamic balance of the energy of the capacitors C_1 and C_2.

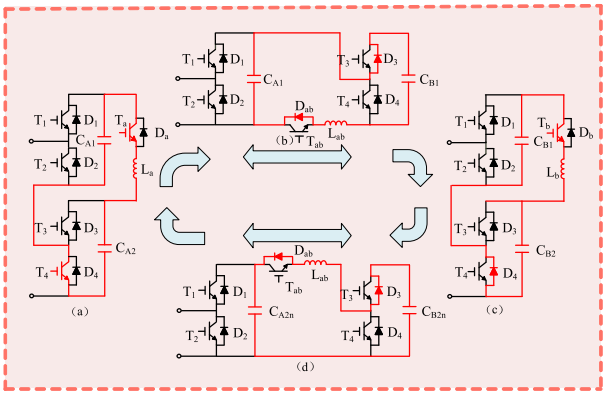


FIGURE 7. Adjacent sub-modules bidirectional voltage self-balancing.

That is:

$$U_{C1} = U_{C2} \tag{3}$$

Through the above process, the energy balance between the adjacent sub-module capacitors is completed. The pulse generation principle of added IGBT is similar to the principle of carrier phase shift pulse triggering.

After adding the voltage balancing circuit, the capacitor voltages between the adjacent sub-modules can be realized, and the energy transmission path is short and the loss is small. Taking the two phases A and B as an example, the voltage balancing principle of the bidirectional voltage self-balancing MMC topology is shown in Fig.7.

Fig.7(a) shows the transfer of electrical energy between the sub-modules of the A-phase. When the voltage of the capacitor C_{A1} is greater than that of capacitor C_{A2}, the T_a is turned on, and the energy is transmitted to the capacitor C_{A2} through the T_a and the inductor L_a, and then return to the capacitor C_{A1} through the freewheeling diode D_4, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (4) during the dynamic process:

$$U_{CA1} \leq U_{CA2} \tag{4}$$

When the voltage of capacitor C_{A2} is greater than that of capacitor C_{A1}, T_a is in the off state, and the energy is transmitted to the capacitor C_{A1} through the freewheeling diode D_a and the inductor L_a, and then flows back to the capacitor C_{A2} through the T_4 forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (5) during the dynamic process:

$$U_{CA1} \geq U_{CA2} \tag{5}$$

The physical meaning of inequality (4) can be described as follows: Capacitor C_{A1} is always in a tendency to make the voltage of capacitor C_{A2} greater than its own voltage. The physical meaning of inequality (5) can be described as: Capacitor C_{A2} is always in a tendency to make the voltage of capacitor C_{A1} greater than its own voltage. That is:

$$U_{CA1} = U_{CA2} \tag{6}$$

The adjacent two sub-modules in the A-phase bridge arm are the same as the Fig.7(a), which satisfies in the dynamic process:

$$U_{CA1} = U_{CA2} = \cdots = U_{CAn} = \cdots U_{CA2n} \tag{7}$$

Fig.7(b) shows the transfer of energy between the A and B phases, the left submodule is the first submodule of the A phase upper arm, and the right submodule is the first sub-module of B phase upper arm.

When the voltage of the capacitor C_{A1} is greater than the voltage of the capacitor C_{B1}, the T_{ab} is turned off, the energy flows to the capacitor C_{B1} through the freewheeling diode D_3, and then returns to the capacitor C_{A1} through the inductor L_{ab} and the freewheeling diode D_{ab}, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (8) during the dynamic process:

$$U_{CA1} \leq U_{CB1} \tag{8}$$

When the voltage of the capacitor C_{B1} is greater than the voltage of the capacitor C_{A1}, the Tab is turned on, the energy flows to the capacitor C_{A1} through the T_3 and the freewheeling diode D_1, and then returns to the capacitor C_{B1} through the inductor L_{ab} and T_{ab}, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (9) during the dynamic process:

$$U_{CA1} \geq U_{CB1} \tag{9}$$

The physical meaning of equation (8) can be described as follows: Capacitor C_{A1} is always in a tendency to make the voltage of capacitor C_{B1} greater than its own voltage. The physical meaning of equation (9) can be described as: Capacitor C_{B1} is always in a tendency to make the voltage of capacitor C_{A1} greater than its own voltage.

The two capacitors interact, so that the energy difference is transmitted between the two capacitors, and finally realise the dynamic balance of the energy of the capacitors C_{A1} and C_{B1}. That is:

$$U_{CA1} = U_{CB1} \tag{10}$$

Fig.7(c) shows the transfer of electrical energy between the sub-modules of the B-phase. When the voltage of the capacitor C_{B1} is greater than the voltage of the capacitor C_{B2}, the T_b is turned on, the energy flows to the capacitor C_{B2} through the inductors L_b and T_b, and then returns to the capacitor C_{B1} through the freewheeling diode D_4, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (11) during the dynamic process:

$$U_{CB1} \leq U_{CB2} \tag{11}$$

When the voltage of the capacitor C_{B2} is greater than the voltage of the capacitor C_{B1}, the Tb is turned off, and the energy flows through the freewheeling diode D_b and the inductor L_b to the capacitor C_{B1}, and then return to the capacitor C_{B2} through the freewheeling diode D_2 and T_4, forming

a complete energy loop. The voltage of the two capacitors are satisfied inequality (12) during the dynamic process:

$$U_{CB1} \geq U_{CB2} \tag{12}$$

The physical meaning of equation (11) can be described as follows: Capacitor C_{B1} is always in a tendency to make the voltage of capacitor C_{B2} greater than its own voltage. The physical meaning of equation (12) can be described as: Capacitor C_{B2} is always in a tendency to make the voltage of capacitor C_{B1} greater than its own voltage.

The two capacitors interact, so that the energy difference is transmitted between the two capacitors, and finally realise the dynamic balance of the energy of the capacitors C_{B1} and C_{B2}. That is:

$$U_{CB1} = U_{CB2} \tag{13}$$

The adjacent two sub-modules in the B-phase bridge arm are the same as the Fig.7(c), which satisfies in the dynamic process:

$$U_{CB1} = U_{CB2} = \cdots = U_{CBn} = \cdots U_{CB2n} \tag{14}$$

Fig.7 (d) is the transfer of energy between the A and B phases, the left submodule is the nth sub-module of the A phase lower arm, and the right sub-module is the nth subsection of the B phase lower arm. When the voltage of the capacitor C_{A2n} is greater than the voltage of capacitor C_{B2n}, the Tab is turned on, and the energy flows to the capacitor C_{B2n} through the T_1, the inductor L_{ab}, the T_{ab}, and the freewheeling diode D_3, and then returns to the capacitor C_{A2n}, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (15) during the dynamic process:

$$U_{CA2n} \leq U_{CB2n} \tag{15}$$

When the voltage of the capacitor C_{B2n} is greater than the voltage of the capacitor C_{A2n}, the Tab is turned off, and the energy flows to the capacitor C_{A2n} through the T_3, the freewheeling diode D_{ab}, the inductor L_{ab}, and the freewheeling diode D_1, and then returns to the capacitor C_{B2n}, forming a complete energy loop. The voltage of the two capacitors are satisfied inequality (16) during the dynamic process:

$$U_{CA2n} \geq U_{CB2n} \tag{16}$$

The physical meaning of equation (15) can be described as follows: Capacitor C_{A2n} is always in a tendency to make the voltage of capacitor C_{B2n} greater than its own voltage. The physical meaning of equation (16) can be described as: Capacitor C_{B2n} is always in a tendency to make the voltage of capacitor C_{A2n} greater than its own voltage.

The two capacitors interact, so that the energy difference is transmitted between the two capacitors, and finally realise the dynamic balance of the energy of the capacitors C_{A2n} and C_{B2n}. That is:

$$U_{CA2n} \geq U_{CB2n} \tag{17}$$

Figure 7 shows the voltage balancing process of the sub-modules of the A and B phase. It can be obtained by formulas (4)-(17):

$$U_{CA1} = \cdots = U_{CA2n} = U_{CB1} = \cdots = U_{CB2n} \tag{18}$$

Due to the modular nature of the MMC, the sub-modules of B and C phases are connected in exactly the same way with the A and B phases. After the voltage balancing process as shown in Fig.7, the voltage of sub-modules capacitors between the B and C phases can be realized. That is:

$$U_{CB1} = \cdots = U_{CB2n} = U_{CC1} = \cdots = U_{CC2n} \tag{19}$$

According to formulas (18) and (19):

$$U_{CB1} = \cdots = U_{CB2n} = U_{CC1} = \cdots = U_{CC2n} \tag{20}$$

It can be obtained from equation (20). After the voltage balancing process as shown in Figure 7, the capacitor voltages of A, B, and C three-phase circuits is balanced. In the process of voltage balancing, IGBTs in each phase voltage balancing circuit is not turn on at the same time to avoid single-phase short circuit fault.

IV. VOLTAGE BALANCING PRINCIPLE OF BIDIRECTIONAL VOLTAGE SELF-BALANCING TOPOLOGY

The phase-to-phase bidirectional self-balancing topology balances the voltage of the sub-modules by the voltage balancing circuit loop between the adjacent sub-module capacitors, and does not require voltage balancing algorithm. When the number of the voltage levels of the MMC system increases sharply, the control difficulty of the system is not improved. In order to illustrate the voltage balancing effect of this topology, the voltage balancing effect of the phase-to-phase bidirectional self-balancing topology is measured objectively from two aspects.

A. CAPACITORS VOLTAGE FLUCTUATION ANALYSIS

The degree of fluctuation of the capacitor voltage:

$$\delta = \frac{U\,(\max) - U\,(\min)}{U\,(\exp)} \times 100\% \tag{21}$$

In the formula: U (max) is the peak value of the capacitor voltage, U (min) is the valley value of the capacitor voltage, and U (exp) is the expected value of the capacitor voltage.

The fluctuation degree of the capacitor voltage is an important index to measure the voltage balancing effect. After the capacitor voltage is balanced, the peak value and the valley value of the capacitor voltage are closer to the expected value, and the equalization effect is better. That is, the smaller the ε is, the better the voltage balancing effect is. And the voltage balancing stability can be reflected to some extent.

B. CIRCULATION SUPRESSION EFFECT ANALYSIS

The voltage imbalance between the sub-module capacitors will produce phase-to-phase circulation. And the more imbalanced of the voltages between the sub-module capacitors,

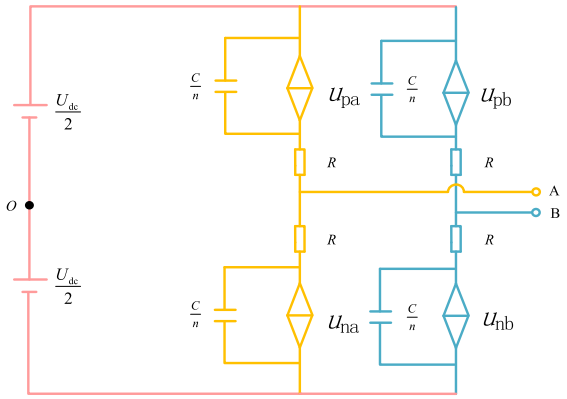


FIGURE 8. Phase-to-phase equivalent circuit diagram.

the greater the phase-to-phase circulation. So that the inhibition effect of the sub-module capacitors to the circulating current can also be used to evaluate the effect of voltage balancing.

In order to analyse the mechanism of phase-to-phase circulation concisely, the two phases A and B of MMC can be equivalent to Fig.8. Each arm of the MMC can be equivalent to a controlled voltage source. U_{pa} is the equivalent controlled voltage source of the upper arm of the A-phase circuit. U_{na} is the equivalent controlled voltage source of the lower arm of the A-phase circuit. U_{pb} is the equivalent controlled voltage source of the upper arm of the B-phase circuit. U_{nb} is the equivalent controlled voltage source of the lower arm of the B-phase circuit. R is the equivalent resistance of each bridge arm. The phase-to-phase circulation expression of the two phases A and B can be expressed as equation (22).

$$i_{cira} = (u_{pa} + u_{na} - u_{pb} - u_{nb})/4R \tag{22}$$

When the A-phase capacitor voltage and the B-phase capacitor voltage are equal, $i_{cira} = 0$.That is, when the capacitor voltages of the A and B two-phase sub-modules are equal, no circulation occurs between the two phases. When the A-phase capacitor voltage and the B-phase capacitor voltage are not equal, the phase-to-phase circulation $i_{cira} \neq 0$. And the larger the capacitance difference between the two-phase sub-modules, the larger the circulation is. Therefore, the degree of balance between the sub-module capacitances can be judged according to the amplitude of the phase-to-phase circulation.

V. SIMULATION VERIFICATION AND ANALYSIS

A. SIMULATION MODEL

In order to verify the effect of voltage self-balancing MMC topography, three models of 11-levels model were built on the MATLAB/Simulink simulation platform to compare the voltage balancing effects.

Model 1: Traditional half-bridge MMC topology model for open-loop carrier phase-shift modulation.

Model 2: Traditional half-bridge MMC topology for carrier phase-shift modulation based on sorting algorithm.

*Model 3:*Voltage self-balancing MMC topology for carrier phase-shift modulation.

TABLE 1. System parameter of simulation.

Parameter	Value
DC-bus voltage	10kV
Inductor of balancing circuit	1mH
Power rating	30MW
SM capacitor voltage	1kV
Arm inductor	5mH
SM capacitors	4700uf
Output frequency	50Hz
Load	0.01H+5Ω

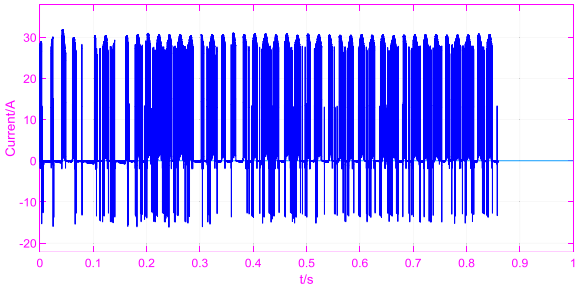


FIGURE 9. The current of voltage balancing circuit loop.

The three models are identical in system parameters, only in the voltage equalization mode or topology. The specific system parameters are as follows:

B. SIMULATION RESULTS

1) BIDIRECTIONAL VOLTAGE SELF-BALANCING FUNCTION VERIFICATION

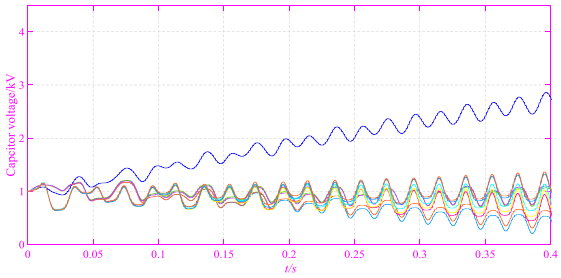
Fig.9 shows the current simulation waveform of the voltage balancing circuit loop. It can be seen from Fig.9 that the current of the voltage balancing circuit loop is positive or negative, indicating that the energy can be transmitted bidirectional in the voltage balancing circuit loop, and the voltage balancing principle described in part 3 can be realized. The bidirectional transmission of energy between adjacent sub-modules shortens the energy transfer path during the voltage balancing process, which can reduce the energy loss during the voltage balancing process and shorten the time of the sub-module capacitor voltage realize to balancing.

2) VOLTAGE SELF-BALANCING FUNCTION VERIFICATION

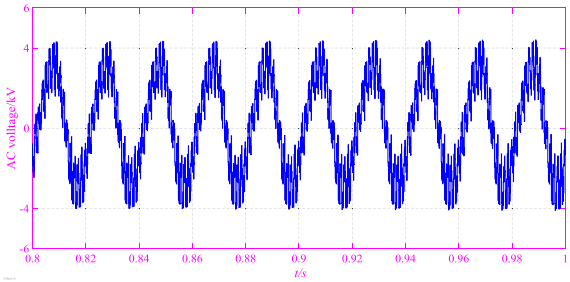
It can be seen from the comparison between Fig.10 and Fig.11 that the sub-module capacitor voltage of the open-loop carrier phase shifting is diverging, and the quality of the output AC voltage waveform is poor. Compared with the model 1, the voltage waveform and the output AC voltage waveform of model 3 is Smoother, and the waveform quality is better. From the comparison point of view, the voltage self-balancing topology has a better effect on voltage balancing.

3) VOLTAGE SELF-BALANCING EFFECT VERIFICATION AND ANALYSIS

Fig.12 shows the capacitor voltage waveform of model 2, and Fig.13 shows the capacitor voltage waveform of model 3.

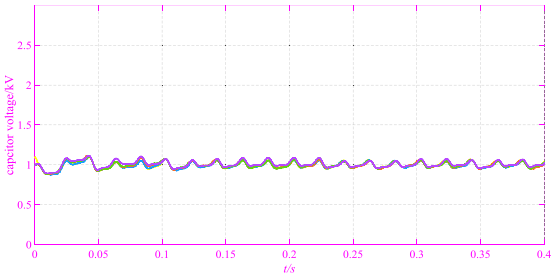


(a) Submodule capacitor voltage

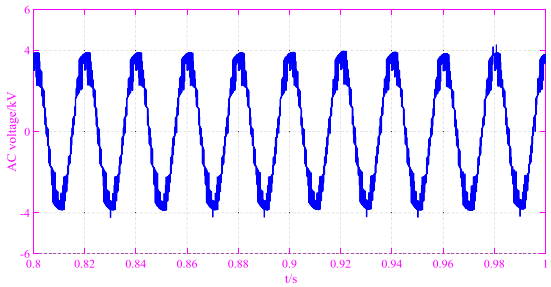


(b) AC output voltage

FIGURE 10. Model 1 voltage waveform.



(a) Submodule capacitor voltage



(b) AC output voltage

FIGURE 11. Model 3 voltage waveform.

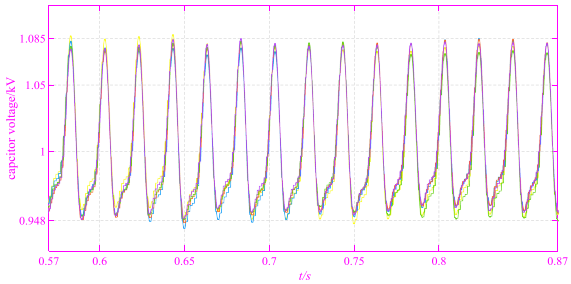


FIGURE 12. Model 2 voltage waveform.

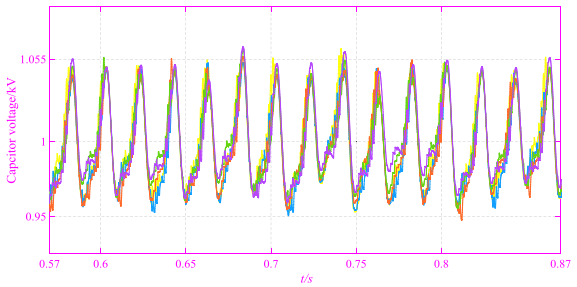


FIGURE 13. Model 3 voltage waveform.

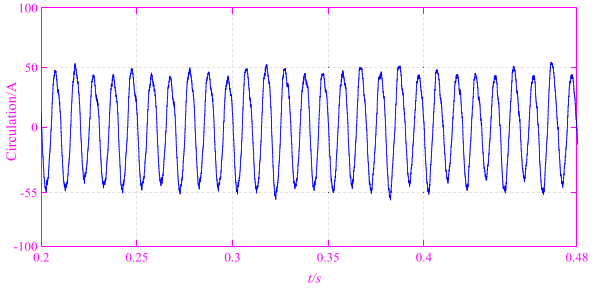


FIGURE 14. Model 2 circulation waveform.

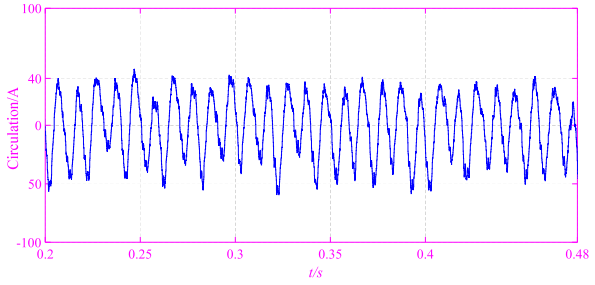


FIGURE 15. Model 3 circulation waveform.

As can be seen from the simulation result, when model 2 reaches a stable state, the maximum value of model 2 is 1.085kV and the minimum value is0.948kV.When model 3 reaches a stable state, the maximum value is 1.055kV and the minimum value is 0.958kV.

According to the analysis in section 4.1, the smaller the fluctuation index is, the better the voltage balancing effect will be. According to equation (21), the voltage fluctuation δ of model 2 is 13.7%, and the voltage fluctuation δ of model 3 is 9.7%. In terms of fluctuation amplitude, the maximum fluctuation of capacitor voltage can be reduced by 30%. Compared with model 2, model 3 has a better voltage balancing effect.

Fig.14 shows the circulation waveform of model 2, and Fig.15 shows the circulation waveform of model 3.According to the analysis in section 4.2 of this paper, the circulation is smaller when the voltage balancing effect is better. Compared with Fig.14 and Fig.15, the circulation of model 3 is 15% smaller than that of model 2. Therefore, the bidirectional voltage self-balancing MMC topology has a better voltage balancing effect.

TABLE 2. System parameter of experiment.

Parameter	Value
DC-bus voltage	300V
Switch frequency	2.5KHz
SM capacitor voltage	25V
Arm inductor	4.5mH
SM capacitors	2200uf
Output frequency	50Hz
Load	10Ω
Voltage balancing loop inductor	0.05mH

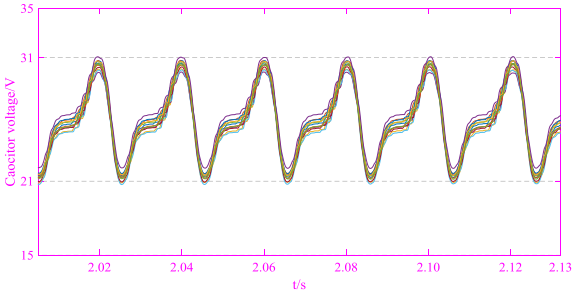


FIGURE 16. Capacitor voltage waveform of sorting algorithm.

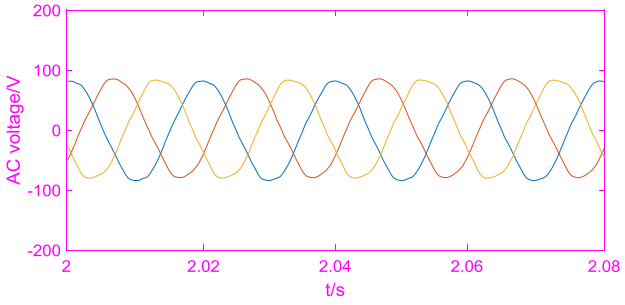


FIGURE 17. AC voltage of sorting algorithm.

VI. EXPERIMENTAL VERIFICATION

In order to verify the voltage balancing effect of the topology proposed in this paper, a 13-level MMC experimental platform based on TMS28335 is built. The platform parameters are shown in Table 2. The following experimental results were obtained by using the LabVIEW PC software.

Fig 16 and Fig 17 show the capacitor voltage waveform and the AC voltage waveform based on the sorting algorithm, respectively. Fig 18 and Fig 19 show the capacitor voltage waveform and the AC voltage waveform of the voltage self-balancing topology, respectively. The capacitor voltage fluctuation of voltage self-balancing topology is reduced by 20% compared with the sorting algorithm. The capacitor voltage is more balanced.

Figure 20 shows the upper arm current waveform of the A-phase based on the sorting algorithm. Figure 21 shows the upper arm current waveform of the A-phase based on the voltage self-balancing topology. The main component of the circulation is the double frequency. Comparing Fig. 20 and

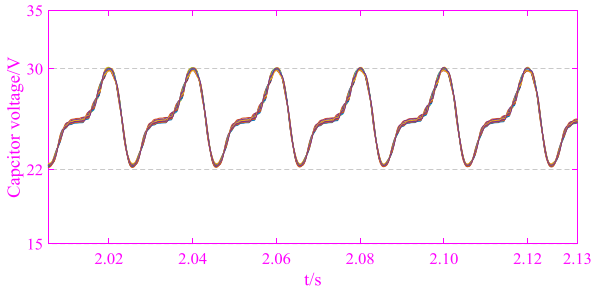


FIGURE 18. Capacitor voltage waveform of voltage self-balancing topology.

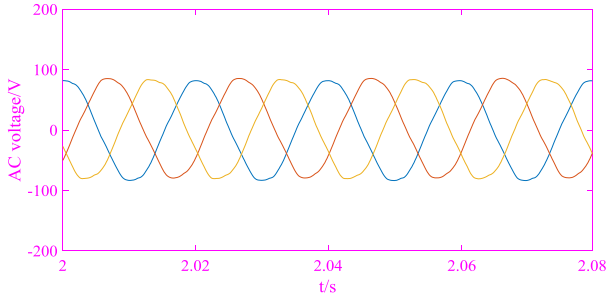


FIGURE 19. AC voltage of voltage self-balancing topology.

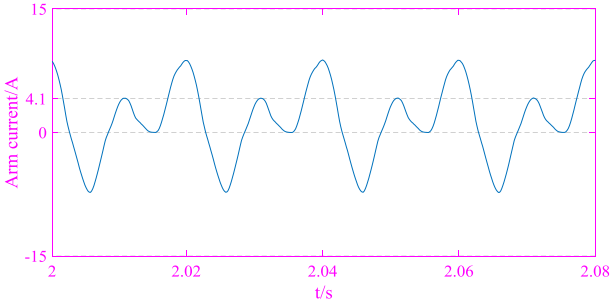


FIGURE 20. Arm current of sorting algorithm.

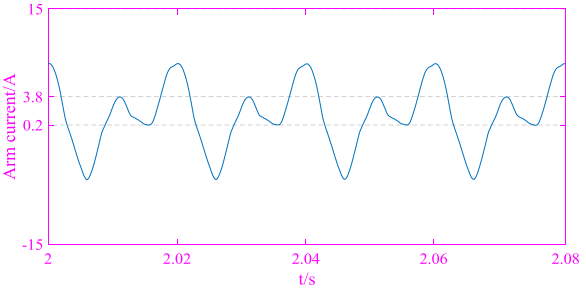


FIGURE 21. Arm current of voltage self-balancing topology.

Fig. 21, the double frequency of the upper arm current of the voltage self-balancing topology is reduced by 12.5% compared with the double frequency of the upper arm current based on the sorting algorithm. Therefore, the voltage self-balancing topology has a better ability to suppress the circulating current.

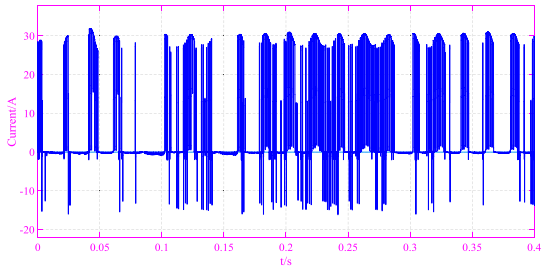


FIGURE 22. Current of voltage balancing circuit loop.

Analysis from the experimental results, the voltage self-balancing MMC topology has a better voltage balancing effect and circulation inhibition ability compared to the MMC system based on the sorting algorithm.

VII. ENGINEERING APPLICATIONS

A. COST VOLTAGE SELF-BALANCING MMC

Fig.22 shows the current of voltage balancing circuit loop and the peak current is 30A. As the current to be withstood increases, the cost of the IGBT increased exponentially, so the cost of the IGBT in the voltage balancing circuit loop is lower than that of the IGBT in the main circuit. Although the bidirectional voltage self-balancing MMC topology adds half the number of IGBTs on the conventional MMC topology, the cost of the IGBTs in the voltage balancing circuit loop is lower, about 10% of the main circuit, and during construction the cost of the converter accounts for about 30% of the total investment in the project. In terms of project cost, the increased cost of the voltage balancing loop is limited, which will only increase the cost of the entire project by about 3%.Even if the cost of the converter is slightly increased, it will not have a substantial impact on the engineering investment.

B. LOSS ANALYSIS

The IGBT loss mainly includes two parts: conduction loss and switching loss. The loss of the voltage self- balancing topology is carried out by using an accurate calculation method proposed in the literature [32].

1) CONDUCTION LOSSES CALCULATION METHOD

The conduction losses of IGBTs and diodes can be expressed as the product of the conduction current and the voltage drop of the switch:

$$P_{T\mathrm{con}} = U_{\mathrm{ce}} I_{\mathrm{c}} = (R_T I_{\mathrm{c}} + U_{\mathrm{ce0}}) I_{\mathrm{c}} \tag{23}$$

$$P_{D\mathrm{con}} = U_{\mathrm{D}} I_{\mathrm{D}} = (R_D I_{\mathrm{D}} + U_{\mathrm{D0}}) I_{\mathrm{D}} \tag{24}$$

where U_{ce} is the voltage between the collector and emitter of the IGBT. I_{c} is the collector current. R_{T} is the IGBT conduction resistance. U_{ce0} is the IGBT latching voltage.

2) SWITCHING LOSS CALCULATION METHOD

Generally, the switching loss of an IGBT is obtained by accumulating an average value of a single switching energy over a certain period. The switching loss of the switch can be expressed by the quadratic polynomial fitting of the conduction current, and the switching loss is approximately linear with the DC side voltage.

$$E_{\mathrm{Tsw}} = E_{\mathrm{on}} + E_{\mathrm{off}} = (a_1 + b_1 I_{\mathrm{c}} + c_1 I_c^2) \frac{U_{\mathrm{dc}}}{U_{\mathrm{dcN}}} \tag{25}$$

where the fitting parameters a_1, b_1, c_1 are from the component parameters provided by the manufacturer. U_{dc} is the instantaneous value of the DC side voltage of the switch. U_{dcN} is the rated value of the DC side voltage. E_{Tsw} is the loss of the IGBT turn-on and turn-off for once.

The IGBT in the voltage balancing circuit loop adopts Fairchild's SGH80N60UFD, with a forward withstand voltage of 600V and a maximum conduction current of 80A. When the system conduction current is 40A, the maximum switching frequency is 20KHz, which meets the parameters requirement of the system. According to SGH80N60UFD's manual data:

The IGBT conduction loss power is:

$$P_{T\mathrm{con}} = U_{\mathrm{ce}} I_{\mathrm{c}} = 2.1V \times 40A \tag{26}$$

The diode conduction loss power is:

$$P_{D\mathrm{con}} = U_{\mathrm{D}} I_{\mathrm{D}} = 1.4V \times 25A \tag{27}$$

The IGBT switching loss power is:

$$E_{\mathrm{Tsw}} = E_{\mathrm{on}} + E_{\mathrm{off}} = 570uJ + 590uJ = 1160uJ \tag{28}$$

In order to verify that the voltage self-balancing MMC topology can reduces the system loss, it is assumed that the IGBT and diode are always in the conduction state, and the IGBT always have switch loss (the switching frequency is calculated according to the maximum switching frequency).

At that moment, the calculated system loss is greater than the actual loss of the system. The total loss generated during ΔT is:

$$\begin{aligned} W_{\mathrm{A\_loss}} &= (P_{T\mathrm{con}} + P_{D\mathrm{con}} + E_{\mathrm{Tsw}} \times 20\mathrm{K})\, \Delta T \times \mathrm{m} \\ &= 4408.2 \Delta T \end{aligned} \tag{29}$$

where m is the number of IGBTs in the voltage balancing circuit loop.

The system loss reduced by voltage self-balancing MMC topology is:

$$\begin{aligned} W_{\mathrm{A\_loss}} \sum_{\mathrm{j=a}}^{\mathrm{c}} &= U_j \times \Delta i_{cir\_j} \times \Delta T = 2400 \times 15 \Delta T \\ &= 108000 \Delta T \end{aligned} \tag{30}$$

where U_j is the single-phase voltage. Δi_{cir_j} is the amplitude of the decrease of the phase-to-phase circulation. And j is a, b, and c.

By comparing equations (29) and (30), it can be concluded that the voltage self-balancing MMC topology can significantly reduce the system loss.

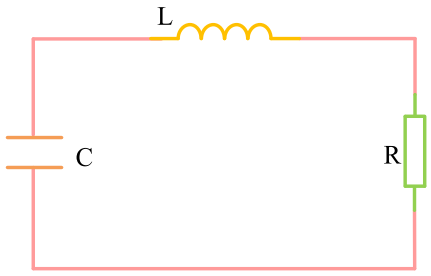


FIGURE 23. Voltage balancing circuit equivalent diagram.

C. INDUCTOR SELECTION VOLTAGE BALANCING CIRCUIT LOOP

The inductor in the voltage balancing circuit loop can suppress the overcurrent during the voltage balancing process and protect the IGBTs and submodule capacitor in the voltage balancing circuit loop. Fig 23 is an voltage balancing circuit of a voltage equalization loop. The voltage balancing circuit loop is equivalent to the RLC series loop, and LC series resonance should be avoided when selecting the inductor, that is:

$$L \neq \frac{1}{w^2 C} \tag{31}$$

C is the capacitance of the sub-module, L is the inductance of the voltage balancing circuit loop, and R is the equivalent resistance of the circuit. According to the circuit theorem KVL:

$$U_c + i\mathrm{R} = L\frac{di}{dt} \tag{32}$$

$$L = \frac{U_\mathrm{c} + i\mathrm{R}}{\mathrm{d}i/\mathrm{d}t} \tag{33}$$

The maximum value of the current in the voltage balancing circuit loop is the rated current value i_p of the IGBT, then the value of L is:

$$L \leq \frac{U_\mathrm{c} + i_\mathrm{p}R}{\mathrm{d}i/\mathrm{d}t} \tag{34}$$

In order to better suppress the overvoltage of the voltage balancing circuit and protect the IGBT in the voltage balancing circuit, the electric inductor in the voltage balancing circuit should use a large inductor as much as possible. Combining equation (34), the electrical induction takes the critical value of the conclusion and satisfies equation (31).

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