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Monolithic GaN Half-Bridge Stages With Integrated Gate Drivers for High Temperature DC-DC Buck Converters

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ABSTRACT This paper presents a GaN based synchronous buck DC-DC converter, which monolithically integrates gate drivers and a half-bridge power stage in a 3-μm enhancement-mode (E-mode) GaN-on-Si process. The fabricated synchronous converter with integrated gate drivers is based on E-mode GaN MIS-HFETs (metal-insulator-semiconductor heterojunction-field-effect-transistors), which have a large gate swing of 10 V due to the insertion of 20 nm high-k gate insulator Al_2O_3. At 100 kHz, the proposed DC-DC integrated circuits (ICs) exhibit good thermal stability at high temperatures up to 250 °C for 25 V down conversion. Furthermore, four different designs (asynchronous and synchronous) including converters with external drivers were systematically evaluated at different input voltages and duty cycles, the GaN-based DC-DC converters with integrated gate drivers exhibit small voltage overshoots and oscillations due to reduced parasitic inductance and chip size. These results validate the advantages of monolithic, lateral integration of half-bridge GaN ICs with gate drivers for high temperature power converters.

INDEX TERMS GaN integration circuits (ICs), high temperature operations, integrated gate drivers, synchronous and asynchronous dc-dc buck converters.

I. INTRODUCTION

High temperature power converters are becoming increasing important in applications under extreme environment, such as electric vehicles, aviation and oil drilling. For electric vehicles, the ambient temperature of the hood is usually above 150 °C, and the temperature near engine can even reach 200 °C. Si-based devices can only work at temperature below 150 °C, however, the superior material properties of wide bandgap (WBG) semiconductors (GaN and SiC) with good thermal conductivity are expected to be excellent candidates for power converters at high temperatures over 200 °C in electrical vehicle applications.

Power integration becomes increasingly essential to fully utilize the superior performance of GaN material due to the reduced parasitic inductance, high power density and high-temperature operation. The lateral channel makes AlGaN/GaN heteroepitaxy structure an excellent candidate for power integrated circuits (ICs), compared with vertical GaN, dMode GaN and SiC technologies [1]. A design towards monolithic integration for low and mid power applications is proposed using Metal Insulator Semiconductor (MIS) or Metal Oxide Semiconductor (MOS) gate MIS-HEMTs (high-electron-mobility-transistors) [2]. A hybrid architecture using recessed gate and an insulator

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TABLE 1. Recent studies of integrated GaN based DC-DC buck converters.

Design	[7]	[8]	[9]	[1]	This work
Year	2014	2016	2016	2017	2019
Technology	0.5 µm E-mode P-AlGaN HEMT	0.15 µm D-mode GaN-HEMT	E-mode GaN-on-SiC	E-mode GaN FETs	3 µm E-mode GaN MIS-HFET
Gate Driver	Integrated	Integrated	Integrated	Integrated	Integrated
Topology	Half-bridge	Half-bridge	Half-bridge	Half-bridge	Half-bridge
$^{a}V_{G,max}$	5 V	0 V	2.5 V	N.A.	10 V
$^{b}V_{G,min}$	0 V	-5 V	-2.5 V	N.A.	0 V
V_{IN}/V_{OUT}	12V/1.8V	20V/14V	25V/12 V	650V/N.A.	25V/4V
Temperature	RT	RT	RT	RT	250 °C
Frequency	3 MHz	100 MHz	20-400 MHz	2 MHz	100 kHz
Area	11.7 mm^2	5.52 mm^2	4 mm^2	48 mm^2	3 mm^2

N.A.=Not Applicable. $^{a}V_{G,max}$ and $^{b}V_{G,min}$ are maximum and minimum driving voltages of integrated drivers.

was used by many studies [3]–[5] for enhancement (E-mode) devices. The recessed E-mode MIS-HFETs are excellent candidates for GaN-based power ICs, which can suppress gate leakage and provide strong immunity to large voltage overshoots or oscillations, especially in high frequency power switching circuits. The insulated gate (V_{GS} over 10 V) could be driven with circuits designed for the mainstream Si and SiC power MOSFETs, without any additional drivers or level shifters.

Monolithic integration of GaN drivers and GaN power transistors is highly recommended for high frequency operation and shows advantages of reduced chip size [6]. Recent studies [1], [7]–[9] have been reported to monolithically integrate gate drivers with power transistors for GaN-based DC-DC buck converters as summarized in Table 1. Most of these studies focus on the low voltage DC-DC converters, especially for point-of-load (POL) devices. However, these integrated GaN converters are only measured at room temperature (RT), or negative drive voltages are needed [8], [9]. Limited reports show high temperature characteristics of integrated GaN converters, which are essential for electrical vehicle applications at high temperatures over 200 °C. In this work, the monolithically integrated GaN-based synchronous buck converter with gate drivers and a half-bridge stage is proposed and experimentally evaluated, which exhibits good stability at high temperatures up to 250 °C, with a large gate swing of 10 V and a relatively small circuit size of 3 mm^2 as well. In addition, the low frequency in this work is caused by current or mobility degradation of recessed channel compared with other works. Fully recessed gate is recommended in this work in GaN ICs platform, and balance should be made between V_{th} of E-mode devices and current degradation using recessed E-mode GaN MIS-HFETs.

In this work, the design, fabrication process and characterization of the integrated gate drivers using E-mode AlGaN/GaN MIS-HFETs are proposed, the gate drivers consist of direct coupled FET logic (DCFL) inverters [10]–[13], a buffer stage [7], [14], [15]. The fabricated synchronous converter with monolithically integrated GaN drivers and one half-bridge power stage (V_{IN} = 15 to 25 V at 100 kHz) shows less temperature degradation at 250 °C at various duty cycles and input voltages. Results in this work validate the advantages of E-mode AlGaN/GaN MIS-HFETs for monolithic integration ICs in achieving high temperature, high power density and high efficiency power converters.

II. DEVICE FABRICATION AND CHARCTERISTICS

This section describes the fabrication process and device characteristics of both E-mode and D-mode devices at room temperatures and also high temperatures.

A. FABRICATION PROCESS

The GaN ICs were fabricated on GaN-on-Si substrate consisting of a 4.2 μm GaN buffer, a 21 nm AlGaN and 1 nm GaN cap layer. The process started with mesa etching, and a 100 nm SiN_x was deposited as an etching hard mask for E-mode gate recess, and digital etching [16] was performed to fully etch the barrier layer to realize E-mode devices. After SiN_x removal by buffered oxide etch (BOE), Au-free source and drain contacts [17], [18] were formed by Ti/Al/Ni/TiN (22.5/90/45/100 nm) evaporation followed by a rapid thermal anneal at 900 °C. Then, a 20 nm atomic layer deposition (ALD) Al_2O_3 gate dielectric layer for E/D-mode devices was deposited followed by the evaporation of Ni/TiN as the gate metal. Lastly, a 100 nm SiN_x was deposited as inter-metal dielectrics and a 200 nm Al metal was finally evaporated as metal connection on GaN ICs platform.

B. DEVICE CHARACTERISTICS

Fig. 1 shows the DC characteristics of discrete E-mode and D-mode devices which were fabricated on the same chip with GaN gate drivers and power transistors. At 25 °C, the threshold voltage (V_{th}) is +1.5 V and the maximum output current ($I_{DS,\,max}$) is 240 mA/mm (V_{DS} = 10 V) for E-mode devices, whereas V_{th} is −7.1 V and $I_{DS,\,max}$ is 480 mA/mm (V_{DS} = 10 V) for D-mode devices. When the temperature is increased up to 250 °C, both D-mode and E-mode devices show degraded performance. At 250 °C, the V_{th} is

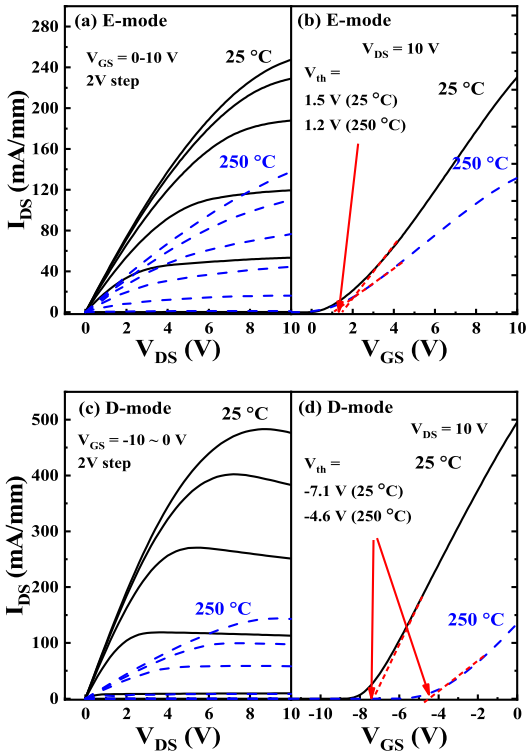

FIGURE 1. Output and transfer characteristics of E-mode MIS-HFETs (a) and (b), D-mode MIS-HEMTs (c) and (d) at 25 °C and 250 °C, respectively. (Device dimension: L_{GS} /W_G /L_G /L_{GD} = 5/50/3/10 μm).

+1.2 V and the $I_{DS,\,max}$ decreases to 135 mA/mm for E-mode devices, whereas D-mode MIS-HEMTs show a V_{th} of −4.6 V and a decreased $I_{DS,\,max}$ of 143 mA/mm. The decrease of output current at high temperature is due to degradation of channel mobility [19], [20]. The GaN-based E-mode MIS-HFETs show better V_{th}-thermal stabilities than D-mode MIS-HEMTs, which is attributed to the absence of polarized barrier layer in E-mode HFETs. The temperature-induced V_{th} instability in D-mode AlGaN/GaN MIS-HEMTs is mainly caused by Al_2O_3/AlGaN interface traps [21], [22], and the positive shift of threshold voltage of D-mode MIS-HEMTs might be caused by the strain relaxation in AlGaN barrier above 250 °C [23]. Efforts should be made to improve the reliability of dielectric at high temperatures, and to provide a promising pathway toward reliable and stable insulated GaN-based ICs for high temperature applications.

III. MONOLITHIC GATE DRIVERS WITH INTEGRATED GAN HALF-BRIDGE POWER STAGES

The monolithic half-bridge stage shown in Fig. 2 includes a high-side transistor (H_S) and a low-side transistor (L_S). At the first half period, when the high-side transistor is at on-state (V_{GS_H} is at high voltage and V_{DS_H} is at low voltage) and the low-side transistor is at off-state (V_{GS_L} is at low voltage and V_{DS_L} is at high voltage), the output voltage (V_{OUT}) is obtained by deducting the voltage drop of the inductor L from an input voltage (V_{IN}). At the second half period, when the

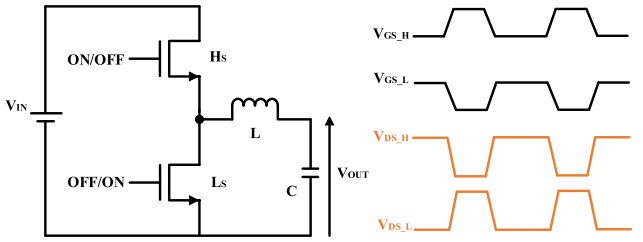

FIGURE 2. Circuit diagram and switch timing chart of synchronous DC-DC buck converter with a half-bridge stage [7]. V_{GS_H} and V_{DS_H} are gate to source voltage and drain to source voltage of the high-side transistor H_S, respectively. V_{GS_L} and V_{DS_L} are gate to source voltage and drain to source voltage of the low-side transistor L_S, respectively.

high-side transistor is at off-state (V_{GS_H} is at low voltage and V_{DS_H} is at high voltage), while the low-side transistor is at on-state (V_{GS_L} is at high voltage and V_{DS_L} is at low voltage), the V_{OUT} is equal to the voltage drop of the inductor. The total area under the inductor voltage is zero whenever the converter operates in steady states, V_L refers to the voltage of the inductor and D is the duty cycle of the input of the high-side transistor, so equation (1) can be obtained:

$$\begin{aligned} \int_0^{T_s} v_L(t)\,dt &= 0 \\ (V_{IN} - V_{OUT}) \times \mathrm{D} + (-V_{OUT}) \times (1-D) &= 0 \\ V_{OUT} &= DV_{IN} \end{aligned} \quad (1)$$

The synchronous DC-DC converter down-converts the input voltage through changing the duty cycles of the high-side transistor. Both high-side driver and low-side driver need to provide the required gate to source voltages to switch on the corresponding power transistors. The low-side driver is easy to control since the source of the low-side transistor is grounded. However, since the source voltage of the high-side transistor is switching between zero and input voltage V_{IN}, the high-side driver should provide efficient level shift to ensure required gate to source voltage of the high-side transistor. This section presents integrated gate drivers for DC-DC buck converters, the mechanism of the bootstrapped driver is introduced in section III-A, the asynchronous and synchronous buck converters with integrated gate drivers are illustrated in section III-B and III-C, respectively.

A. BOOTSTRAP DRVIER

Fig. 3 shows the circuit diagram of a bootstrap driver, and it operates as followings: when the high-side transistor H_S is at off-state, and the low-side transistor L_S is at on-state, the V_S is pulled down to the ground and the V_{DD} power supply charges the bootstrap capacitor C_{BT} through bootstrap diode D_{BT} (the charging path is shown as the red line). On the other hand, when the V_S is pulled up to a higher voltage by the switching-on process of the high side transistor H_S (the low-side transistor L_S is at off-state), the increased V_S will reverse the bootstrap diode D_{BT} and block the rail voltage from V_{DD}, and the bootstrap capacitor discharges current through blue

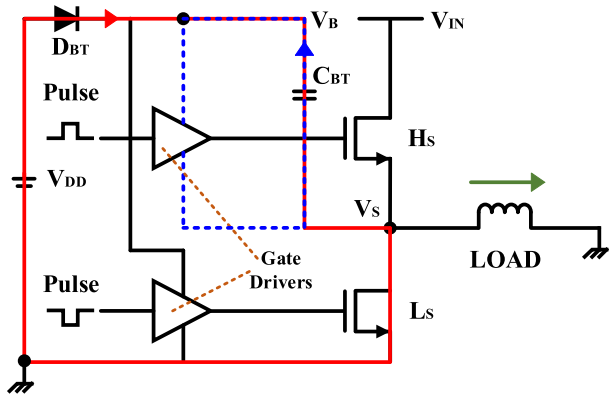

FIGURE 3. Circuit diagram of a bootstrap driver with a half-bridge stage (red line and blue line are the charging and discharging current paths of the bootstrap driver, respectively).

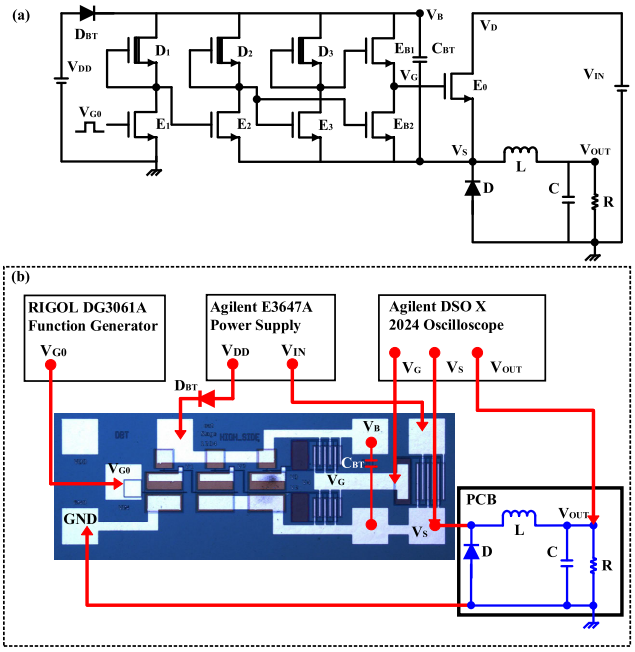

FIGURE 4. (a) The circuit diagram of the GaN-based asynchronous DC-DC buck converter with an integrated gate driver. (b) The experimental setup and microphotograph of the integrated circuits. (The parameters of discrete components are: L=1 mH, C=20 μF, R=500 Ω, V_{DD} = 10 V, V_{IN} = 20 V, f=100 kHz, D=0.5, the threshold voltage V_F of the discrete diodes D and D_{BT} is +0.7 V, C_{BT} = 22 nF).

line, the floating V_{BS} supply maintains the required gate to source voltage to fully turn on the high-side transistor H_S.

B. ASYCHRONOUS DC-DC BUCK CONVERTER WITH AN INTEGRATED GATE DRVIER

Fig. 4 (a) shows the circuit diagram of a GaN based asynchronous DC-DC buck converter with an integrated gate driver. The gate driver and the power transistor E_0 were integrated on one chip. The experimental setup is shown in Fig. 4 (b), the inductor L, diode D, capacitor C and the load resistor R were integrated on a PCB board, the integrated gate driver and power transistor E_0 were externally connected with

TABLE 2. Device parameters for asynchronous buck converter.

Components	Devices	Width (μm)
DCFL inverters	D_1, D_2, D_3	5
	E_1, E_2, E_3	200
Buffer stage	E_{B1}, E_{B2}	500
Power transistor	E_0	1000

The gate length L_G is 3 μm for all devices.

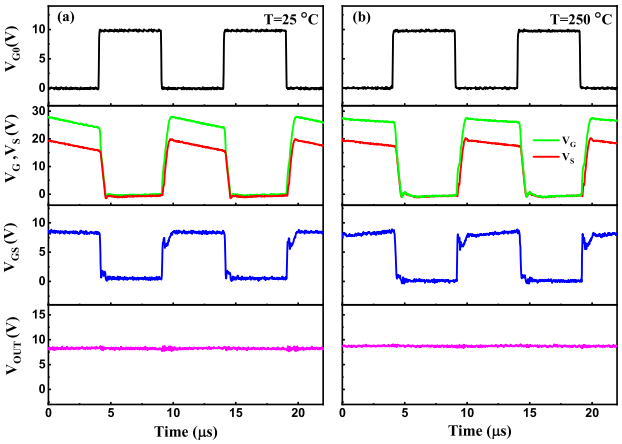

FIGURE 5. Dynamic waveforms of the GaN-based asynchronous DC-DC converter in Fig. 4 at room temperature 25 °C (a) and 250 °C (b), respectively, when duty cycle is 0.5. V_{G0} is the input gate signal of the driver, V_G is the output voltage of the gate driver, V_S is the source voltage of the power transistor E_0, and the V_{GS} voltage between V_G and V_S is equal to the gate to source voltage of power transistor E_0.

the bootstrap diode D_{BT}, bootstrap capacitor C_{BT} and components of PCB board using probes. The high temperature tests were also carried out to study the thermal properties of the proposed converters. During the high temperature tests, the GaN chip with integrated gate drivers and power transistor E_0 were heated on the hot stage, whereas C_{BT}, D_{BT} and the PCB board were off the probing stage. The parameters of the integrated asynchronous buck converter are shown in Table 2, which are based on our previous work [18]. The integrated driver consists of direct coupled FET logic (DCFL) inverters and a buffer stage. To be specific, one DCFL inverter contains a D-mode device with gate and source connected, and an E-mode device as well. The buffer stage consists of two E-mode devices E_{B1} and E_{B2} for high speed switching transition.

Fig. 5 shows the dynamic waveforms of the integrated buck converter in Fig. 4. The pull-up voltage V_{DD} is 10 V and the input voltage of the converter V_{IN} is 20 V. When the input of the gate driver V_{G0} is at a high voltage of 10 V, the output of the driver V_G is at low voltage around 0 V and the power transistor E_0 is at off-state. Hence, the floating source V_S is pulled down to the ground through the discrete diode D. On the other hand, when the input voltage of the driver V_{G0} is 0 V, the high output voltage of V_G will turn on the power transistor E_0, and therefore V_S is pulled up to

TABLE 3. Device parameters for synchronous buck converter.

Components	Devices	Width (μm)
DCFL inverters(HS)	D_1, D_2, D_3	5
	E_1, E_2, E_3	200
Buffer stage(HS)	E_{B1}, E_{B2}	500
DCFL inverters(LS)	D_4, D_5	5
	E_4, E_5	200
Buffer stage(LS)	E_{B3}, E_{B4}	500
Power transistor	E_{HS}, E_{LS}	1000

The gate length L_G is 3 μm for all devices.

V_{IN} = 20 V. The bootstrap driver will reverse the bootstrap diode D_{BT} and the floating V_{BS} supply pull up the V_G to a higher voltage, which provides the required gate to source voltage V_{GS} in order to maintain the power transistor E_0 at on-state, as discussed in the previous session. The dynamic waveforms V_{G0}, V_G, V_S and calculated V_{GS} are shown in Fig. 5 (a) at room temperature and Fig. 5 (b) at 250 °C, respectively. At 100 kHz, the output voltage waveforms of the driver V_{GS} can function well with small voltage overshoots and oscillations even at high temperature 250 °C, owing to full integration of the gate driver and power transistor, this indicates the advantages of using GaN MIS-HFETs technology in GaN ICs platform. Additionally, the maximum voltage of V_{GS} (around 9 V) is slightly lower than V_{DD} = 10 V, which is caused by the voltage drop of the diode (V_F = + 0.7 V) during the charging process of the bootstrap driver, since the open-loop test shows a maximum voltage of 10 V with V_S grounded. In addition, it is found that the etch depth of the barrier layer is essential, when we use recessed gate with insulators to achieve GaN ICs for power converters, especially for gate drivers with multi-stages. What's more, the full recess of the barrier is recommended, because the output of the drivers with partial recess can easily work at the first stage but hardly at the following stages. However, if the channel is over-recessed, the current degradation and operating frequency might be concerns, so balance should be made between V_{th} of E-mode devices and current/mobility degradation.

C. SYNCHRONOUS DC-DC BUCK CONVERTER WITH INTEGRATED GATE DRVIERS AND A HALF-BRIDGE STAGE

The synchronous buck converter with a half-bridge power stage is an important topology in power converter configurations. The detailed parameters of the proposed half-bridge power stage with integrated gate drivers are listed in Table 3.

The circuit diagram of the proposed synchronous buck converter is shown in Fig. 6 (a), and Fig. 6 (b) shows the experimental setup and microphotograph of the synchronous buck converter. In order to compare different designs (asynchronous and synchronous) of buck converters, we use the same external load side as Fig.4 in this work, including a discrete diode D, an inductance L, a load capacitor C and a resistor R in the PCB board. The synchronous buck converter

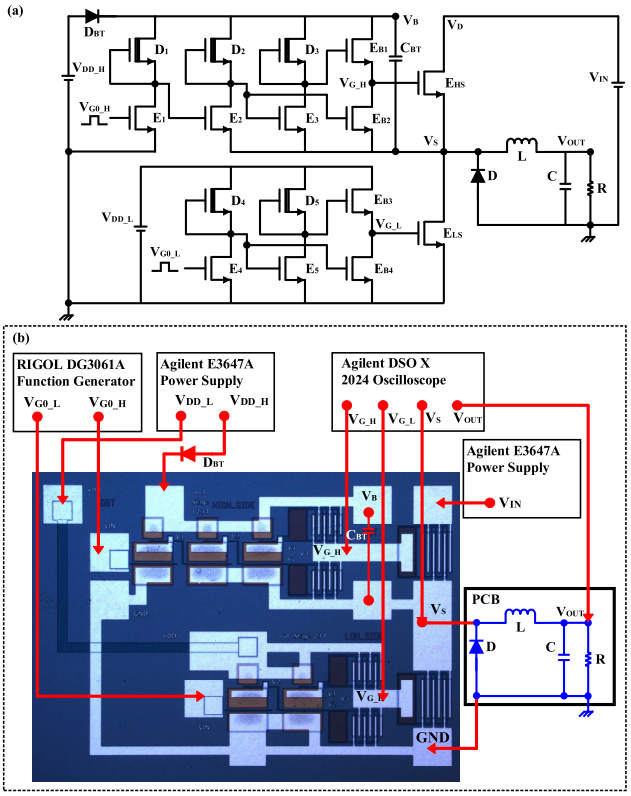

FIGURE 6. (a). The circuit diagram of GaN-based synchronous DC-DC buck converter with integrated gate drivers. (b) The experimental setup and microphotograph of the proposed circuit. (The parameters of discrete components are: L=1 mH, C=20 μF, R=500 Ω. V_{DD} = 10 V, V_{IN} = 20 V, f=100 kHz, duty cycle=0.5, the threshold voltage V_F of the discrete diodes D and D_{BT} is +0.7 V, C_{BT} = 22 nF).

integrates a high-side gate driver, a low-side driver, a high-side power transistor E_{HS} and a low-side power transistor E_{LS}. Normally, the inputs of high-side driver V_{G0_H} and low-side driver V_{G0_L} are reversely oriented and have a dead time between them in order to avoid short circuit or shoot-through failure [24], [25]. In this work, the input signals of both high-side and low-side drivers are in the same direction for simplicity due to the different numbers of DCFL inverters (the stage number is odd in the high-side driver and even in the low-side driver). That means the output voltage of the high-side driver V_{G_H} is reverse with the input voltage of the high-side driver V_{G0_H}, whereas the output voltage of the low-side driver V_{G_L} changes in the same direction with the input voltage V_{G0_L}. Meanwhile, the synchronous buck converter has a dead time of 0.25 μs between V_{G0_H} and V_{G0_L} to avoid simultaneous conduction of two power transistors E_{HS} and E_{LS}, and 0.25 μs is chosen to prevent short circuit or shoot-through failure because the proposed driver in Fig. 4 shows propagation delay times of less than 0.22 μs at various temperatures, similar with rise times and fall times of less than 0.25 μs at various temperatures in our previous work [18].

Fig. 7 (a) and (b) show dynamic waveforms of the GaN-based synchronous buck converter at 25 °C and 250 °C,

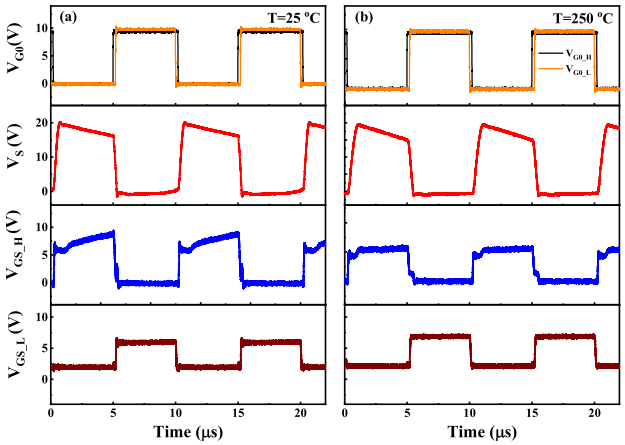

FIGURE 7. Dynamic waveforms of GaN-based synchronous DC-DC converter in Fig. 6 at room temperature 25 °C (a) and 250 °C (b), respectively. V_{G0_H} and V_{G_H} are the input and output voltages of the high-side driver, respectively. V_{G0_L} and V_{G_L} are the input and output voltages of the low-side driver, respectively. V_{GS_H} (voltage between V_{G_H} and V_S) is equal to the gate to source voltage of high-side transistor E_{HS}, whereas V_{GS_L} or V_{G_L} is the gate to source voltage of the low-side transistor E_{LS}.

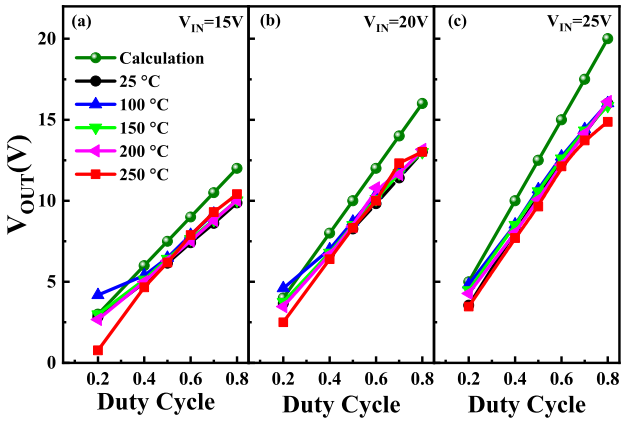

FIGURE 8. Experimental results of the asynchronous converter in Fig. 4 at various duty cycles and temperatures, f=100 kHz. (a) V_{IN} = 15 V, (b) V_{IN} = 20 V and (c) V_{IN} = 25 V.

respectively. The input signal V_{G0_H} has a 0.25 μs extension over V_{G0_L} during switching-on and switching-off transition, this ensures a 0.25 μs dead time control between the high-side transistor E_{HS} and low-side transistor E_{LS}. As the similar discussion in part B, when the input signals of high-side driver V_{G0_H} and low-side driver V_{G0_L} are both at a high voltage of 10 V, the corresponding V_{G_H} and V_{G_L} are at low voltage and high voltage, respectively. Hence, the high-side transistor E_{HS} is at off-state and the low-side transistor E_{LS} is at on-state, V_S is pulled down to the ground through the low-side transistor E_{LS}. On the other hand, when V_{G0_H} and V_{G0_L} are both equal to 0 V, this leads to a high voltage of 10 V at V_{G_H} and a low voltage at V_{G_L}, respectively. Therefore, the high-side transistor E_{HS} is switched on and the low-side transistor E_{LS} is switched off, and the floating V_S is consequently pulled up to V_{IN}, enabling the bootstrap driver to maintain specific gate to source voltage of the high-side transistor E_{HS} as the previous discussion. The proposed half-bridge transistors with integrated high-side and low-side drivers work well at 25 °C and 250 °C with small voltage overshoots and oscillations in Fig. 7 (a) and Fig. 7 (b), respectively. In addition, the V_{GS_H} of the high-side driver is a little bit lower than V_{GS} in Fig. 5 due to the additional low-side loop. This is because the maximum voltage of V_{GS} or V_{GS_H} is determined by voltage bias supply V_{BS} of the bootstrap driver. The V_{BS} (during charging process of the bootstrap) in Fig. 5 is equal to V_{DD}-V_F, V_F is the threshold voltage of the diode D_{BT}, whereas V_{BS} of the synchronous converter in Fig. 7 is equal to V_{DD_H}-V_F-V_{DS,ON_LS} due to the existence of the low-side transistor E_{LS} during the charging process of the bootstrap driver, where V_{DS,ON_LS} is on-state drain to source voltage of the low-side transistor E_{LS}. This possibly explain the lower V_{GS_H} in Fig. 7, and a lower V_{GS_L} can also be explained by the existence of high-side loop as the similar discussion. Nevertheless, this does not affect the switching performance of the power transistors and hence converter performance in the following Part IV.

IV. CONVERTER RESULTS AND DISCUSSIONS

Fig. 8 shows results of the asynchronous converter in Fig. 4 over a wide temperature range from 25 °C to 250 °C, the calculated values using equation (1) were also plotted for comparison. Here, the duty cycles of output waveforms of the bootstrap driver V_G are used for the simplicity. The output voltages of the asynchronous buck converter increase with increasing duty cycles, and the overall performance is close to theoretical lines. Moreover, there is only small degradation of output voltages at high temperatures up to 250 °C, this indicates the good performance of GaN ICs for high temperature power converters at extreme environment. In addition, there is some dispersion of output voltages at a low duty cycle of 0.2, which might be caused by asynchronous topology and will be discussed later.

The discrepancies between experimental and calculated values in Fig. 8 are observed with increasing input voltages and duty cycles. At room temperature with V_{IN} = 15 V, the discrepancy at a duty cycle of 0.8 is 2 V, this value increases up to 3 V, 4 V at V_{IN} = 20 V, 25 V, respectively. The possible cause of this phenomena is due to increased dynamic R_{ON} with increasing V_{IN} and duty cycles, the increased dynamic R_{ON} or current collapse is mainly caused by defects traps [26]–[28].

As shown in Fig. 9 (a), V_{IN} = 20 V with different duty cycles of 0.2, 0.5 and 0.8, V_{DS} refers to the drain to source voltage of the power transistor E_0 and is normally as low as zero at on-state in an ideal case. However, when the power transistor is at on-state, the increased R_{ON} or V_{DS} will change equation (1) to equation (2). Compared with equation (1), the output voltage decreases at higher duty cycles due to increased R_{ON} or $V_{DS,ON}$, this can explain the decreased output voltages at high duty cycles in Fig. 8. On the other hand, the input voltage can also affect dynamic R_{ON} as shown

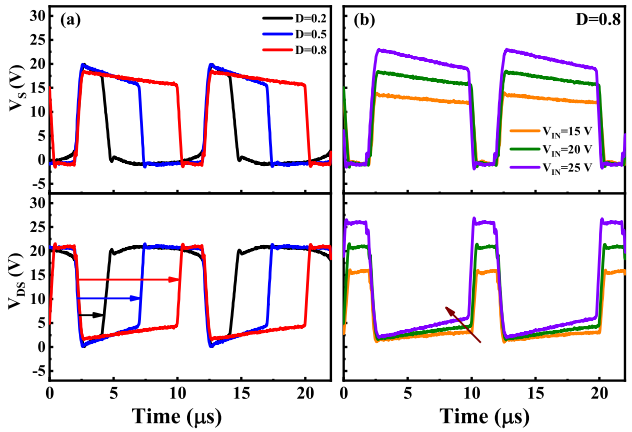

FIGURE 9. (a) Dynamic V_S and V_{DS} at different duty cycles 0.2, 0.5 and 0.8 at V_{IN} = 20 V. (b) Dynamic V_S and V_{DS} at different input voltages of 15 V, 20 V and 25 V with a duty cycle of 0.8. Temperature=25 °C, f=100 kHz.

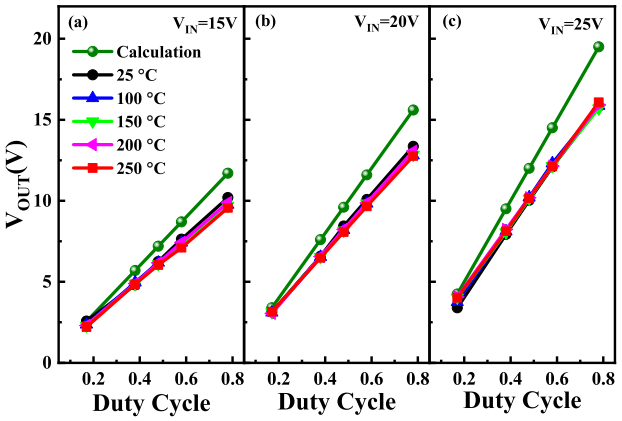

FIGURE 10. Experimental results of the synchronous converter in Fig. 6 at various duty cycles and temperatures at f=100 kHz. (a) V_{IN} = 15 V, (b) V_{IN} = 20 V and (c) V_{IN} = 25 V.

in Fig. 9 (b), with a duty cycle of 0.8, the on-state voltage $V_{DS,ON}$ or dynamic R_{ON} increases slightly when the input voltage varies from 15 V to 25 V. This might be caused by off-state drain voltage induced traps, which may promote the trapping of electrons under the gate and in the gate-drain access region [29]. When the power transistor is at off-state with a positive drain voltage, which is equal to V_{IN} in the converter, electrons are captured by defect traps. When the power transistor switches on, the trapped electrons cannot escape immediately and lead to a reduced current or an increased R_{ON}, and a higher V_{IN} of 25 V leads to more electrons traps at off-state and an increased R_{ON} compared with a lower V_{IN} of 15 V in Fig. 9 (b). This possibly explains the increased discrepancies between calculation and experiment results at higher input voltages in Fig. 8.

$$(V_{IN} - V_{OUT} - V_{DS,ON}) \times \mathrm{D} + (-V_{OUT}) \times (1 - D) = 0$$
$$V_{OUT} = D(V_{IN} - V_{DS,ON}) \quad (2)$$

Fig. 10 shows the synchronous converter results in Fig. 6 over a wide temperature range from 25 °C to 250 °C, and here we use the duty cycle of the output waveform V_{GS_H} of the high side driver. The output voltages of the synchronous buck converter show the similar trends with the asynchronous converter. However, the synchronous buck converter with an integrated half-bridge power stage shows more stable and uniform performance under various temperatures from 25 °C to 250 °C, and it shows less temperature dispersion not only at different duty cycles, but also at different input voltages compared with the results of the asynchronous converter in Fig. 8. The stable performance at high temperatures outstands the excellent candidate of the synchronous converter with a half-bridge stage in power converter applications at extreme environment.

The reason why the integrated synchronous converter shows better temperature performance over the integrated asynchronous converter can be explained as the follows. In Fig. 8, the asynchronous converter shows some temperature dispersion especially at a low duty cycle of 0.2, in order to analyze the difference between two topologies, here we take duty cycle D=0.2 as an example. Fig. 11 (a) and Fig. 11 (b) present the dynamic V_S and V_{DS} of the asynchronous converter and synchronous converter at various temperatures from 25 °C to 250 °C, respectively. It can be obviously observed that the synchronous converter shows better V_S and V_{DS} waveforms at various temperatures, especially during the switching-on transition of the high-side transistor. The low-side transistor E_{LS} of the synchronous converter in Fig. 6, conducts load current instead of the discrete D of the asynchronous converter in Fig. 4, here we do not consider the small conduction loss of the discrete diode D during deadtimes. When the high-side transistor E_{HS} is at off-state, the large current of the low-side transistor E_{LS} will speed up the discharging process of the converter. On the other hand, the large discharging current of low-side transistor E_{LS} will accelerate to pull up the floating V_S to V_{IN} and speed up the switching-on transition of the high-side transistor E_{HS}. This can explain the good stability of the synchronous converter at various duty cycles and temperatures in Fig. 10.

The excellent performance of the synchronous buck converter with integrated gate drivers and a half-bridge stage emphasizes the importance of the full integration design on a single chip, especially for high temperature operations in electrical vehicle applications. In order to fully understand the advantages of GaN ICs, both asynchronous and synchronous DC-DC buck converters using external drivers were experimentally compared but with discrete GaN based E-mode MIS-HFETs, which were fabricated on the same chip with the integrated circuits in Fig. 4 and Fig. 6. The external drivers used in this work are Texas Instruments LM5113, and the output voltages of logic high V_{OH} and logic low V_{OL} are 5 V and 0 V, respectively. Besides, the external drivers have limited temperature operation of less than 150 °C, so the comparison was carried out only at room temperature.

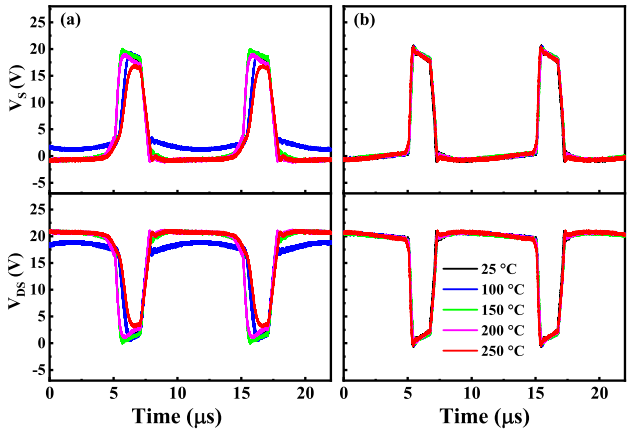

FIGURE 11. Dynamic V_S and V_{DS} of (a) asynchronous converter in Fig. 4 and (b) synchronous converter in Fig. 6 at various temperatures (V_{DS} is the drain to source voltage of the high-side transistor E_{HS}). Duty cycle D=0.2, V_{IN} = 20 V, f=100 kHz.

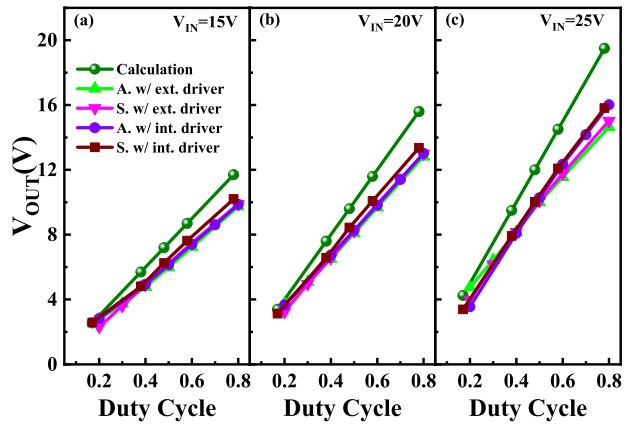

FIGURE 12. Converters comparison between integrated drivers and external drivers. (a) V_{IN} = 15 V, (b) V_{IN} = 20 V and (c) V_{IN} = 25 V. Four different designs of converters, including asynchronous converter with external driver (A. w/ ext. driver), synchronous converter with external driver (S. w/ ext. driver), asynchronous converter with integrated driver (A. w/ int. driver in Fig. 4). and synchronous converter with integrated drivers (S. w/ int. driver in Fig. 6).

At room temperature, Fig. 12 compares four different designs for the buck converters, asynchronous and synchronous converters with external drivers, asynchronous (Fig. 4) and synchronous (Fig. 6) converters with integrated drivers, respectively. The latter two converters integrate power transistors, whereas the two converters with external drivers were externally connected with E-mode power transistors, which were fabricated on the same chip with GaN ICs in Fig. 4 and Fig. 6, and they have the same gate width of 1000 μm with power transistors $E_0/E_{HS}/E_{LS}$. In addition, the same PCB board in Fig. 4 and Fig. 6 was used in converters with external drivers in order to study the impact of different drivers on the performance of the converters. In Fig. 12 (a) and (b), the synchronous converter with integrated drivers shows slightly higher output voltages, owing to high-speed transition and low R_{ON} as the previous discussion. At V_{IN} = 25 V in Fig. 12 (c), converters with

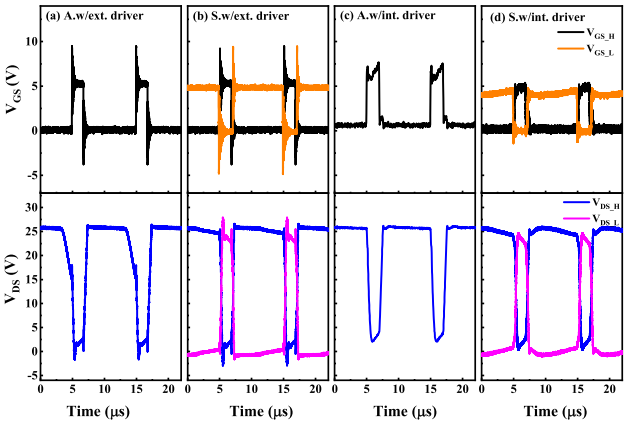

FIGURE 13. At room temperature, dynamic V_{GS} and V_{DS} of (a) asynchronous converter w/ external driver, (b) synchronous converter w/ external drivers, (c) asynchronous converter w/ integrated driver in Fig. 4 and (d) synchronous converter w/ integrated drivers in Fig. 6. D=0.2, V_{IN} = 25 V, f=100 kHz. V_{GS_H}/V_{GS_L} and V_{DS_H}/V_{DS_L} refer to gate to source voltage and drain to source voltage of high-side/low-side transistors, respectively.

integrated drivers exhibit higher output voltages than converters with external drivers, and the discrepancies increase with increasing duty cycles. In addition, both asynchronous and synchronous converters with integrated drivers show similar output voltages at 25 V, which is attributed to the role of increased dynamic R_{ON} caused by high input voltages.

Even though there are no obvious output voltage differences at low duty cycles among converters with external drivers and integrated drivers in Fig. 12, the dynamic waveforms vary a lot from each other. Fig. 13 shows dynamic V_{GS} and V_{DS} waveforms of the high-side transistor in four different converters with a duty cycle of 0.2 at V_{IN} = 25 V. Converters with integrated drivers in Fig. 13 (c) and Fig. 13 (d) show small gate overshoots and oscillations, while converters with external drivers in Fig. 13 (a) and Fig. (b) exhibit obvious gate voltage V_{GS} overshoots up to 10 V or undershoots around negative −5 V, and obvious voltage oscillations as well. The large gate overshoots or undershoots can seriously damage or breakdown switching transistors, especially for low gate voltage swing transistors [30], such as HEMTs or P-GaN HEMTs, which usually show $V_{G,max}$ less than 7 V [29]. The voltage overshoots and oscillations in external drivers are caused by the increased parasitic inductance through external connection. Besides, there are also serious drain to source V_{DS} overshoots due to overshoots of V_{GS} signal in converters with external drivers, which will impact the accuracy of the output voltages to some extent. What's more, there is obvious waveform distortion of V_{DS} for the asynchronous converter with the external driver in Fig. 13 (a) before the high-side transistor switches on. This might be caused by low charging and discharging current at a low duty cycle of 0.2, the synchronous converter with external drivers can solve the problem owing to the low-side loop of the synchronous topology in Fig. 13 (b), the high duty cycle D=0.8 of the low-side transistor can maintain the V_S at

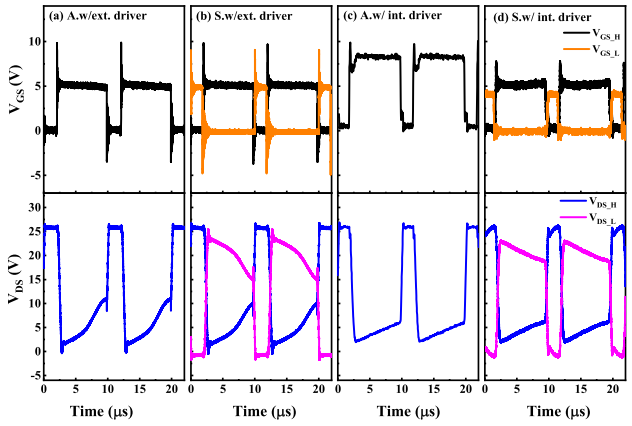

FIGURE 14. At room temperature, V_{GS} and V_{DS} of (a) asynchronous converter w/ external driver, (b) synchronous converter w/ external drivers, (c) asynchronous converter w/ integrated driver in Fig. 4 and (d) synchronous converter w/ integrated drivers in Fig. 6. D=0.8, V_{IN} = 25 V, f=100 kHz.

0 V through E_{LS} instead of the discrete diode D. However, the asynchronous converter in Fig. 13 (c) does not have this problem due to the integrated driver, which acts as a current booster even at low duty cycles.

Fig. 14 shows dynamic V_{GS} and V_{DS} waveforms of four different converters with a duty cycle of 0.8 at V_{IN} = 25 V. Besides the similar overshoots and oscillation as the previous discussion, converters with external drivers show obvious degradation of dynamic R_{ON} or $V_{DS,ON}$ in Fig. 14 (a) and Fig. 14 (b). The possible reason might be due to the degradation of dynamic R_{ON} with increased switching loss or increased parasitic inductance by external connection, the increased power loss will be more serious and lead to self-heating problems at high input voltage of 25 V. This will consequently degrade dynamic R_{ON} and cause output reduction as shown in Fig. 12 (c). Overall, dynamic waveforms in Fig. 13 and Fig. 14 (despite of low maximum V_{GS} as the previous discussion) emphasize the importance of the full integration of gate drivers and power transistors, to reduce the parasitic inductance, power loss and chip size as well.

V. CONCLUSION

Power integration is essential to fully utilize the advantages of GaN technologies, especially at high temperatures over 200 °C for electrical vehicle applications. This paper addresses the integration of gate drivers with a half-bridge stage based on E-mode GaN MIS-HFETs. The asynchronous and synchronous buck DC-DC converters with integrated gate drivers were evaluated at high temperatures from 25 °C to 250 °C with a frequency of 100 kHz, both converters can operate at high temperatures with an input voltage from 15 V to 25 V. However, the synchronous buck converter with a half-bridge stage shows better stability at various temperatures, duty cycles and input voltages due to the advantages of fast switching transition of the topology. Moreover, the asynchronous and synchronous buck converters with external drivers were also tested and compared, the large voltage overshoots and oscillations were observed and can seriously affect the dynamic waveforms of the converters at low duty cycles and at a high input voltage of 25 V. These results emphasize the importance of full integration ICs on a single chip in achieving high temperature, high power density and high efficiency power converters.

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(Miao Cui and Ruize Sun contributed equally to this work.)

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