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Novel Quadruple Cross-Coupled Memory Cell Designs With Protection Against Single Event Upsets and Double-Node Upsets

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ABSTRACT This paper presents two novel quadruple cross-coupled memory cell designs, namely QCCM10T and QCCM12T, with protection against single event upsets (SEUs) and double-node upsets (DNUs). First, the QCCM10T cell consisting of four cross-coupled input-split inverters is proposed. The cell achieves full SEU tolerance and partial DNU tolerance through a novel feedback mechanism among its internal nodes. It also has a low cost in terms of area and power dissipation mainly due to the use of only a few transistors. Next, based on the QCCM10T cell, the QCCM12T cell is proposed that uses two extra access transistors. The QCCM12T cell has a reduced read-and-write access time with the same soft error tolerance when compared to the QCCM10T cell. Simulation results demonstrate the robustness of the proposed memory cells. Moreover, compared with the state-of-the-art hardened memory cells, the proposed QCCM12T cell saves 28.59% write access time, 55.83% read access time, and 4.46% power dissipation at the cost of 4.04% silicon area on average.

INDEX TERMS Double-node upset, memory cell, radiation hardening, single event upset, soft error.

I. INTRODUCTION

As one of the most extensively used memory devices, *static random access memories* (*SRAMs*) play an increasingly important role in modern circuits and systems. Meanwhile, SRAM-circuit integration and performance in nano-scale CMOS technologies have significantly improved. However, the aggressive shrinking of transistor feature sizes makes modern advanced SRAMs more and more sensitive to soft errors caused by the strike of particles, such as protons, neutrons, heavy ions, electrons, muons, and alpha particles [1]. Soft errors can lead to data corruptions, execution errors, or even system crashes in the worst case [2]. The recent adoption of FinFET technologies can reduce the soft error rate at transistor or cell level [3]. However, this feature of FinFET-based circuits does not exempt designers to provide valuable and scalable solutions for soft error tolerance, especially for safety-critical applications in harsh environments. Therefore, SRAM-circuit reliability caused by soft errors is still an increasing concern.

In a combinational logic circuit, when a particle strikes a sensitive node in a logic gate, the collected charges may cause a transient pulse, i.e., a *single event transient* (*SET*), at the output of the struck logic gate. Subsequently, the SET pulse may propagate through the downstream logic gates arriving at a storage element, and the pulse may be captured, thus leading to invalid value-retention. For a storage module such as a memory cell or a flip-flop, particle strike may result in the state change of a single node, thus leading to a soft error. This is called a *single event upset* (*SEU*). However, in modern advanced nano-scale CMOS technologies, the aggressive shrinking of transistor feature sizes can make circuit

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integration higher and circuit node-spacing smaller. As a result, due to charge-sharing, the strike of one particle may simultaneously change the states of two nodes in a storage element, which is called a *double-node upset* (*DNU*). SEUs and DNUs may cause storage elements to retain incorrect values, resulting in potential errors and failures in circuits and systems. Therefore, to improve robustness of circuits and systems, there is a strong need for IC designers and manufacturers to perform radiation hardening against SEUs and DNUs.

To tolerate SEUs and/or even DNUs, researchers have proposed a series of latches, flip-flops, and memory cells. The designs in [4]–[7] consider hardening for flip-flops, the designs in [8]–[16] consider hardening for latches, while the other designs in [17]–[26] and the designs proposed in this paper consider hardening for memory cells. The traditional memory cell is called 6T, which consists of six transistors, i.e., two PMOS and two NMOS transistors for retaining values, and two extra NMOS transistors for access operations. Since the 6T cell cannot tolerate SEUs, many radiation hardened memory cells have been proposed to improve robustness. Typical SEU and/or even DNU hardened cells include NASA13T [17], Lin12T [18], RHD12T [19], RH12T [20], QUCCE10T [21], and QUCCE12T [21]. However, these memory cells still have the following problems.

(1) Most of the existing memory cells suffer from a large silicon area and power dissipation, such as NASA13T [17], Lin12T [18], and RH12T [20]. Moreover, some cells suffer from a large read and write access time, such as NASA13T [17] and QUCCE10T [21].

(2) Most of the existing memory cells have not been effectively hardened, since one or more nodes cannot tolerate SEUs, such as NASA13T [17]. Moreover, some memory cells cannot tolerate DNUs, such as Lin12T [18], RHD12T [19], RH12T [20], QUCCE10T [21], and QUCCE12T [21].

Based on a *radiation hardening by design* (*RHBD*) approach, this paper first presents a novel and highly reliable Quadruple Cross-Coupled Memory cell, namely QCCM10T. The storage module of the memory cell consists of four interlocked input-split inverters. Since the QCCM10T cell uses a few transistors, it has lower cost in terms of area and power consumption. Due to a special feedback mechanism among the internal nodes of the QCCM10T cell, it effectively tolerates SEUs. To reduce read and write access time, the QCCM12T cell is further proposed. This cell has the same soft error tolerance ability when compared to the QCCM10T cell. Moreover, using two extra access transistors, the QCCM12T cell has smaller overhead in terms of read-and-write access time. Simulation results demonstrate the reliability and low overhead of the proposed memory cells.

The rest of this paper is organized as follows. Section II describes the typical SEU and/or DNU hardened cells. Section III describes the schematics and working principles of the proposed memory cell designs. Section IV presents experimental results and comparison results. Section V concludes the paper.

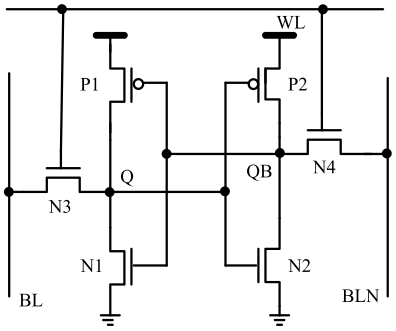

FIGURE 1. Schematic of the traditional 6T cell.

II. PREVIOUS HARDENED MEMORY CELLS

The schematic of the traditional 6T cell is shown in FIGURE 1. The storage module of the 6T cell consists of a couple of cross-coupled inverters. The 6T cell is widely used because of its simple construction and small area. However, the 6T cell cannot tolerate an SEU. Therefore, many radiation hardened cells have been proposed for reliability improvement. FIGURE 2 shows the schematics of typical hardened memory cells, including the NASA13T [17], Lin12T [18], RHD12T [19], RH12T [20], QUCCE10T [21], and QUCCE12T [21].

The schematic of the NASA13T cell [17] is shown in FIGURE 2-(a). It can be seen that the NASA13T cell consists of three parts. The upper left part acts as a value storage module with write access transistors N1 and N2. The lower left part is redundant for value protection. The right part is a special read module for reading values. Compared with 6T, NASA13T provides an improved level of protection against SEUs. However, the NASA13T cell is not effectively SEU-hardened since it cannot tolerate SEUs caused by large energy particles.

The schematic of the Lin12T cell [18] is shown in FIGURE 2-(b). The source and drain terminals of access transistors N5 and N6 connect bit lines (BL and BLN) and storage nodes (Q and QN). Moreover, gate terminals (S0 and S1) of cross-coupled transistors P1 and P4 are also storage nodes, which increase the redundancy of nodes for SEU tolerance. The Lin12T cell is completely SEU-hardened, but only one pair of nodes (i.e., <S0, S1>) is DNU-hardened.

The schematic of the RHD12T cell [19] is shown in FIGURE 2-(c). It can be seen that the RHD12T cell is composed of 12 transistors. NMOS transistors N1 and N2 are access transistors that are controlled by word line WL, and output nodes Q and QN are connected to bit lines BL and BLN through transistors N1 and N2, respectively. The storage module of the cell consists of 10 transistors in which P1 to P6 are PMOS transistors and N3 to N6 are NMOS transistors. Due to the special construction of feedback loops, the RHD12T cell is completely SEU-hardened, but only one pair of nodes (i.e., <S0, S1>) is DNU-hardened.

The schematic of the RH12T cell [20] is shown in FIGURE 2-(d). S0, S1, Q, and QN are storage nodes used for keeping values. Consider the status shown in FIGURE 2-(d)

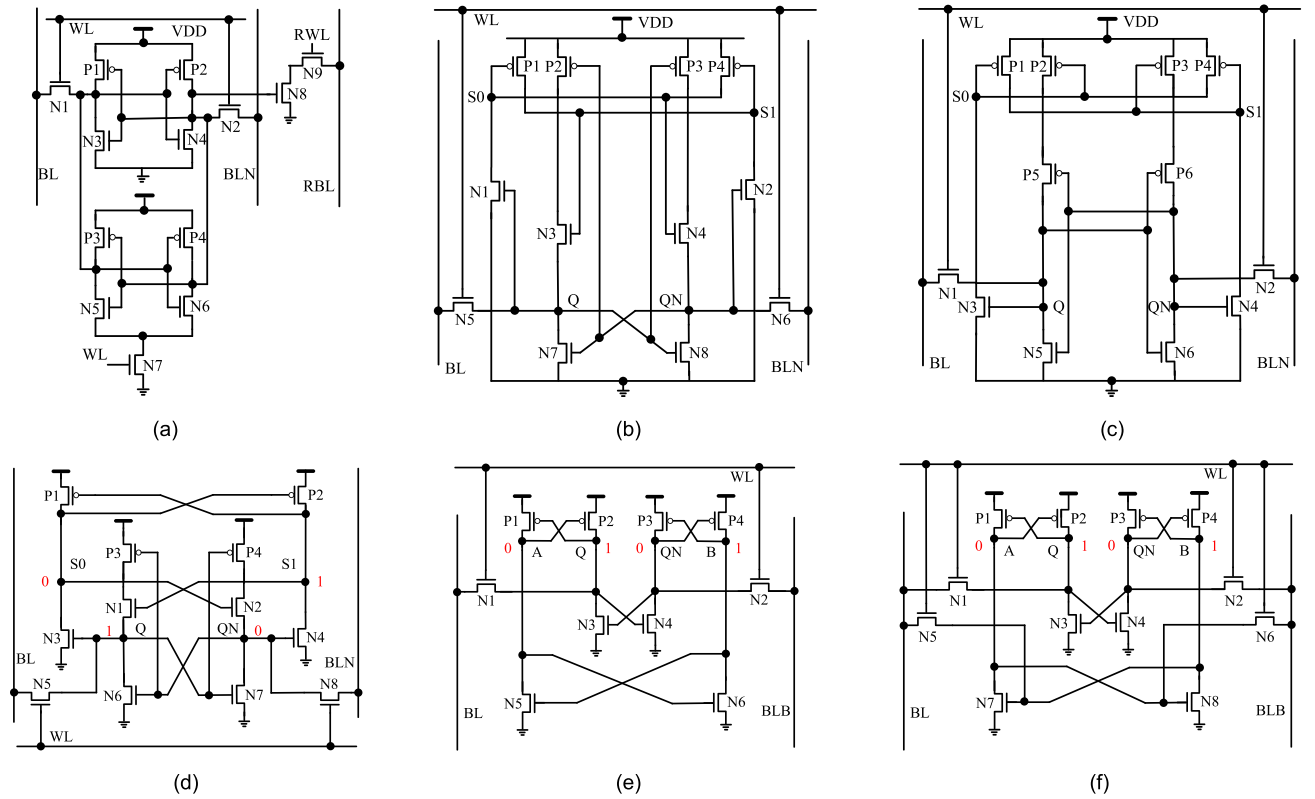

FIGURE 2. Schematics of typical hardened memory cells. (a) NASA13T [17]. (b) Lin12T [18]. (c) RHD12T [19]. (d) RH12T [20]. (e) QUCCE10T [21]. (f) QUCCE12T [21].

as an example (i.e., Q = S1 = 1 and QN = S0 = 0), nodes S0, S1, Q, and QN constitute a feedback loop allowing the cell to keep the stored value effectively. Transistors N1 and N2 split output nodes of two traditional cross-coupled inverters into two nodes (i.e., <Q, QN>), respectively. Moreover, nodes S0 and S1 are connected to gate terminals of transistors N1 and N2 to intercept errors. Similarly to Lin12T and RHD12T, the RH12T cell is completely SEU-hardened, but only one pair of nodes (i.e., <S0, S1>) is DNU-hardened.

The schematic of the QUCCE10T cell [21] is shown in FIGURE 2-(e). The QUCCE10T cell has four storage nodes A, Q, QN, and B. The cell mainly consists of four cross-coupled input-split inverters, constructing a large error-interceptive feedback loop to robustly retain the stored values. As shown in the FIGURE 2-(e), when Q = 1, nodes A, Q, QN and B constitute a robust feedback loop (A → Q → QN → B → A). The QUCCE10T cell is SEU-hardened.

The schematic of the QUCCE12T cell [21] is shown in FIGURE 2-(f). It can be seen that the QUCCE12T cell uses two extra access transistors with respect to the QUCCE10T cell to improve performance. The QUCCE12T cell has a reduced read-and-write access time with the same soft-error tolerance ability when compared with the QUCCE10T cell.

III. PROPOSED MEMORY CELL DESIGNS

A. SCHEMATIC AND NORMAL OPERATIONS

FIGURE 3 shows the schematic of the proposed *Quadruple Cross-Coupled Memory* (*QCCM10T*) cell. From FIGURE 3,

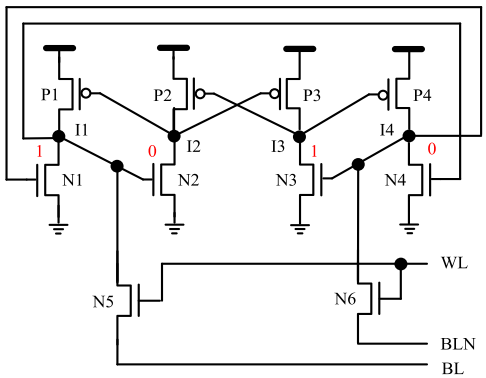

FIGURE 3. Schematic of the proposed QCCM10T cell.

it can be seen that the QCCM10T cell is composed of 10 transistors in which P1 to P4 are PMOS transistors and N1 to N6 are NMOS transistors. Transistors N5 and N6 are used for access operations and their gate terminals are connected to word-line WL. BL and BLN are bit-lines. I1, I2, I3, and I4 are storage nodes for keeping values. FIGURE 4 shows the layout of the proposed QCCM10T cell. When WL is high (WL = 1), the access transistors are ON, allowing read/write operations to be executed. When WL is low (WL = 0), the cell keeps the stored values.

The normal operations of the proposed QCCM10T cell are described as follows. Let us first consider the case of

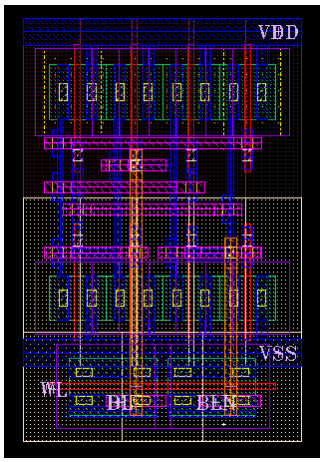

FIGURE 4. Layout of the proposed QCCM10T cell.

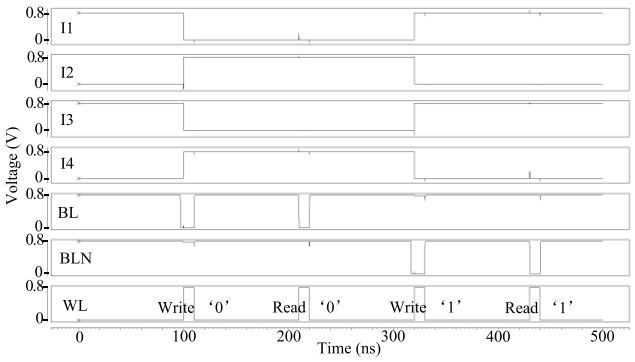

FIGURE 5. Simulation results for normal operations of the proposed QCCM10T cell.

writing 1. Before the normal write operation, owing to the writing circuitry, BL = 1 and BLN = 0. When WL = 1, the operation of writing 1 is executed. Transistors P1, N2, P3, and N4 are ON. Meanwhile, transistors N1, P2, N3, and P4 are OFF, so that the stored value is rightly changed to 1, and the operation of writing 1 is completed. Next, let us consider the case of reading 1. Before the normal read operation, owing to a pre-charge circuitry, the voltages of bit-lines BL and BLN will be set to 1. During the read operation, WL = 1, and access transistors N5 and N6 become ON immediately. Nodes I1, I2, I3, and I4 are keeping the stored values, and the voltage of BL does not change. However, the voltage of BLN decreases due to the discharge operation through N4. BL and BLN are directly connected to a differential sense amplifier, and once the voltage difference between BL and BLN becomes a constant value, the read operation is completed and 1 is read out. Note that, similar scenarios can be observed when writing/reading 0. The simulation results of normal operations of the proposed QCCM10T cell are shown in FIGURE 5. It can be seen that ''write 0, read 0, write 1, and read 1'' operations are correctly executed.

Next, the fault tolerance principle of the proposed QCCM10T cell is described. For the purpose of illustration, we consider the case of a 1 being stored in the cell (i.e., I1 = I3 = 1 and I2 = I4 = 0). In the next section, we discuss the SEU-tolerance principle and the DNU-tolerance principle, respectively.

B. SEU-TOLERANCE PRINCIPLE

The cell state shown in FIGURE 3 is considered for SEU-tolerance analysis. Let us first consider the case where I1 is affected by an SEU. In this case, I1 is temporarily changed to 0 from 1, and hence N2 and N4 are temporarily changed from ON to OFF. Since I3 is not affected (i.e., I3 = 1), P2 and P4 are still OFF. Thus, I2 and I4 still have the same original correct value 0. Thus, N1 is still OFF and P1 is still ON, so that I1 can self-recover from the SEU. Note that the similar SEU self-recovery principle can be obtained when I2 is affected by an SEU.

Let us now describe the case where I3 is affected by an SEU. In this case, I3 is temporarily changed to 0 from 1, and hence P2 and P4 are temporarily changed from OFF to ON. I2 has the value 1 (weak 1) since P2 is temporarily changed from OFF to ON. Since I1 is not affected (i.e., I1 = 1), N2 is still ON and I2 has the value 0 (strong 0). However, the strong 0 of I2 can neutralize the weak 1 and hence I2 is still correct (I2 = 0). Similarly, I4 has the value 1 (weak 1) since P4 is temporarily changed from OFF to ON. Since I1 is not affected (i.e., I1 = 1), N4 is still ON and I4 has the value 0 (strong 0). However, the strong 0 of I4 can neutralize the weak 1 and hence I4 is still correct (I4 = 0). Thus, P3 is still ON and N3 is still OFF, and I3 can self-recover from the SEU.

Let us now describe the case where I4 is affected by an SEU. In this case, I4 is temporarily changed to 1 from 0, and hence N1 and N3 are temporarily changed from OFF to ON. I1 has the value 0 (weak 0) since N1 is temporarily changed from OFF to ON. Since I2 is not directly affected (i.e., I2 = 0), P1 is still ON and I1 has the value 1 (strong 1). However, the strong 1 of I1 can neutralize the weak 0 and hence I1 is still correct (I1 = 1). Thus, N4 is still ON. Similarly, I3 has the value 0 (weak 0) since N3 is temporarily changed from OFF to ON. Since I2 is not directly affected (i.e., I2 = 0), P3 is still ON and I3 has the value 1 (strong 1). However, the strong 1 of I3 can neutralize the weak 0 and hence I3 is still correct (I3 = 1). Since P4 is still OFF, I4 can self-recover from the SEU (N4 is still ON as mentioned above). However, when the striking-particle energy is sufficiently large, I4 will be upset since I1 and I3 can be changed to 0 and P2 and P4 can be ON, so that the stored value of the cell can be flipped. To summarize, the proposed QCCM10T cell exhibits effective SEU self-recovery ability, especially for I1, I2, and I3 when 1 is stored in the cell. Note that the OCCM10T cell exhibits effective SEU self-recovery ability, especially for I2, I3, and I4 when 0 is stored in the cell.

C. DNU-TOLERANCE PRINCIPLE

The cell state shown in FIGURE 3 is considered for DNU-tolerance analysis. Obviously, the proposed QCCM10T cell has six node pairs, i.e., <I1, I2>, <I1, I3>, <I1, I4>,

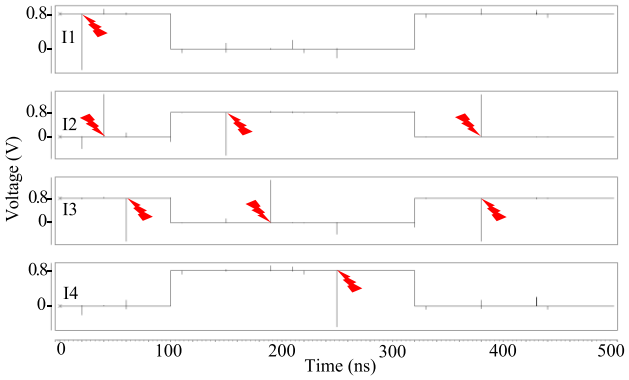

FIGURE 6. Simulation results for SEU and DNU self-recovery of the proposed QCCM10T cell.

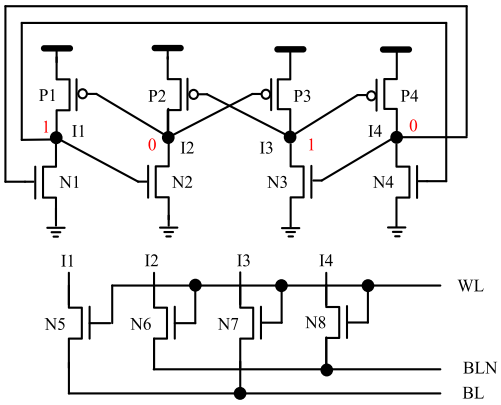

FIGURE 7. Schematic of the proposed QCCM12T cell.

<I2, I3>, <I2, I4>, and <I3, I4>. Let us first describe the case where <I1, I2> is affected by a DNU. In this case, I1 is changed to 0 from 1 and I2 is changed to 1 from 0, and hence P1, P3, N2, and N4 are changed from ON to OFF. I3 and I4 cannot be determined since P3 and N4 are OFF. As time passes, all nodes and transistors cannot self-recover to their original states. In other words, <I1, I2> of the proposed QCCM10T cell cannot self-recover from the DNU. Note that, the similar scenario can be obtained when <I3, I4> is affected by a DNU. Let us now consider the case where <I1, I3> is affected by a DNU. The nodes in the pair are not adjacent considering the layout shown in FIGURE 2, and hence the proposed cell can avoid the occurrence of this DNU. Note that, <I1, I4> and <I2, I4> have the same behavior as <I1, I3>.

Let us now describe the case where <I2, I3> is affected by a DNU. In this case, I2 is temporarily changed to 1 from 0 and I3 is temporarily changed to 0 from 1. Hence, P1 and P3 are temporarily changed from ON to OFF, and P2 and P4 are temporarily changed from OFF to ON. Clearly, N1, N2, N3, and N4 are not directly affected, having their original ON/OFF states. Since I1 = 1, N4 is ON and I4 has the value 0 (strong 0). Meanwhile, since P4 is temporarily changed from OFF to ON, I4 has the value 1 (weak 1). However, the strong 0 of I4 can neutralize the weak 1 and hence I4 is still correct (I4 = 0). Since I1 = 1, N2 is ON and I2 has the value 0 (strong 0). Since P2 is temporarily changed from OFF to ON, I2 has the value 1 (weak 1). However, the strong 0 of I2 can neutralize the weak 1 and hence I2 is still correct (I2 = 0). Obviously, P3 is ON and N3 is OFF, and hence I3 can self-recover from the DNU. In other words, node pair <I2, I3> of the cell can self-recover from the DNU. To summarize, the proposed QCCM10T cell exhibits effective DNU tolerance ability, especially for <I1, I3>, <I1, I4>, <I2, I4>, and <I2, I3>.

FIGURE 6 shows the simulation results for SEU and DNU self-recovery of the proposed QCCM10T cell. As shown in FIGURE 6, when I1 = 1, SEUs were respectively injected on nodes I1, I2, and I3 at 20 ns, 40 ns, and 60 ns. When I1 = 0, SEUs were respectively injected on nodes I2, I3, and I4 at 150 ns, 190 ns, and 250 ns. It can be seen that the proposed QCCM10T cell can self-recover from these injected SEUs. Moreover, a DNU was injected on <I2, I3> at 380 ns as shown in FIGURE 4. It can be seen that the proposed QCCM10T cell can self-recover from the DNU on <I2, I3>. The injection of DNUs on <I1, I3>, <I1, I4>, and <I2, I4> are omitted since DNUs are hardly to happen on these pairs considering the layout of the cell.

In the above simulations, a flexible double-exponential current source model was used to perform all fault injections. The time constant of the rise and fall of the current pulse was set to 0.1 and 3 ps, respectively [26]. The proposed cells are implemented using an advanced 22 nm CMOS library from GlobalFoundries under the room temperature and 0.8V supply voltage. All simulations were performed using Synopsys HSPICE tool.

In order to reduce the read and write access time, the QCCM12T cell is proposed and the schematic of the cell is shown in FIGURE 7. It can be seen that the storage module of QCCM12T is the same as that of QCCM10T. Therefore, the QCCM12T cell has the same soft-error tolerance ability when compared to the QCCM10T cell, i.e., they have the same SEU and DNU tolerance principles. However, the QCCM12T cell uses two extra access transistors compared to the QCCM10T cell to effectively improve the access-operation performance. FIGURE 8 shows the layout of the proposed QCCM12T cell.

IV. COMPARISON AND EVALUATION RESULTS

In the following, the comparison and evaluation results for the proposed QCCM10T and QCCM12T cells and the state-of-the-art cells described in Section I (i.e., NASA13T [17], Lin12T [18], RHD12T [19], RH12T [20], QUCCE10T [21], and QUCCE12T [21]) are described. The same implementation conditions that described in the above section were used to implement all cells. Table 1 shows the reliability and overhead comparison results of the unhardened and hardened memory cells, in terms of SEU tolerance, *number of DNU-hardened node-pairs* (#*DHNP*), silicon area,

TABLE 1. Reliability and overhead comparison results of the unhardened and hardened memory cells.

SRAM	6T	NASA13T	Lin12T	RHD12T	RH12T	QUCCE10T	QUCCE12T	QCCM10T	QCCM12T
Ref.	-	[17]	[18]	[19]	[20]	[21]	[21]	Proposed	Proposed
SEU Hardness	×	×	√	√	√	√	√	√	√
#DHNP	0	0	1	1	1	0	0	4	4
$10^{-3}\times$Area (nm^2)	4.35	9.70	9.28	8.27	9.28	6.16	8.71	7.79	8.71
Power (nW)	5.24	18.92	9.74	10.38	9.74	10.08	10.43	8.50	10.43
RAT (ps)	25.88	128.67	37.68	25.72	37.72	36.36	13.02	18.20	12.99
WAT (ps)	3.65	16.39	3.78	5.06	3.85	6.29	4.31	23.21	3.65

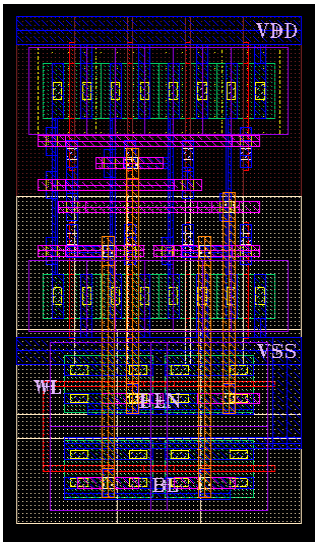

FIGURE 8. Layout of the proposed QCCM12T cell.

power dissipation, *read access time* (*RAT*), and *write access time* (*WAT*).

Let us first describe the reliability comparison results. It can be seen from Table 1 that all cells except the 6T and the NASA13T are SEU hardened, providing high reliability. Regarding #DHNP, only the proposed QCCM10T and QCCM12T cells can tolerate DNUs for 4 node-pairs, while the other cells can only tolerate DNUs for 0 or 1 node-pair. To summarize, the proposed QCCM10T and QCCM12T cells can provide much better reliability.

Let us now discuss the overhead comparison results. For power and area, we consider that a cell using only a few transistors has a small area and small power consumption, and a cell having a larger area will consume extra power. It can be seen from Table 1 that the 6T cell has the smallest power consumption and area overhead since it uses only 6 transistors. Since NASA13T uses extra transistors and there is more current competition in its feedback loops, it has the largest area and power. Lin12T, RHD12T, RH12T, QUCCE12T, and the proposed QCCM12T use the same amount of transistors and they have similar cell constructions, and hence they have similar area and power consumption. It can be seen from Table 1 that the proposed QCCM10T cell has the smallest power consumption, except when compared with the 6T cell, mainly due to the smaller area and the less current competition in its feedback loops.

For WATs and RATs, we consider that the intrinsic charge/discharge of cell nodes through access transistors can affect WATs and RATs. It can be seen from Table 1 that the 6T cell has the smallest WAT, mainly because the cell has less current competition when the write operation is executed. The proposed QCCM12T also has the smallest WAT due to the use of extra access transistors. However, the NASA13T has the largest WAT, mainly due to more current competition when the write operation is executed. The proposed QCCM10T has the largest RAT mainly due to the slow current flow from the cell when the read operation is executed. However, the proposed QCCM12T has the smallest RAT owing to the use of extra access transistors.

$$\Delta Area = \frac{Area_{\text{compared}}(i) - Area_{\text{proposed}}(i)}{Area_{\text{compared}}(i)} \times 100\% \quad (1)$$

$$PRC_{Area}^{Average} = \sum_{i=1}^{n} \frac{Area_{\text{compared}}(i) - Area_{\text{proposed}}(i)}{Area_{\text{compared}}(i)} \times 100\% \quad (2)$$

The *percentages of reduced costs* (*PRCs*) of the proposed QCCM10T cell compared with the other memory cells are calculated and analyzed. The PRC of the area can be calculated with Eq. (1). Similarly, the PRCs of the power dissipation, RAT, and WAT can be calculated. The average PRC of the area can be calculated with Eq. (2). Similarly, the average PRCs of the power dissipation, RAT, and WAT can also be calculated. Table 2 shows the PRCs for the proposed QCCM10T cell compared with the other memory cells. For the sake of brevity, only the average PRCs are discussed. It can be seen from Table 2 that compared with the six hardened cells, the average PRCs of the silicon area, power dissipation, WAT, and RAT for the proposed QCCM10T cell are 6.95%, 22.14%, 38.12%, and −353.97%, respectively.

TABLE 2. Percentages of reduced costs for the proposed QCCM10T cell compared with the other memory cells.

SRAM	Δ Area (%)	Δ Power (%)	Δ RAT (%)	Δ WAT (%)
NASA13T	19.69	55.07	85.86	-41.61
Lin12T	16.06	12.73	51.70	-514.02
RHD12T	5.80	18.11	29.24	-358.70
RH12T	16.06	12.73	51.75	-502.86
QUCCE10T	-26.46	15.67	49.94	-268.10
QUCCE12T	10.56	18.50	-39.78	-438.52
Average	6.95	22.14	38.12	-353.97

TABLE 3. Percentages of reduced costs for the proposed QCCM12T cell compared with the other memory cells.

SRAM	Δ Area (%)	Δ Power (%)	Δ RAT (%)	Δ WAT (%)
NASA13T	10.21	44.87	89.90	77.73
Lin12T	6.14	-7.08	65.53	3.44
RHD12T	-5.32	-0.48	49.49	27.87
RH12T	6.14	-7.08	65.56	5.19
QUCCE10T	-41.39	-3.47	64.27	41.97
QUCCE12T	0	0	0.23	15.31
Average	-4.04	4.46	55.83	28.59

It means that the proposed QCCM10T cell saves 6.95% silicon area, 22.14% power dissipation, and 38.12% WAT on average. However, the proposed QCCM10T cell has an extra 353.97% WAT on average, which motivates us to use extra access transistors to reduce the WAT.

The PRCs of the QCCM12T cell compared with the other memory cells are calculated and analyzed. Table 3 shows the PRCs for the proposed QCCM12T cell compared with the other memory cells. For the sake of brevity, only the average PRCs are discussed. It can be seen from Table 3 that compared with the six hardened cells, the average PRCs of the silicon area, power dissipation, WAT, and RAT for the proposed QCCM12T are −4.04%, 4.46%, 55.83%, and 28.59%, respectively. It means that the proposed QCCM12T cell saves 4.46% power dissipation, 55.83% WAT, and 28.59% RAT on average. On the other side, the proposed QCCM12T cell only increases silicon area by 4.04% on average.

To summarize, the proposed QCCM10T and QCCM12T cells have been effectively hardened. Compared with the existing state-of-the-art hardened cells, the proposed QCCM10T cell has lower overhead especially in terms of silicon area and power dissipation, and the proposed QCCM12T cell has lower overhead especially in terms of RAT and WAT.

V. CONCLUSION

CMOS technology scaling makes modern memory cells more and more sensitive to soft errors that include SEUs and DNUs. In this paper, first, a novel and highly reliable QCCM10T cell has been proposed. The cell is effectively hardened against SEUs and DNUs and has a low cost especially in terms of area and power consumption. Next, to reduce the read and write access time, the QCCM12T cell has further been proposed. The cell has the same soft error tolerance ability compared to the QCCM10T cell and can achieve low overhead in terms of the read and write access time. The proposed cells can be effectively applied for safety-critical applications, such as aerospace, nuclear plants, and banking, where high reliability is required.

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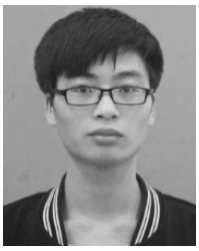

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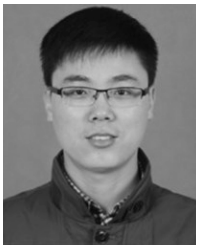

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