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Asymmetric Pulse Frequency Modulation With Constant On-Time for Series Resonant Converter in High-Voltage High-Power Applications

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ABSTRACT The series resonant converter (SRC), controlled by the traditional pulse frequency modulation (PFM) with constant on-time, can operate in discontinuous conduction mode (DCM) and is applicable for high-voltage high-power applications with the requirement of a wide output voltage range. However, in the traditional PFM with constant on-time, the resonant capacitor voltage will be higher than the input voltage during the zero current stage, leading to a higher maximum magnetic flux density (MMFD) case. To avoid this, a novel asymmetric pulse frequency modulation (APFM) with constant on-time is proposed for SRC operating in DCM, where the MMFD of transformer core varies linearly with the operating frequency and output voltage among the whole output voltage range. The high-power transformer can be designed according to highest operating frequency and the transformer turns ratio can be designed to be small. Furthermore, the proposed APFM leads to smaller peak current for all switches and fully zero-current-switching can be achieved. The output power and voltage can be still regulated, meeting the high-voltage high-power applications. For the proposed APFM, there are four different driver combinations with exact the same effects and advantages. The theoretical analysis has been validated by the established simulation model and experimental platform.

INDEX TERMS Series resonant converter (SRC), asymmetric pulse frequency modulation (APFM), constant on-time, magnetic flux density (MFD), small peak current.

I. INTRODUCTION

The high-voltage high-power converter is the key unit of high-voltage equipment, for example, the electrostatic precipitator (ESP) and X-ray power generator in environmental protection and medical industry fields [1]–[4]. Moreover, to meet the practical demand in such applications, the high-voltage high-power converter should be able to operate in wide output power/voltage range, like dozens of kilowatts/kilovolts to hundreds of kilowatts/kilovolts [1].

High-voltage large-current semiconductors are required for such applications, where IGBTs are preferred rather than MOSFETs thanks to the much higher voltage and current ratings [5]–[7]. To eliminate the tail current effect and reduce the switching loss of IGBTs, the soft-switching technique of zero-current-switching (ZCS) should be employed [6], [7]. The resonant converters can generally realize ZCS easier and have been paid a lot attention [3], [8]–[20]. For example, the parallel resonant converter is one candidate for such high-voltage high-power applications due to the fact that the capacitive output filter [8], without a bulky and difficult-manufactured high-voltage filter inductor [9], can be utilized. However, it has a relatively large circulating current with relatively low conversion efficiency at light loads. The series-parallel resonant converter (SPRC), featuring with high voltage gain, can also be adopted since both the leakage inductance and winding capacitance of high-power transformer can function as the resonant components [10]–[12]. The SPRC is difficult to design and optimize due to the difficult assessment of the transformer parasitic parameters, especially the winding capacitance. The full-bridge series resonant converter (SRC) is another available resonant

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approach to achieve ZCS for IGBTs, where the capacitive output filter can be utilized as well and makes it suitable for high-voltage applications. Moreover, with inherent short-circuit protection, the SRC can function as a current source for resistive load [13]–[15]. For applications such as high-voltage ESP [1], [2], where short-circuit like flashover might frequently happen, it is a great advantage.

To realize ZCS for the four IGBTs in SRC, the discontinuous-conduction-mode (DCM) should be adopted. Based on different modulations, the SRC operating in DCM (DCM-SRC) can be assorted into four main kinds. The first kind is well known as the half-cycle DCM-SRC (HC-DCM-SRC) [16], [17], which can be found in solid state transformer for smart grids and traction systems with significantly reduced system size and weight [18]. Actually, the HC-DCM-SRC can be seen as a dc transformer and has no power and voltage control ability [17]. To meet the wide output voltage range requirement, the pulse frequency modulation (PFM) can be employed. For example, the second kind of DCM-SRC is controlled by PFM with a constant 50% duty cycle to realize the output voltage regulation [3], [15], leading to a wide switching frequency range. Although the ZCS can be achieved for all IGBTs in this kind of DCM-SRC, the high-power transformer needs to be designed according to the lowest switching frequency since the magnetic flux density (MFD) value of transformer core is highest at lowest switching frequency. As a result, the transformer size is large and the total cost is high. To solve the problem of high MFD at low frequency, a novel control called the pulse removal technique is introduced in [19], [20], which can be classified as the third kind of DCM-SRC. But it is more suitable for dc transformer applications just as the first kind of DCM-SRC since only the output power can be regulated but with constant input and output voltages. The last kind of DCM-SRC is modulated by the traditional PFM with constant on-time [21], [22], where fully ZCS can be achieved for all IGBTs and the output power and voltage can be regulated easily. However, the maximum MFD (MMFD) of transformer core will increase unexpectedly after the output voltage rising to a certain value, where the transformer step-up turns ratio is smaller than two times of output voltage/input voltage (i.e., $n < 2V_o/V_{in}$). Few literatures have discussed the MFD of the last kind of DCM-SRC within a wide output voltage range. Additionally, the peak current of IGBTs is high under the traditional PFM with constant on-time.

An asymmetric pulse frequency modulation (APFM) with constant on-time for DCM-SRC is proposed in this paper to solve the above problems, where all IGBTs can achieve fully ZCS among the whole operation range. Among the whole output voltage range, the MMFD of transformer core increases linearly with the increase of operating frequency and output voltage, avoiding the unexpected MMFD increase case in traditional PFM with constant on-time. And the high-power transformer can be designed according to highest operating frequency instead of lowest operating frequency. Furthermore, there is no much restriction on the transformer turns ratio except for that it must be larger than the value of output voltage/input voltage (i. e., $n > V_o/V_{in}$) since the voltage gain of SRC is inherently smaller than one. Hence, the transformer turns ratio can be set as much smaller. The proposed APFM can realize the regulation of the output power and voltage, which can meet the requirement of applications such as ESP and X-ray power generator. Meanwhile, the peak current of IGBTs is smaller, where IGBTs with lower current rating can be utilized.

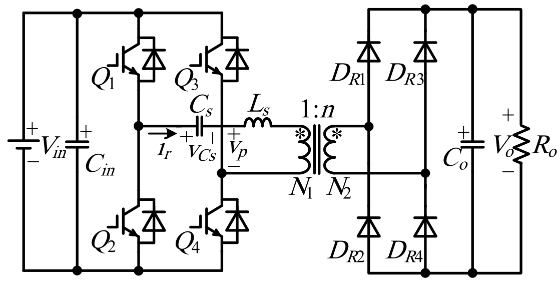

FIGURE 1. Series resonant converter (SRC).

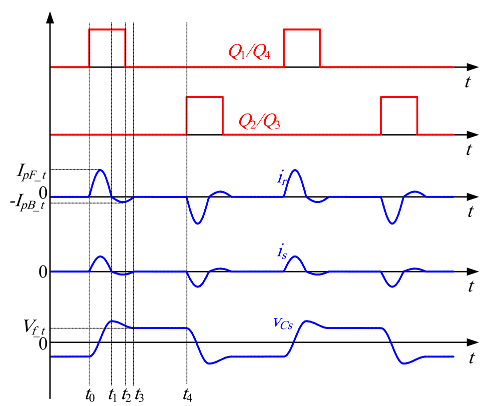

FIGURE 2. Key waveforms of traditional PFM with constant on-time.

II. PROBLEM OF TRADITIONAL PFM FOR DCM-SRC

A SRC is illustrated in Fig. 1, including four switches $Q_1 \sim Q_4$ and four rectifier diodes $D_{R1} \sim D_{R4}$, where the resonant inductor L_s and resonant capacitor C_s form the resonant tank, and N_1 and N_2 are turns of primary and secondary windings of the high-power high-frequency transformer, respectively, and $n = N_2/N_1$. The key waveforms of traditional PFM with constant on-time are drawn in Fig. 2, where the switching frequency is variable to regulate the output voltage and power. Switches Q_1 and Q_4 have the same gate driver with constant on-time, so do the switches Q_2 and Q_3 with half a switching period delay from Q_1 and Q_4. And the constant on-time is the same for all switches. As shown in Fig. 2, there are three stages for traditional PFM with constant on-time during $[t_0, t_4]$, namely, the forward resonant stage $[t_0, t_1]$, the backward resonant stage $[t_1, t_3]$, and the zero current stage $[t_3, t_4]$. Some already-known results will be briefly presented and before that, some assumptions are made as follows:

1) all the switches, diodes, transformer and capacitors are ideal;
2) the output voltage V_o is considered to be constant at steady state;
3) the parasitic capacitance of high-power high-frequency transformer is not that large [20] and can be further reduced through optimized multi-section multi-layer structure of the secondary winding [23], [24], hence, it is neglected.

Referring to [15] and [22], the peak current of forward resonant stage and backward resonant stage of the traditional PFM with constant on-time can be expressed as

$$\begin{cases} I_{pF\_t} = (V_{in} + V_o/n)/Z_r \\ I_{pB\_t} = (V_{in} - V_o/n)/Z_r \end{cases} \tag{1}$$

From Fig. 2, V_{f_t} is the voltage across C_s during the zero current stage, which satisfies with (2) according to [15] and [22].

$$V_{f\_t} = v_{Cs}(t_3) = -v_{Cs}(t_0) = 2V_o/n \tag{2}$$

It is easy to find that V_{f_t} will increase with the increase of V_o, and it will be higher than V_{in} when $n < 2V_o/V_{in}$. In that case, the anti-paralleled diodes of Q_1 and Q_4 are naturally turned on and a current path can be formed, leading to an unexpected MMFD increase during the zero current stage.

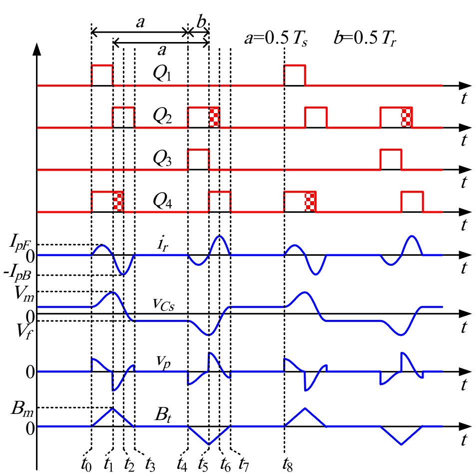

FIGURE 3. Key waveforms of proposed APFM with constant on-time.

III. ANALYSIS OF PROPOSED APFM FOR DCM-SRC

To avoid the unexpected MMFD increase case, namely, to avoid the resonant capacitor voltage during the zero current stage is higher than V_{in}, an APFM with constant on-time is proposed. The key waveforms of proposed APFM are drawn in Fig. 3, where the resonant inductor voltage is included in the transformer primary winding voltage v_p for the transformer leakage inductor is adopted as the resonant inductor without any extra series inductor through proper transformer design. [t_0, t_8] is one operating period T_s, which can be classified into six operation stages.

1) Before t_0: As shown in Fig. 3, all the switches are under off state, there is no current flowing in any switches and diodes, and the voltage across C_s, v_{Cs}, keeps unchanged. Besides, both v_p and the transformer MFD B_t keeps unchanged with the value of zero.
2) Stage 1 [t_0, t_1] (see Fig. 4(a)): At t_0, Q_1 and Q_4 are turned on simultaneously, L_s starts to forward resonate with C_s, and the resonant inductor current i_r rises from zero, where ZCS turn-on is achieved for both Q_1 and Q_4. Obviously, this stage lasts half of the resonant period T_r of L_s and C_s, i. e., $t_1 - t_0 = 0.5T_r$. During this stage, i_r can be expressed as

$$i_r(t) = I_{pF} \sin \omega_r (t - t_0), \quad I_{pF} = \frac{V_{in} - V_o/n - v_{Cs}(t_0)}{Z_r} \tag{3}$$

where I_{pF} is the peak current of Stage 1, and

$$\omega_r = 1/\sqrt{L_s C_s}, Z_r = \sqrt{L_s/C_s} \tag{4}$$

Since i_r is positive during this half resonant period, C_s is charged and the following can be obtained

$$v_{Cs}(t_1) - v_{Cs}(t_0) = \frac{2I_{pF}}{\omega_r C_s} = 2[V_{in} - V_o/n - v_{Cs}(t_0)] \tag{5}$$

Referring to Fig. 4(a), the voltage across the secondary winding is clamped by V_o during Stage 1 (hence, v_p varies with the resonant inductor voltage, as shown in Fig. 3), and the transformer core is magnetized and B_t increases linearly as shown in Fig. 3. According to the Faraday law of electromagnetic induction, one can obtain

$$\frac{V_o}{n} = N_1 \frac{d\phi}{dt} = \frac{N_1 B_t(t_1) A_e}{\pi \sqrt{L_s C_s}} \tag{6}$$

where A_e is the effective cross-sectional area of transformer core.

3) Stage 2 [t_1, t_3] (see Fig. 4(b)): At t_1, Q_1 is turned off while Q_2 is turned on. Hence, Q_2, the anti-paralleled diode of Q_4, and the transformer primary winding provide a backward resonant path for L_s and C_s. Since i_r has decayed to zero at t_1, ZCS is realized for both Q_1 and Q_2. This stage is the other half resonant period, i. e., $t_3 - t_1 = 0.5T_r$. Within time interval [t_1, t_3], i_r starts to reverse from t_1, and it can be presented as

$$i_r(t) = -I_{pB} \sin \omega_r (t - t_1), \quad I_{pB} = \frac{v_{Cs}(t_1) - V_o/n}{Z_r} \tag{7}$$

where I_{pB} is the peak current of Stage 2.

Since i_r is negative during this stage, C_s is discharged and the following can be obtained

$$v_{Cs}(t_3) - v_{Cs}(t_1) = -\frac{2I_{pB}}{\omega_r C_s} = -2[v_{Cs}(t_1) - V_o/n] \tag{8}$$

Taking the symmetrical operation principle of the converter into consideration, v_{Cs} should satisfy with

$$v_{Cs}(t_3) = -v_{Cs}(t_0) \tag{9}$$

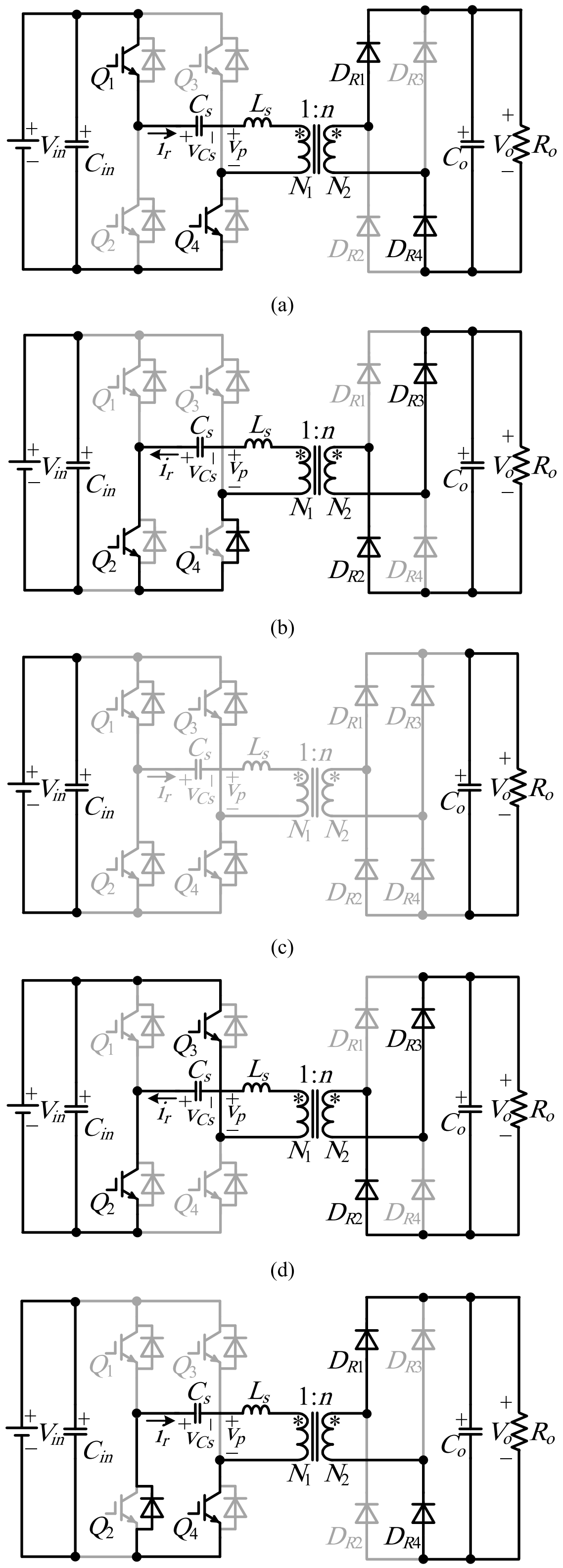

FIGURE 4. **Current paths of one operation period. (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_3]. (c) Stages 3 and 6 [t_3, t_4] & [t_7, t_8]. (d) Stage 4 [t_4, t_5]. (e) Stage 5 [t_5, t_7].**

Combining (5), (8), and (9), and one can get

$$\begin{cases} v_{Cs}(t_3) = -v_{Cs}(t_0) = V_f = 2V_o/n - V_{in} \\ v_{Cs}(t_1) = V_m = V_{in} \end{cases} \tag{10}$$

where V_f is the voltage across C_s at the end of the resonance and V_m is the maximum voltage across C_s. V_f will increase with the increase of V_o, and it is negative when V_o is low then it can turn to be positive with the increase of V_o; while V_m is a constant value of V_{in}.

For C_s is discharged during [t_1, t_3], $v_{Cs}(t_1) > v_{Cs}(t_3)$ and it can be concluded that V_f is smaller than V_{in} regardless of the value of n. According to the conclusion in Section II, the unexpected higher MMFD of the traditional PFM with constant on-time can be completely avoided when the proposed APFM is adopted. In other words, even V_o increases to meet that $n < 2V_o/V_{in}$, the MMFD will not increase unexpectedly with the proposed APFM. Furthermore, (11) can be obtained since $V_f < V_{in}$ and it should be the design rule for n to guarantee the normal operation of the proposed APFM for DCM-SRC.

$$n > V_o/V_{in} \tag{11}$$

Substituting (10) into (3) and (7), and I_{pF} and I_{pB} can be expressed as

$$\begin{cases} I_{pF} = V_o/(nZ_r) \\ I_{pB} = (V_{in} - V_o/n)/Z_r \end{cases} \tag{12}$$

As can be seen, I_{pF} will increase with the increase V_o while I_{pB} will decrease. By comparing (1) and (12), one can find that I_{pF} of the proposed APFM is much smaller than that in traditional PFM with constant on-time. In fact, since $V_{in} > V_o/n$ according to (11), I_{pF} can be at least 50% lower than I_{pF_t}.

Referring to Fig. 4(b), the voltage across the secondary winding is clamped by $-V_o$ during Stage 2 (v_p varies with the resonant inductor voltage as well), the transformer core is demagnetized and B_t decreases linearly. Since the time intervals of Stages 1 and 2 are exactly the same of $0.5T_r$, B_t will decay to zero at t_3, as shown in Fig. 3. Hence, the MMFD B_m of the proposed APFM can be expressed as

$$B_m = B_t(t_1) = \frac{\pi V_o \sqrt{L_s C_s}}{n N_1 A_e} \tag{13}$$

As shown in Fig. 4(b), the current flows through the anti-paralleled diode of Q_4 the whole stage. Hence, Q_4 can be turned off with ZCS at any moment t_1 and t_3. Without loss of generality, Q_4 can be turned off at t_2.

4) Stage 3 [t_3, t_4] (see Fig. 4(c)): Q_2 is turned off with ZCS at t_3 since the backward resonance is over at that time. During this stage, as V_f is lower than V_{in}, there is absolutely no current flowing in the resonant tank through the paralleled diodes nor the secondary side and v_{Cs} keeps unchanged with the value of V_f.

Hence, Stage 3 can be called the zero current stage. Meanwhile, both v_p and B_t keeps unchanged with the value of zero.

As shown in Fig. 3, Stages 1 to 3 are half of the operation period, i. e., $t_4-t_0=0.5T_s$. Due to the symmetrical operation principle of SRC, Stages 4 to 6 during $[t_4, t_8]$ will be briefly presented in the following.

5) Stage 4 $[t_4, t_5]$ (see Fig. 4(d)): At t_4, Q_2 and Q_3 are turned on with ZCS simultaneously, L_s starts to backward resonate with C_s, and i_r reversely rises from zero, of which the peak current is $-I_{pF}$. Since the voltage across the secondary winding is clamped by $-V_o$, B_t reversely increases to $-B_m$ at t_5. It is the same as Stage 1, and this stage lasts half of the resonant period, i. e., $t_5-t_4=0.5T_r$.

6) Stage 5 $[t_5, t_7]$ (see Fig. 4(e)): $t_7-t_5=0.5T_r$ with Q_3 is ZCS turn-off and Q_4 is ZCS turn-on at t_5. The transformer primary winding, Q_4, and the anti-paralleled diode of Q_2 provide a forward resonant path for L_s and C_s, hence, Q_2 can be turned off with ZCS at t_6. Similar within Stage 2, the peak current of i_r is I_{pB} during this stage. The voltage across the secondary winding is clamped by V_o during this stage, leading to B_t will reversely decrease to zero at t_7.

7) Stage 6 $[t_7, t_8]$ (see Fig. 4(c)): Q_4 is turned off with ZCS at t_7 and there is no current flowing in the primary and/or secondary sides, with that v_{Cs} keeps unchanged with the value of $-V_f$. Hence, Stage 6 is the zero current stage as well. Similar within Stage 3, v_p and B_t are zero during this stage.

In practice, to avoid turning on Q_2 before t_1, some reasonable dead time can be added between Stages 1 and 2 and v_{Cs} will keep unchanged as V_{in} during that dead time. Likewise, the same dead time can be added between Stages 4 and 5, during which v_{Cs} will keep unchanged as $-V_{in}$.

Based on the above analysis, the total power can be calculated within $[t_0, t_4]$. It can be obtained as (14) from the secondary side (assuming the conversion efficiency is 100%).

$$P_{in}=2f_sV_o\left(\int_0^{\pi\sqrt{L_sC_s}}\frac{I_{pF}}{n}\sin\omega_r t dt+\int_0^{\pi\sqrt{L_sC_s}}\frac{I_{pB}}{n}\sin\omega_r t dt\right)=\frac{4f_sV_o\left(I_{pF}+I_{pB}\right)}{n\omega_r}=P_o=\frac{V_o^2}{R_o} \quad (14)$$

where R_o is the load resistance and $f_s(=1/T_s)$ is the operating frequency of Q_1 and Q_3, while the operating frequency of Q_2 and Q_4 is $2f_s$, as shown in Fig. 3. It should be noted that since all the switches can realize ZCS, the higher operating frequency of Q_2 and Q_4 has no impact on the switching loss.

When it comes to the conduction loss, since there are two more resonant stages for Q_2 and Q_4 ($[t_1, t_3]$ and $[t_5, t_7]$), Q_2 and Q_4 have higher conduction loss. Hence, when designing the experimental platform one should pay attention on the higher conduction loss of Q_2 and Q_4.

Substituting (12) into (14), one can get

$$V_o=\frac{4f_sV_{in}R_oC_s}{n} \quad (15)$$

From (15), it can be concluded V_o will increase linearly with the increase of f_s when the load of SRC is a constant resistor.

By summarizing the above analysis, some conclusions can be made when the proposed control adopted:

i) ZCS turn-on and turn-off can be realized for all switches.

ii) The peak current of four main switches is at least 50% smaller and IGBTs with lower current rating can be adopted.

iii) n can be designed with rule of $n > V_o/V_{in}$. Then, regardless of the value of n, there is $|V_f| < V_{in}$ and there is no current flowing in the primary and/or secondary sides during the zero current stages. Hence, v_p and B_t are zero during the zero current stages and the unexpected MMFD increase under traditional PFM with constant on-time will never occur.

iv) Among the whole V_o variation range and even when that $n < 2V_o/V_{in}$, B_m of the proposed control can be calculated with (13), which is proportional to V_o.

v) V_o is proportional to f_s under resistive load. And the high-power transformer can be designed at the highest switching frequency.

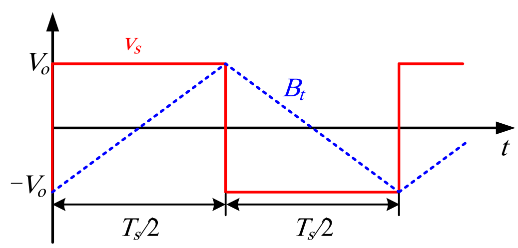

FIGURE 5. Square waveform of secondary winding voltage in many cases.

Generally, the secondary winding voltage of transformer is square wave in most cases, as shown in Fig. 5. According to the Faraday law of electromagnetic induction, one can obtain

$$V_o=N_2\frac{d\phi}{dt}=\frac{N_2B_{m\_G}A_e}{T_s/4} \quad (16)$$

where B_{m_G} is the MMFD in general cases.

Since $N_2=nN_1$, B_{m_G} can be expressed as

$$B_{m\_G}=\frac{V_oT_s}{nN_1A_e} \quad (17)$$

Obviously, B_{m_G} is proportional to T_s and will be high if f_s is low. In such case, to make sure the normal operation of transformer, the A_e should be large to get low B_{m_G} and avoid the transformer saturation problem. As a result, the transformer should be designed at the lowest switching frequency.

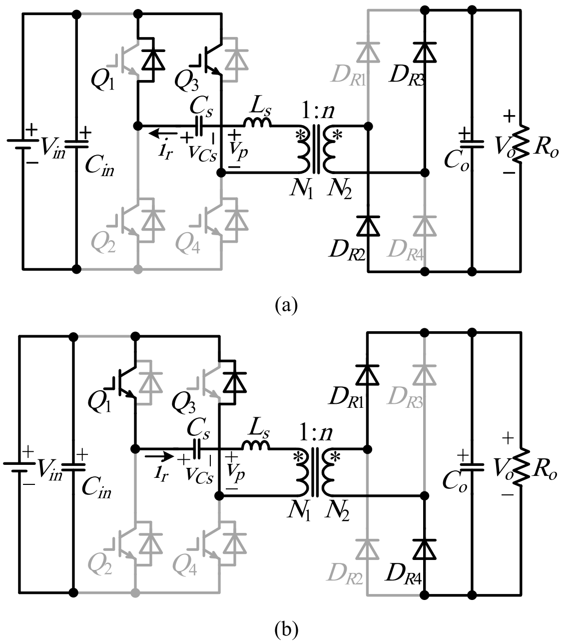

FIGURE 6. **Alternative resonant current paths. (a) For Stage 2 [t_1, t_3]. (b) For Stage 5 [t_5, t_7].**

Referring to (13) and (17), it can be found that B_m of the proposed APFM has no such problem with the same V_o. As a result, the transformer can be designed at the highest switching frequency without that large A_e.

Additionally, Q_2 is turned on at t_1 to provide a backward resonant current path for Stage 2. Actually, one can choose to turn on Q_3 rather than Q_2 to provide the current path for Stage 2, as shown in Fig. 6(a). In such way, the backward resonant current flows through the anti-paralleled diode of Q_1, Q_3, and the transformer primary winding. It should be noted that it has the same v_{Cs}, i_r, and B_t during Stage 2. Hence, there are two alternative current paths (Fig. 4(b) and Fig. 6(a)) for Stage 2. Likewise, one can choose to turn on Q_1 rather than Q_4 at t_5 to provide the forward current path for Stage 5. As shown in Fig. 6(b), the forward resonant current flows through the transformer primary winding, the anti-paralleled diode of Q_3, and Q_1. Hence, there are two alternative current paths (Fig. 4(e) and Fig. 6(b)) for Stage 5 as well. As a result, there are four different APFMs. Except for the first APFM shown in Fig. 3, the left three APFMs are drawn in Fig. 7. As can be seen, all the APFMs have exact the same current, voltage and MFD waveforms, leading to exact the same effects and advantages. Hence, the first APFM with constant on-time is taken for analysis.

IV. SIMULATION VERIFICATION AND COMPARISON

To validate the above theoretical analysis results and compare B_m of the proposed APFM with that of traditional PFM among the same output voltage range, the same simulation parameters are adopted, as presented in Table 1. The transformer core is made of nanocrystalline material

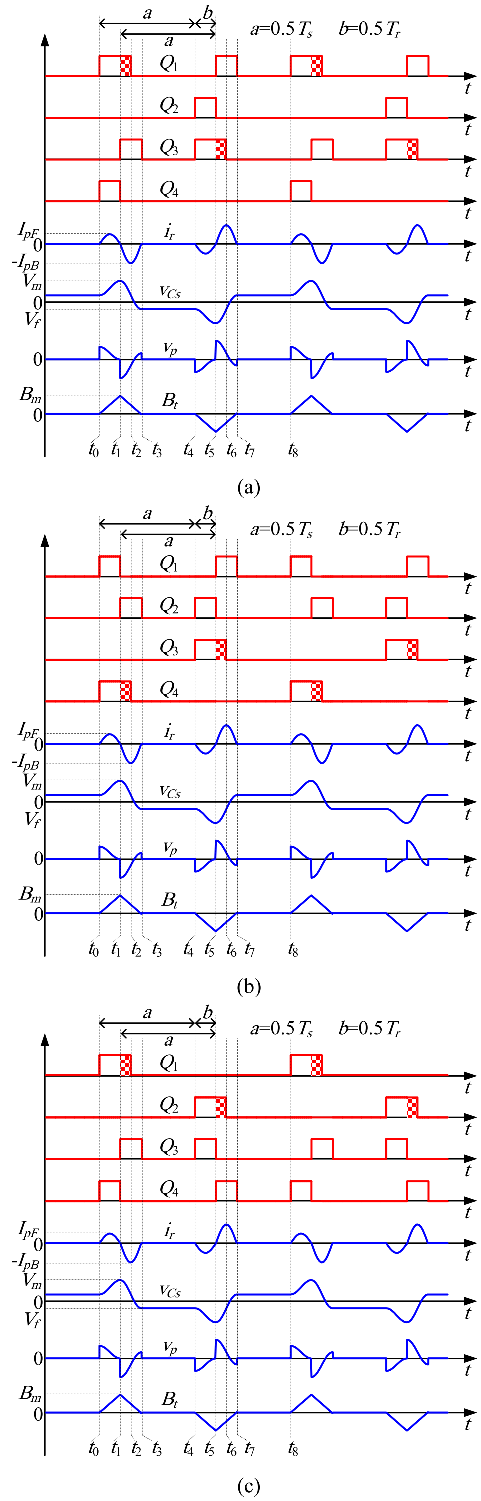

FIGURE 7. **Key waveforms of the other three APFMs. (a) Fig. 6(a) for Stage 2 [t_1, t_3] and Fig. 6(b) for Stage 5 [t_5, t_7]. (b) Fig. 4(b) for Stage 2 [t_1, t_3] and Fig. 6(b) for Stage 5 [t_5, t_7]. (c) Fig. 6(a) for Stage 2 [t_1, t_3] and Fig. 4(e) for Stage 5 [t_5, t_7].**

which is suitable for high-power and high-frequency applications for its high unsaturated relative permeability $\mu_{r,unsat}$ and high saturation MFD B_{sat}. To make the simulation

TABLE 1. Simulation parameters.

Symbol	Quantity	Symbol	Quantity	Symbol	Quantity
V_{in}	540 V	N_2	1920	$\mu_{r,unsat}$	30000
L_s	8 μH	n	160	B_{sat}	1.2 T
C_s	6 μF	R_o	72 kΩ	C_o	125 nF
f_r	23 kHz	A_e	14.4 cm^2		
N_1	12	l	100 cm		

more practical and convincing, the transformer core type is CN-280*150*45*40 provided by Advanced Technology & Materials Company, Ltd (AT&M) [25], where the effective cross-sectional area A_e and flux path length l of the selected transformer core can be acquired as well.

According to (15) in this paper and [15] and [22], f_s of the proposed APFM should be two times of that of the traditional PFM with constant on-time to get the same V_o. Hence, two different f_s of 6 kHz and 10 kHz (respective responding to 3 kHz and 5 kHz under traditional PFM), with respective V_o of 35 kV and 58.3 kV representing cases of $n > 2V_o/V_{in}$ and $n < 2V_o/V_{in}$, will be simulated for validation and comparison.

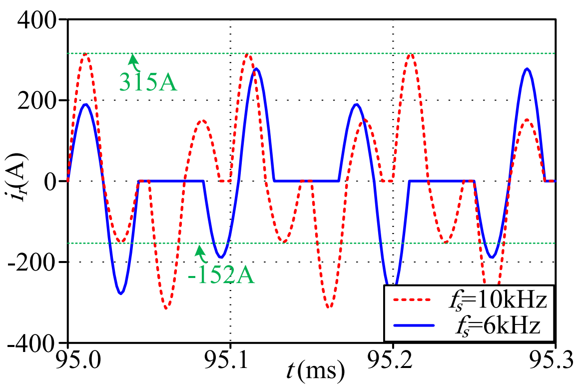

FIGURE 8. Simulation waveforms of i_r.

Fig. 8 shows the simulation waveforms of i_r under 6 kHz and 10 kHz. As can be seen, peak currents are different under different V_o and I_{pF} is higher while I_{pB} is lower under larger V_o, which has a good agreement with the theoretical analysis. To compare the exact theoretical and simulation values, without loss of generality, the case of 10 kHz will be discussed in this section. From Fig. 8, I_{pF} and I_{pB} of 10 kHz are about 315 A and 152 A in simulation, respectively. When substituting $V_o = 58.3$ kV and the relative resonant parameters into (12), the theoretical I_{pF} and I_{pB} can be obtained as 315.7 A and 151.9 A, respectively. As a result, the simulation current values are very close to the theoretical results, showing a good consistency between them. Furthermore, I_{pF} of 315 A is reduced by 59.8% from 783 A under traditional PFM, which can be obtained according to (1). Based on (1) and (12), the peak current comparison can be obtained as in Table 2. Obviously, the peak current of proposed APFM is much smaller, where IGBTs with lower current stress can be utilized. At last, there is no current flowing in the primary

TABLE 2. Peak current comparison.

V_o	Traditional PFM I_{pF_t}	Proposed APFM I_{pF}	Reduced by
35 kV	783 A	315 A	59.8%
58.3 kV	657 A	189 A	71.2%

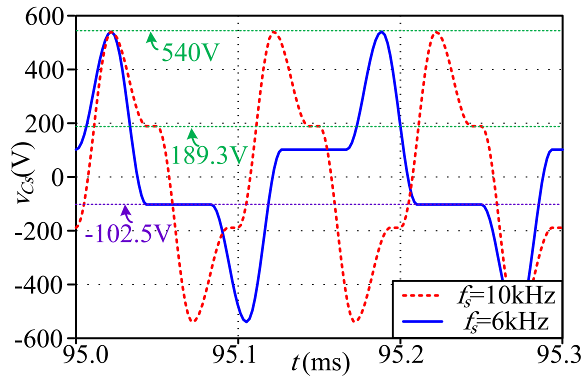

FIGURE 9. Simulation waveforms of v_{Cs}.

and/or secondary sides and B_t has no variation during the zero current stages under both f_s (cf. Fig. 11), avoiding the unexpected higher B_m case under the traditional PFM.

The simulation waveforms of v_{Cs} are shown in Fig. 9, where V_m is exactly the same of V_{in} (540 V) under different f_s. Moreover, V_f is −102.5 V due to the smaller V_o under 6 kHz while V_f is 189.3 V under 10 kHz due to larger V_o, and both values are very close to the theoretical results of (10). As can be concluded, the resonant capacitor voltage has a good agreement with theoretical analysis.

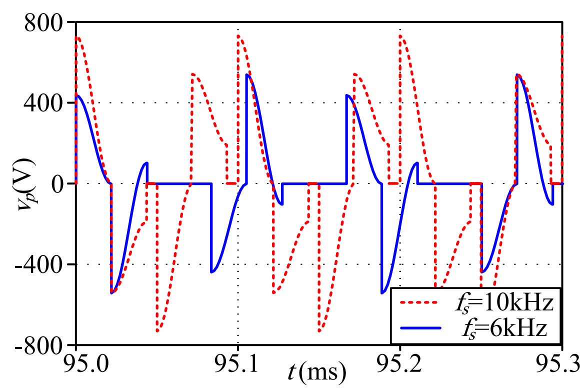

FIGURE 10. Simulation waveforms of v_p.

Since i_r keeps unchanged with the value of zero during the zero current stages, there is no voltage variation on v_p as well, as shown in Fig. 10. As can be seen, v_p keeps unchanged with the value of zero during the zero current stages regardless of the increase of f_s and V_o. Furthermore, B_t keeps unchanged with the value of zero during the zero current stages as shown in Fig. 11 under different f_s. B_m is 0.458 T under 10 kHz with higher V_o, which is close to the theoretical value of 0.459 T according to (13). Consequently, the unexpected

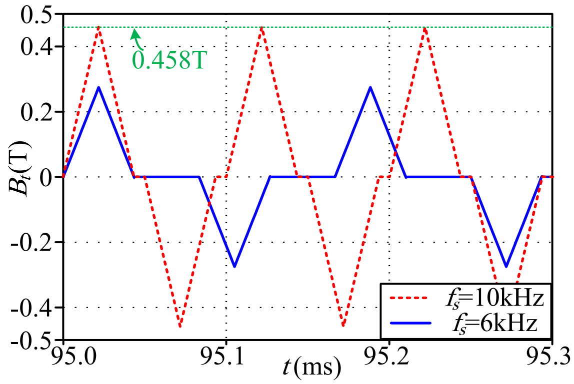

FIGURE 11. Simulation waveforms of B_t.

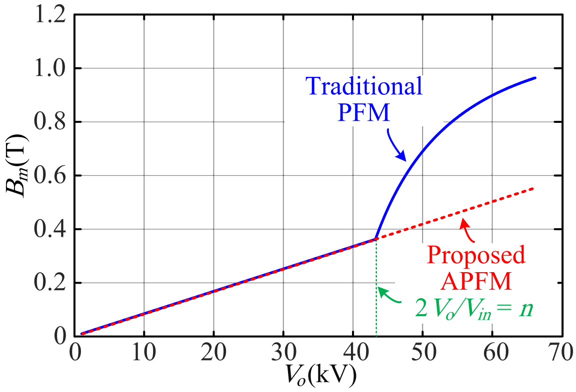

FIGURE 12. Comparison of B_m between the proposed APFM and traditional PFM with constant on-time.

higher B_m case under traditional PFM is avoided even when $n < 2V_o/V_{in}$.

The B_m variation curves under different V_o of the proposed APFM and traditional PFM with constant on-time are demonstrated in Fig. 12. As can be seen, B_m is exact the same under two different controls when $n > 2V_o/V_{in}$. Additionally, it is easy to find that with the increase of V_o, $2V_o/V_{in}$ will be higher than n. B_m of the traditional PFM will increase rapidly while B_m of the proposed APFM still increases linearly with the increase of V_o and is much smaller. Hence, with the proposed APFM, n can be designed only based on $n > V_o/V_{in}$ to avoid the unexpected increase of B_m.

As can be concluded, all the simulation results well validate the theoretical analysis. By employing the proposed APFM with constant on-time, all switches have at least 50% smaller peak current and the DCM-SRC can get different V_o under different f_s. B_m of the proposed control is proportional to V_o no matter $2V_o/V_{in}$ is smaller than n or not, leading to a much smaller B_m when compared to the traditional PFM with constant on-time.

V. EXPERIMENTAL RESULTS

An experimental platform of high-voltage high-power SRC was built for test, as shown in Fig. 13(a), where the four switches are IGBTs of FZ900R12KE4 (1200V/900A) from Infineon and C_s is composed of six capacitors (each one is 1 μF). The drivers for Q_2 and Q_4 are slightly complex, but there are at least two ways to realize it easily. The first way is to adopt a CD4071B chip, which is a quad 2-input OR gate chip. As shown in Fig. 14, the original drivers of $D_1 \sim D_4$ can be easily obtained from DSP28335 with the phase-shift function. Then $D_1 \sim D_4$ are sent to the CD4071B chip, where D_1 and D_4 are inputs of one OR gate while D_2 and D_3 are inputs of another OR gate. As a result, the drivers for Q_2 and Q_4 can be obtained. The second way is to adopt FPGA. One can write the bottom code to get any kinds of drivers from GPIOs (General-purpose input/output) of FPGA, and then the signals from these GPIOs are sent to the driver board. It is very convenient and has very high degree of freedom since even more complex drivers can be obtained easily. Moreover, the FPGA can sample the needed voltage and current signals, which are sent to DSP through a DMA. And the DSP will be in charge of the rest functions, for example the closed-loop-control, start-up, and protections. Hence, the second way is adopted to control the SRC in this paper.

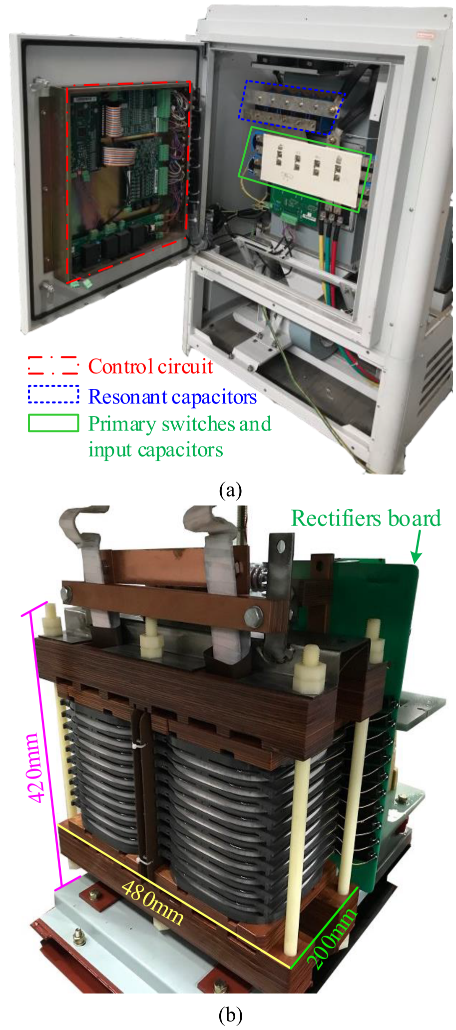

FIGURE 13. Experimental platform. (a) The whole SRC system. (b) Transformer with diode rectifiers (Transformer size: 480*200*420mm).

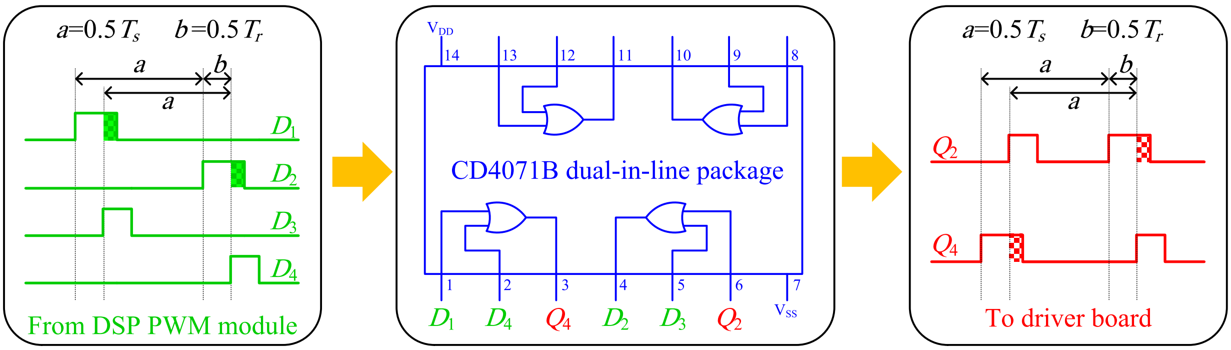

FIGURE 14. Adopting a CD4071B chip to get the drivers for Q_2 and Q_4.

TABLE 3. Experimental results of electric field load.

	f_s (kHz)	Measured V_{in} (V)	Measured I_o (mA)	Equivalent R_o (kΩ)	Measured V_o (kV)	Theoretical V_o (kV)	$2V_o/V_{in}-n$
Fig. 16(a)	4.50	528	353	83.85	29.60	29.78	–47.88
Fig. 16(b)	5.80	524	455	78.68	35.80	35.96	–23.36
Fig. 16(c)	8.20	523	632	72.58	45.00	45.79	12.08

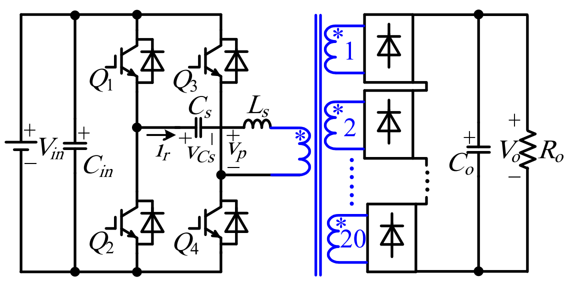

FIGURE 15. Multi-winding structure for high-voltage high-power transformer.

The isolation and heat dissipation are two key issues of the high-voltage high-power transformer. To lower down the difficulty, the multi-section and multi-layer structure of the secondary winding discussed in [23] can be adopted, with which the parasitic capacitance can be reduced as well. Furthermore, the multi-winding structure is employed to make the rectifiers more easily to produce, as shown in Fig. 15. There are 20 secondary windings and 20 full-bridge rectifiers with lower voltage rating rectifier diodes. As a result, the high-voltage high-power transformer is shown in Fig. 13(b). The primary and secondary winding turns are 12 and 1920, respectively, leading to $n = 160$. The leakage inductance of the manufactured transformer, functioning as the resonant inductor, is about 8 μH. The resonant capacitor is 6 μF, and the resonant period T_r is about 43.5 μs. The needed power is supplied by the rectified 380 V three-phase utility grid.

Since the ESP is one typical high-voltage high-power application scenario and the load of which is electric field, an electric field load is adopted for the first experiment. The average V_{in}, V_o, and output current I_o are measured in Table 3, and the equivalent R_o is obtained by calculating V_o/I_o with the measured average values. Then the theoretical V_o can be calculated based on (15) and are very close to the measured V_o, implying the data are reliable. As presented in Table 3, the equivalent R_o is not a constant value since the time-varying nature of electric field (cf. Fig. 2(b) in [1] and Fig. 7 in [26]). As shown in Fig. 16, some reasonable dead time is added between two adjacent forward and backward resonances. Without loss of generality, one can easily tell all the ZCS transitions presented in Fig. 16(a). As can be seen, there are ten ZCS time instants in one switching period, in which the two dashed green lines stand for the instants of current flowing through the anti-paralleled diodes with ZVZCS realized. Additionally, the peak current of the first experiment is about 300 A, while it can be as high as 700 A with similar V_o under the traditional PFM with constant on-time according to (1). As can be calculated, it is reduced by 57%. The experimental V_m equal to V_{in} and are almost the same under different f_s, indicating $|V_f| < V_{in} = V_m$. Hence, the experimental results of both resonant current and resonant capacitor voltage have a good agreement with the theoretical analysis. During the zero current stages, v_p has high-frequency oscillations caused by the parasitic capacitors of IGBTs on the primary side. Even though, the average value of v_p during each zero current stage can be thought as zero no matter $n < 2V_o/V_{in}$ or not, indicating B_t is zero during each zero current stage with B_m not affected. As a result, the high-frequency oscillations have no impact on B_m, which is proportional to V_o, and the unexpected higher B_m case under traditional PFM with constant on-time is avoided. In addition, the output voltage can be as high as 45 kV with the equivalent R_o of 72.58 kΩ according to Table 3, leading to the power is about 28 kW. And the SRC system efficiency is about 94%.

To further validate the lower B_m of the proposed APFM with constant on-time, the second experiment is conducted

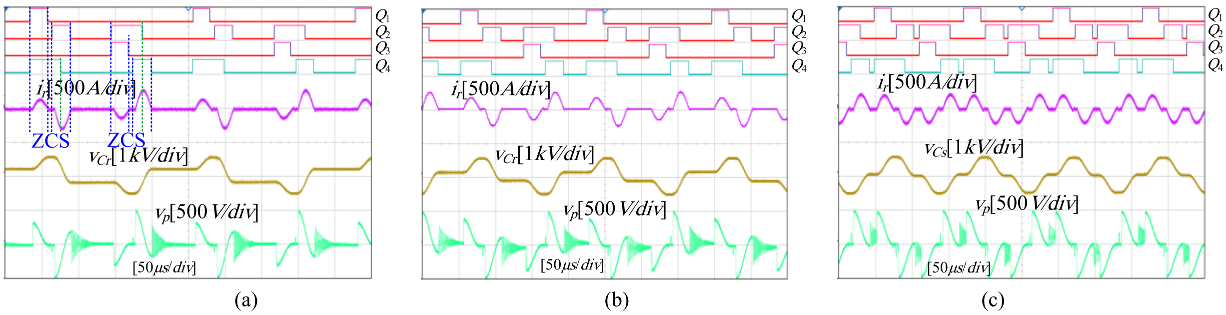

FIGURE 16. Experimental waveforms with electric field load under proposed APFM. (a) $f_s = 4.5$ kHz. (b) $f_s = 5.8$ kHz. (c) $f_s = 8.2$ kHz.

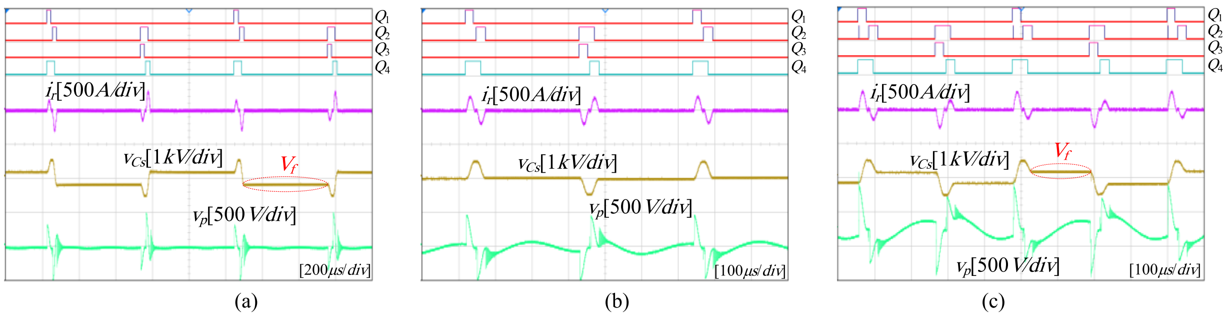

FIGURE 17. Experimental waveforms with a resistive load of about 300 kΩ under proposed APFM. (a) $f_s = 0.97$ kHz and $V_o = 25.8$ kV. (b) $f_s = 1.6$ kHz and $V_o = 38.2$ kV. (c) $f_s = 2.33$ kHz and $V_o = 50$ kV.

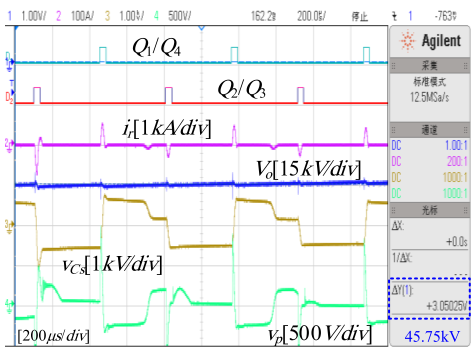

FIGURE 18. Experimental waveforms with a resistive load of about 300 kΩ under traditional PFM.

with a constant resistor load of about 300 kΩ. As shown in Fig. 17, all IGBTs can easily realize ZCS under different f_s and V_o. Referring to the dashed red circles in Fig. 17(a) and (c), V_f increases from negative value to positive value with the increase of V_o. From Fig. 17(c), even V_o is up to 50 kV, the waveforms of i_r and v_{Cs} are normal, indicating the transformer core is unsaturated. While under the traditional PFM with constant on-time, all the current and voltage waveforms are abnormal and the transformer core is saturated when V_o is only 45.75 kV, as shown in Fig. 18. Hence, the proposed control can get lower B_m to keep away from the core saturation problem. It can be found that except for the high-frequency oscillations at the start of each zero current stage, there are relative low-frequency oscillations during each zero current stage in v_p, as shown in Fig. 17. The low-frequency oscillations are caused by the resonance of magnetizing inductor on the secondary side, winding capacitor, and small parasitic capacitors of rectifier diodes. The equivalent magnetizing inductor on the secondary side can be as large as 200 H due to $n = 160$, leading to its relatively low oscillation frequency. And the impact of such low-frequency oscillations on B_m will be discussed in detail in the future paper.

In summary, the theoretical analysis and simulation results are well testified by the experimental results. ZCS can be achieved for all IGBTs and no matter the result of $2V_o/V_{in} - n$ is positive or negative, there is $|V_f| < V_{in}$ and B_t is zero during each zero current stage. The most important is that the proposed APFM has smaller peak current for IGBTs and lower B_m for transformer core.

VI. CONCLUSION

The high-voltage high-power DCM-SRC can be employed as power supply for equipment such as ESP and X-ray power generator. The proposed APFM with constant on-time can meet the requirement of a wide output voltage range for such applications, where the output voltage increases linearly with the increase of operating frequency and fully ZCS can be realized for all switches among the whole operation range. By employing the proposed APFM, the resonant capacitor voltage is never larger than the input voltage and there is no variation in MFD during the zero current stages no matter what the transformer turns ratio is. Thanks to that, the MMFD of DCM-SRC is proportional to the output voltage or operating frequency, owning smaller MMFD than the traditional PFM with constant on-time and the high-power transformer can be designed at the highest operating frequency. Moreover, all switches have at least 50% smaller peak current and IGBTs with lower current stress can be adopted. All of the conclusions are well validated by the simulation and experimental results.

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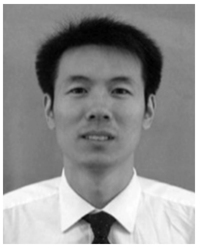

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