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A Pseudo-Constant Frequency Constant On-Time Buck Converter With Internal Current Ripple Injection and Output DC Offset Cancellation

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ABSTRACT A constant on-time buck converter with internal inductor current synthesizer and output DC offset cancellation technique is proposed. A fully integrated inductor current synthesizer based on valley voltage detector is employed to avoid system instability for constant on-time converters with low-ESR output capacitors. Moreover, the valley voltage detector could shift the emulated inductor current signal to zero valley level. In this way, the output DC offset due to ripple injection variation could be eliminated. An on-time circuit with comparator delay compensation is presented to alleviate the switching frequency variation. The small-signal model and design criteria are derived for system stability design. The circuit has been implemented with 0.18 μm BCD process. The measurement results show that the transient response is about 15.4 μs and the overshoot or undershoot voltage is less than 36 mV when the load transient between 1 A and 5 A for input voltage of 12 V and output voltage of 1.05 V. The switching frequency across load variation $\Delta f_{SW}/\Delta I_{LOAD}$ is 4.6 kHz/A at the nominal frequency of 700 kHz. The output DC offset is less than 10 mV in case of 4 A load current change.

INDEX TERMS Constant on-time control, emulated inductor current synthesizer, ripple-based converter, switching frequency, valley voltage detector.

I. INTRODUCTION

With the rapid development of semiconductor manufacturing technology, the power consumption of high-performance microprocessors drastically increases although the supply voltage is scaled down to sub-1V. Consequently, low-voltage, low output ripple, high-power, fast transient response, and high efficiency have become the most important design criteria for DC-DC converters. The conventional converters often use pulse width modulation (PWM) control schemes such as voltage mode or current mode to regulate the output voltage. However, these control schemes are difficult to meet the requirements for increasingly fast transient response due to the finite loop bandwidth limited by the switching frequency.

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The ripple-based constant on-time (COT) converters have the advantages of simple architecture, fast load transient response [1]–[3], and hence are suitable for today's high-power electronics. For the past several years, many researchers focus on solving the following problems in COT converters [4]–[19]. The first is the subharmonic stability problem. To meet the requirements of low output ripple, the converters generally adopts output capacitor with low equivalent series resistor (ESR) for modern low-voltage regulators. However, it suffers from the subharmonic stability due to the lagging phase of the output voltage ripple relative to the inductor current ripple. The second is the output DC offset problem [20]. The COT converters generally adopt the valley voltage control, and the valley of the output voltage is regulated to the preset voltage. Therefore, the output DC offset is proportional to the output voltage ripple. When a large-ESR output capacitor

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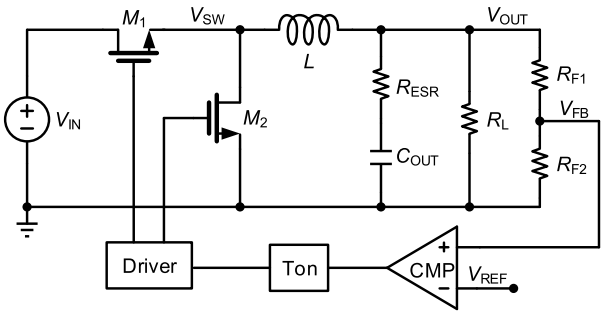


FIGURE 1. Circuit diagram of a general constant on-time regulator.

is adopted, the output voltage ripple will be approximately proportional to the load current. In addition, a larger-ESR output capacitor results in a larger output ripple. The third is the frequency variation problem. The COT converter is a clock-free architecture, and suffers from severe frequency variation with the changes of input voltage, output voltage, or load current.

Some compensation techniques such as ripple injection methods have been proposed to ensure the system stability. In [13], subharmonic stability conditions are derived for inductor current ripple feedback methods, and a sensing resistor in series with the inductor is used to obtain the inductor current ripple information. However, the series resistor introduces additional power consumption. An anti-ESL/ESR variation lossless sensing method by using switch capacitor technique is presented in [14]. However, these methods have not deal with inductor current DC value, and results in output DC offset. A sensing technique based on the inductor DC resistance (DRC) in [15]–[17] have been proposed to eliminate the power loss caused by the sensing circuit. Moreover, a high pass filter [15] or a differential difference amplifier [16], [17] is adopted to correct the output DC offset. However, the inductor DCR is sensitive to temperature variation. An internal inductor ramp signal is generated by integrating the phase signal and removing the DC value using a DC value extractor in [18]. Furthermore, an offset cancellation method by accurately adjusting the reference voltage to cancel the output DC offset is presented. A monolithic self-calibration method by sensing the average output voltage of converter and dynamically reducing offset with digital tuning the reference is proposed in [21]. However, the output DC offset is so small that the reference voltage is not easy to be accurately adjusted. In addition, the frequency stability of constant on-time buck converter is generally affected by on-time variation under different operating conditions [22]. To improve the frequency stability, the converter in [23] adopts a frequency locked loop to generate a constant frequency, and the circuits in [24] utilize predicting correction technique (PCT) to suppress the switching frequency variation. However, the PCT technique requires the accurate value of device parasitic resistances, and large-ESR output capacitor is required to ensure the system stability.

In this paper, an emulated inductor current (EIC) synthesizer based on valley voltage detector is proposed by only using the phase signal V_{SW}. The phase signal is integrated to generate an inductor current ripple signal, and then its valley value is removed by using a valley voltage detector to generate an EIC signal with zero valley level. The EIC signal is superposed on the output feedback voltage, and then compared with the reference voltage to regulate the output voltage. In this way, the output DC offset due to ripple injection variation could be eliminated. The switching frequency variation is suppressed by adjusting the trip voltage of the on-time comparator. The rest of the paper is organized as follows. Section II illustrates the system architecture of the proposed circuits. Section III shows the small-signal model. Section IV illustrates the implementation of our proposed circuit, and Section V presents the measurement results. A conclusion is provided in Section VI.

II. SYSTEM ARCHITECTURE DESIGN

A. CONVENTIONAL COT CONVERTERS

In COT converters, the output voltage ripple is utilized as the PWM ramp to compare with the reference voltage to regulate the output voltage. The feedback signal V_{FB} contains the ESR ripple voltage V_{ESR} and output capacitor's ripple voltage V_C. The value of V_{ESR} is proportional to the inductor current I_L, and there is no time delay between them. However, the capacitor ripple voltage V_C has a time delay relative to the inductor current I_L. When the feedback voltage ripple is dominated by V_C, the feedback signal has a large lag phase relative to the inductor current ripple, resulting in possible subharmonic stability problem. An output capacitor with large-ESR is generally adopted to generate sufficient ESR ripple voltage in conventional COT converters. However, this method is not suitable for modern converters in terms of low output voltage ripple requirement.

Generally, the converters with low output voltage ripple require a low-ESR output capacitor. In this situation, an external ripple signal proportional to the inductor current is usually injected to the feedback voltage to generate sufficient feedback ripple. The generated feedback ripple signal is similar to the ripple signal with large-ESR capacitor. In this way, the ripple injection method could ensure the system stability. This paper proposed a fully on-chip inductor current ripple injection method for COT converters with low-ESR output capacitor.

B. ARCHITECTURE OF THE PROPOSED CONVERTER

The architecture of the proposed COT converter with EIC and output DC offset cancellation is shown in Fig. 2. A first-order RC filter composed of R_1-R_2, and C_1 is introduced to generate a ripple signal V_{RI} to emulate the inductor current. The valley voltage detector tracks the minimum voltage of the emulated ripple signal through a negative feedback loop. The DC offset cancellation circuit adopts a transconductance amplifier to remove the DC value of the emulated inductor current signal. Then, the emulated inductor ripple signal V_{EIC} is superimposed on the feedback voltage V_{FB} using a

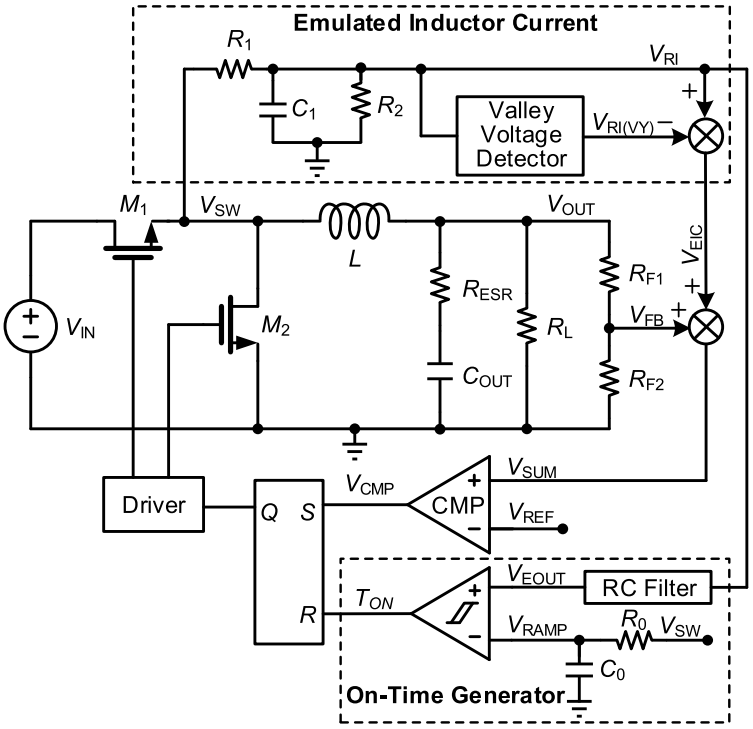


FIGURE 2. Circuit diagram of the proposed constant on-time buck converter.

summation circuit to generate the overall feedback signal V_{SUM}. The overall feedback signal has sufficient ripple, and compares with a reference voltage V_{REF} to generate the PWM signal. The constant on-time generator calculates the on-time of each cycle by comparing the output voltage with a ramp signal relevant to the input voltage.

C. PROPOSED RIPPLE INJECTION METHOD

The on-chip EIC circuit obtains the current ripple signal V_{EIC} by only sensing the phase signal V_{SW}. Then, the current ripple signal V_{EIC} is injected to the feedback loop, and superposed on the output feedback voltage V_{FB} to generate the overall feedback information V_{SUM}, which is compared with the reference voltage V_{REF} to regulate the output voltage V_{OUT}. The ripple injection method relaxes the stability constraint, and allows low-ESR ceramic output capacitors instead of large-ESR capacitors. Furthermore, the output voltage or current sensing signal is not required to feedback, and there is no need to add any extra IC pin for this control scheme. Therefore, this circuit only requires the phase signal V_{SW} to synthesize both the inductor current and output voltage signals, and the circuit is suitable for highly integrated on-chip implementations.

In the EIC circuit, the inductor current ripple signal V_{RI} is generated by filtering the phase signal V_{SW} with a first-order RC filter. Then, the signal V_{RI} is processed by a valley voltage detector to obtain its valley value $V_{RI(VY)}$. The valley value $V_{RI(VY)}$ is removed from the signal V_{RI} to generate the emulated inductor current signal V_{EIC} with zero valley value. The average voltage of V_{RI} represented by $V_{RI(DC)}$ can be obtained as follows.

$$V_{RI(DC)} = DV_{IN}\frac{R_2}{R_1+R_2} = V_{OUT}\frac{R_2}{R_1+R_2} \tag{1}$$

where D, V_{IN}, and V_{OUT} stand for the duty cycle, the input voltage, and the output voltage, respectively.

It is assumed that the filtering time constant $(R_1//R_2)C_1$ is much larger than the switching period T, so the magnitude of the signal V_{RI} is relatively small compared with the input voltage or the output voltage. According to (1), the current charging or discharging the capacitor C_1 is given by

$$\begin{aligned} I_{charge} &= \frac{V_{IN}-V_{RI(DC)}}{R_1} - \frac{V_{RI(DC)}}{R_2} \\ &= \frac{V_{IN}-V_{OUT}}{R_1} \end{aligned} \tag{2}$$

$$I_{discharge} = \frac{V_{RI(DC)}}{R_1//R_2} = \frac{V_{OUT}}{R_1} \tag{3}$$

According to (2) and (3), the slope of the emulated inductor current ripple V_{EIC} is proportional to the actual inductor current I_L. The slope is determined by resistor R_1 and capacitor C_1, and is independent of resistor R_2. However, the added resistor R_2 is very important, and it has two advantages. On the one hand, the DC value of the emulated signal V_{RI} could be set to a proper value according to (2), which is very important for high-voltage converters because the internal control loop is often required to operate in the low-voltage domain. On the other hand, the position of the zero for the loop transfer function could be adjusted flexibly to ensure

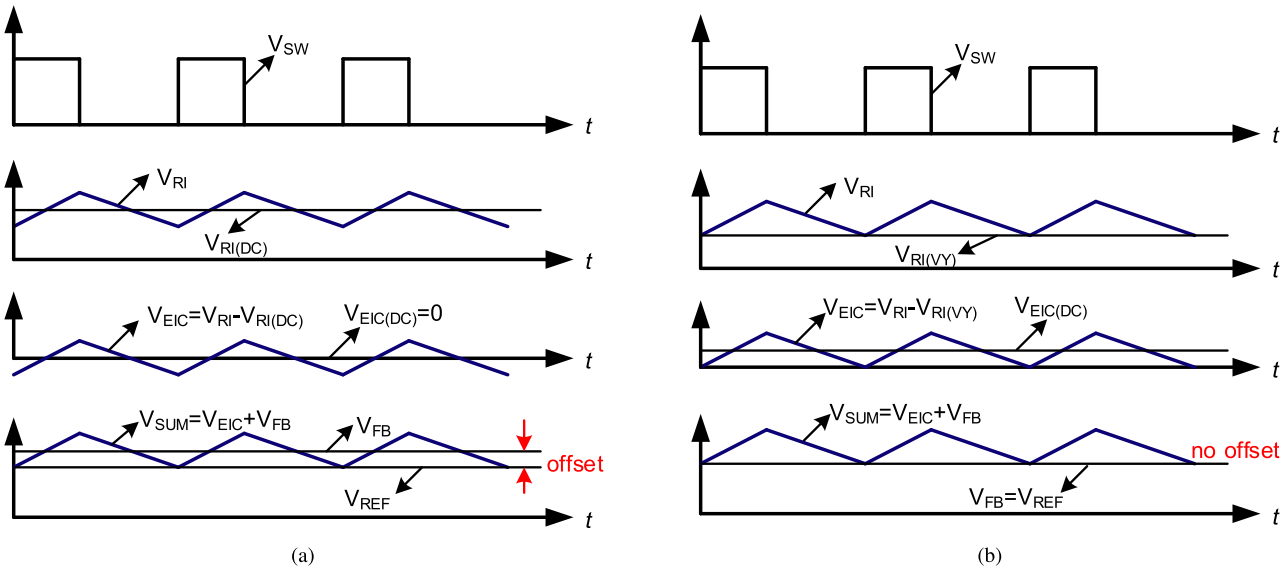


FIGURE 3. Timing diagram of constant on-time converter. (a) w/o output DC offset cancellation. (b) w/i output DC offset cancellation.

system stability, which will be illustrated in Section III. In this way, the overall feedback voltage ripple is effectively enhanced by the additional ripple V_{EIC} and makes the system more stable.

D. DC OFFSET CANCELLATION

The proposed control scheme has another advantage of nearly no output DC offset induced by injecting the emulated inductor current signal, which can be illustrated by the timing diagram for the conventional and proposed constant on-time converters shown in Fig. 3. When a low-ESR ceramic output capacitor is adopted, the output voltage ripple is small, and the feedback voltage V_{FB} ripple value can be ignored reasonably. Therefore, the ripple of the summation signal V_{SUM} is dominated by the emulated inductor signal. As shown in Fig. 3 (a), the DC value of V_{RI} is generally extracted by a second order RC filter in the conventional method. Then, the DC value is removed from the signal V_{RI} to obtain the emulated inductor current signal V_{EIC} with a zero valley value. Therefore, the DC value of the overall feedback signal V_{SUM} is equal to the value of V_{FB}. Because the valley of V_{SUM} is regulated to V_{REF}, the feedback voltage V_{FB} has a DC offset which is equal to the magnitude of V_{EIC}. Furthermore, the magnitude of V_{EIC} is dependent on the input voltage, output voltage, and load current. As a result, the feedback voltage V_{FB} or the output voltage V_{OUT} has a variable DC offset. On the other hand, the proposed method replaces the conventional RC filter with a valley voltage detector, which can extract the valley value of V_{RI}. As shown in Fig. 3 (b), the valley value $V_{RI(VY)}$ is removed from the signal V_{RI} to generate the EIC signal V_{EIC} with zero valley value. In this way, the valley voltage of the summation signal V_{SUM} is equal to the value of V_{FB}. As a result, the feedback voltage V_{FB} is always regulated to V_{REF}, and the output voltage V_{OUT} has a near zero DC offset.

An on-time generator circuit shown in Fig. 2 is designed to set the on-time of the oscillator. The average voltage of V_{RI} is proportional to the output voltage V_{OUT} according to (1), and hence the equivalent output voltage V_{EOUT} can be set to be equal to $V_{RI(DC)}$, which is given by

$$V_{EOUT} = V_{RI(DC)} = V_{OUT}\frac{R_2}{R_1 + R_2} \tag{4}$$

The filter composed of R_0 and C_0 is introduced to integrate the phase signal V_{SW} to generate a ramp signal V_{RAMP} during on-time, which is then compared to the emulated output voltage V_{EOUT} to generate the on-time T_{ON}. It is assumed that the peak value of V_{RAMP} is much smaller than V_{IN}, which can be achieved by the circuit design. Therefore, the charging current can be expressed approximately as V_{IN}/R_0 during the on-time, and the on-time is derived as

$$T_{ON} = D \cdot T = \frac{V_{EOUT} C_0}{V_{IN}/R_0} \tag{5}$$

Based on (4)-(5), the switching period of the constant on-time converter is given by

$$T = \frac{R_2}{R_1 + R_2} R_0 C_0 \tag{6}$$

Both the ramp signal V_{RAMP} and inductor current ripple signal V_{RI} are generated through a first-order RC filter. However, the time constant of each filter is different. The time constant R_0C_0 for generating ramp signal is approximated to the switching period, but the time constant $(R_1//R_2)C_1$ for generating current ripple signal is much larger than the switching period.

As implied by above analysis, the EIC signal and the equivalent output voltage are generated only on the basis of the phase signal V_{SW}, meaning that the proposed method is suitable for fully integrated systems without adding any extra IC pin.

III. SMALL-SIGNAL ANALYSIS

To analyze the system stability, the small-signal model for the converter should be developed [25]–[28]. The small-signal control block diagram for the proposed constant on-time buck converter with EIC and offset cancellation is shown in Fig. 4. There are two control loops, including an inner current loop and an outer control loop.

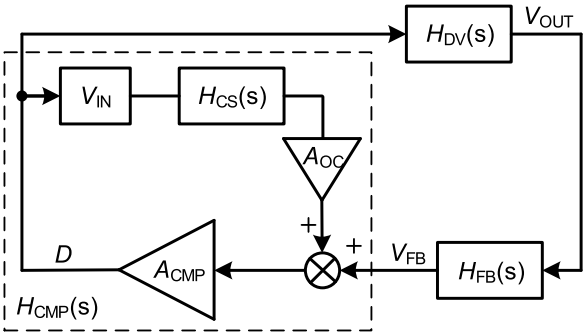


FIGURE 4. Control block diagram of the constant on-time converter.

The transfer function $H_{CS}(s)$ of the EIC circuit is obtained as

$$H_{CS}(s) = \frac{R_2}{R_1+R_2}\frac{1}{1+s\frac{R_1R_2}{R_1+R_2}C_1} = \frac{R_2}{R_1+R_2}\frac{1}{1+sT_C} \tag{7}$$

where T_C is expressed as

$$T_C = \frac{R_1R_2}{R_1+R_2}C_1 \tag{8}$$

The small-signal block diagram of the inner current loop is included in the dashed box in Fig. 4. The relationship between ΔD and ΔV_{FB} is obtained as

$$(\Delta D V_{IN} H_{CS}(s) A_{OC} + \Delta V_{FB}) A_{CMP} = \Delta D \tag{9}$$

Therefore, the closed loop transfer function $H_{CMP}(s)$ from V_{FB} to ΔD for the inner current loop is given by

$$H_{CMP}(s) = \frac{\Delta D}{\Delta V_{FB}} = \frac{A_{CMP}}{1 - V_{IN}A_{CMP}H_{CS}(s)A_{OC}} \approx -\frac{1}{V_{IN}H_{CS}(s)A_{OC}} \tag{10}$$

where A_{CMP} and A_{OC} are the gain of the PWM comparator and the gain of offset cancellation circuit, respectively. A_{CMP} is theoretically infinite, and A_{OC} has a much small value to compress the swing of the EIC signal.

Due to the fixed on-time control, the duty ratio can not change during on-time even though the output voltage changes, so the on-time has a delay factor expressed as

$$H_D(s) = e^{-sDT_{ON}} \tag{11}$$

Using the well-known state-space averaging model, the transfer function of the power stage, $H_{DV}(s)$ is derived as

$$H_{DV}(s) = \frac{V_{IN}(1+\frac{s}{\omega_{ESR}})}{1+\frac{2}{Q_0\omega_0}+(\frac{s}{\omega_0})^2} \tag{12}$$

where,

$$\omega_0 = \frac{1}{\sqrt{LC_{OUT}}} \tag{13}$$

$$Q_0 = R_L\sqrt{\frac{C_{OUT}}{L}} \tag{14}$$

$$\omega_{ESR} = \sqrt{\frac{1}{R_{ESR}C_{OUT}}} \tag{15}$$

The transfer function from V_{OUT} to V_{FB}, $H_{FB}(s)$ is given as

$$H_{FB}(s) = \frac{R_{F2}}{R_{F1}+R_{F2}} \tag{16}$$

According to (7)-(16), the open-loop transfer function $H_{OPEN}(s)$ is expressed as

$$H_{OPEN}(s) = H_{DV}(s)H_{FB}(s)H_{CMP}(s)H_D(s) \tag{17}$$

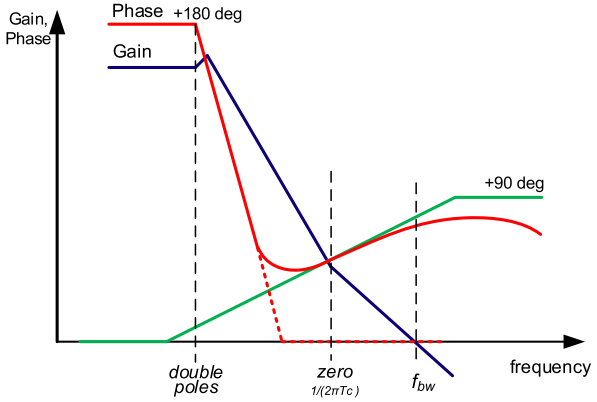


FIGURE 5. Bode plots of the open-loop transfer function.

The bode plots for $H_{OPEN}(s)$ are shown in Fig. 5. Because of the double poles introduced by the power stage, the gain decreases at a slope of −40 dB/dec, and the phase varies from −180 degrees to 0. Therefore, the system could not be stable without compensation. In this paper, the EIC circuit introduces a zero, which makes the gain slope increase up 20 dB/dec, and the phase increase up to 90 degrees. As a result, an adequate phase margin could be achieved to guarantee the system stability.

The parameters of external components for different operating condition are not the same. The feedback resistor R_{F2} and the reference voltage V_{REF} is equal to 22 kΩ and 0.7 V, respectively. Therefore, the other feedback resistor R_{F1} for the output voltage of 1.05 V and 3.3 V is equal to 11 kΩ and 49.5 kΩ, respectively. According to (17), the loop gain and phase margin is decreased with the increase of output voltage. A feedforward capacitor in parallel with resistor R_{F1} is required for high output voltage conditions to ensure the

system stability. Actually, the feedforward capacitor introduces an extra zero to improve the phase lag characteristics. The value of the feedforward capacitor C_{F1} is generally in the range of 5 pF and 22 pF. In the emulated inductor current circuit, $R_1 = 600$ kΩ, $R_2 = 300$ kΩ, and $C_1 = 5$ pF. Other parameters for the simulation are $V_{IN} = 12$ V, $I_{LOAD} = 3$ A, $f_{SW} = 700$ kHz, $C_{OUT} = 22$ μF, $L = 1.5$ μH. The bode plots of the open-loop transfer functions are simulated under the output conditions of 1.05 V and 3.3 V. As shown by the simulation results in Fig. 6, the open-loop bandwidth is 128 kHz with 55 degrees phase margin (Fig. 6 (a)) and 80 kHz with 62 degrees phase margin (Fig. 6 (b)), when the output voltage V_{OUT} is set to 1.05 V and 3.3 V, respectively.

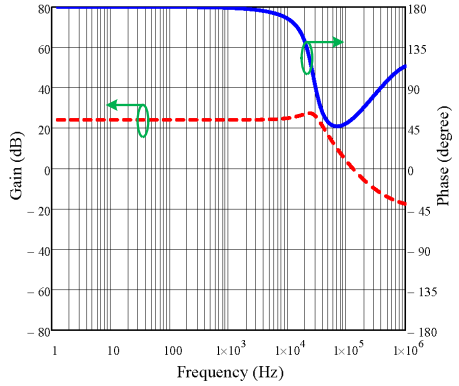


FIGURE 6. Bode plots under different conditions. (a) V_{IN}=12 V, V_{OUT}=1.05 V, and I_{LOAD}=3 A. (b) V_{IN}=12 V, V_{OUT}=3.3 V, and I_{LOAD}=3 A.

IV. CIRCUIT IMPLEMENTATION

A. CONSTANT ON-TIME GENERATOR

The circuit for the proposed constant on-time generator is given in Fig. 7, which can achieve more accurate on-time compared to the basic structure shown in Fig. 2. In the basic structure, the ramp signal V_{RAMP} is generated by a current charging capacitor C_0. During on-time, the charging current I_{0A} is decreased with the increase of the ramp signal. To achieve a constant charging current, a compensation circuit is introduced to add additional current I_{0B} to compensate

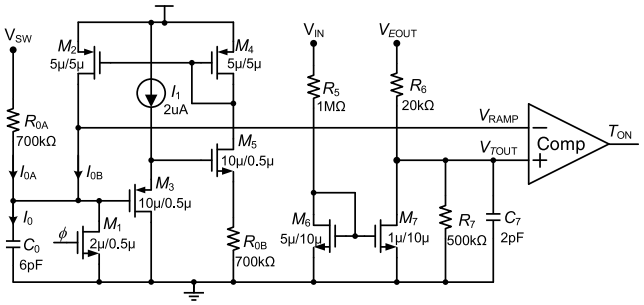


FIGURE 7. Circuit diagram of the constant on-time generator with frequency compensation.

the charging current variation. As a result, a constant charging current I_0 is obtained as

$$I_0 = I_{0A} + I_{0B} = \frac{V_{IN} - V_{RAMP}}{R_{0A}} + \frac{V_{RAMP}}{R_{0B}} = \frac{V_{IN}}{R_0}, \quad (R_0 = R_{0A} = R_{0B}) \tag{18}$$

According to (19), the charging current I_0 is proportional to the value of input voltage V_{IN}, and the slope of V_{RAMP} is proportional to V_{IN}. Therefore, the comparator delay changes with V_{IN} variation. Considering the comparator delay, (5) could be rewritten as

$$T_{ON} = \frac{V_{EOUT} C_0}{V_{IN}/R_0} + t_d \tag{19}$$

where t_d is the comparator delay. Because a larger slope of V_{RAMP} introduces a smaller comparator delay, a compensation circuit is required to ensure constant T_{ON}. The circuit consisted of resistor R_5 and transistors M_6-M_7 is adopted to generate a lower trip voltage V_{TOUT} for a higher input voltage V_{IN}. In this way, the on-time can be kept nearly constant and the switching frequency maintains small variation.

B. VALLEY VOLTAGE DETECTOR

As described in Sec. II, the emulated inductor current signal with zero valley voltage level is introduced to eliminate the output DC offset, in which the valley voltage detector is required to detect the valley voltage $V_{RI(VY)}$ of the signal V_{RI}. The circuit diagram of the valley voltage detector is shown in Fig. 8, in which the difference between $V_{RI(VY)}$ and

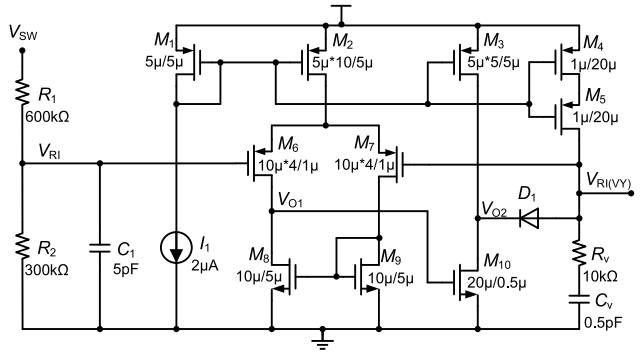


FIGURE 8. Circuit diagram of valley voltage detector.

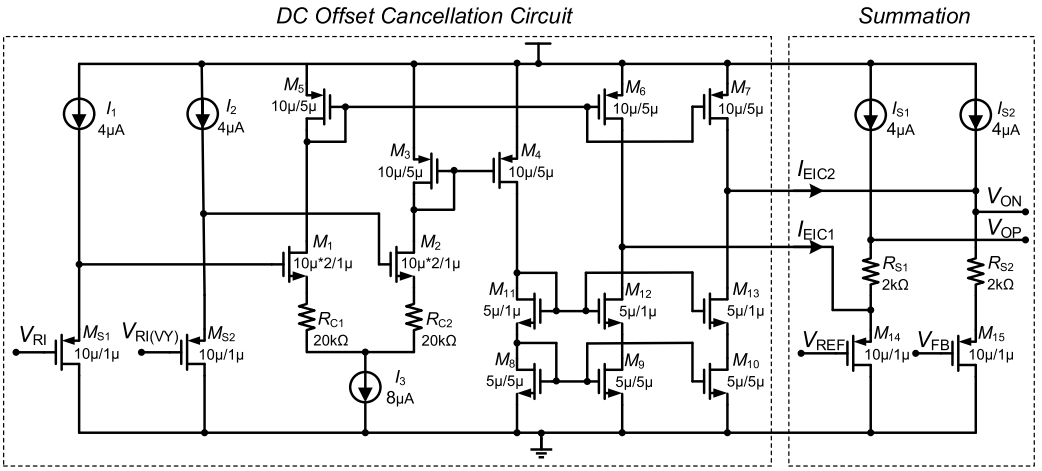


FIGURE 9. Circuit diagram of emulated inductor current and summation circuits.

V_{RI} is amplified by a two-stage operational amplifier. When $V_{RI(VY)}$ is larger than V_{RI}, the output of the amplifier V_{O2} will be pulled to a very low voltage level. Then, the diode D_1 is forward biased, and the capacitor C_V is discharged until $V_{RI(VY)}$ is no longer larger than V_{RI}. On the other hand, when $V_{RI(VY)}$ is smaller than V_{RI}, the output of amplifier V_{O2} will be pulled to a very high voltage level. Under this condition, the diode D_1 is reverse biased, and the capacitor C_V can not be charged by the path through diode D1, so $V_{RI(VY)}$ holds its value. The capacitor C_V can not be charged by the path through diode D_1. In case that the average voltage signal V_{RI} is increased, a charging path is required to charge the capacitor to a higher voltage level. To realize an extra charging path, the transistors M_4-M_5 with large channel length is introduced to generate a very small current of about 50 nA that always charges the capacitor C_V. The current is so small that the ripple of $V_{RI(VY)}$ could be neglected. In this way, the signal $V_{RI(VY)}$ could track the valley voltage signal V_{RI} all the time.

C. DC OFFSET CANCELLATION CIRCUIT AND SUMMATION CIRCUIT

In the proposed constant on-time converter, the output DC offset induced by load current variation is corrected with the DC offset cancellation circuit shown in Fig. 9. The DC offset cancellation circuit removes the DC value of the inductor current ripple signal V_{RI} to generate an emulated inductor current signal $I_{EIC1,2}$ with a zero valley value. Then, the emulated inductor current ripple signal is superposed on the feedback signal V_{FB} using summation circuit to generate large feedback ripple signal to improving the system stability. The DC offset correct circuit and summation circuit are implemented with operational transconductance amplifier, and source follower, respectively. The emulated inductor current signal $I_{EIC1,2}$ with zero valley vale could be derived as

$$I_{EIC1,2} = \frac{g_{m1,2}}{1 + g_{m1,2}R_{C1,2}}(V_{RI} - V_{RI(VY)}) \tag{20}$$

where g_{m1} and g_{m2} are the transconductance of transistors M_1 and M_2, respectively. The source degeneration resistors $R_{C1,2}$ are added to improve the linearity of the transconductance. The amplifier is designed with very low system DC offset. When the two input voltages are equal to each other, it can be considered that no current flows out of the amplifier. Therefore, the signal $I_{EIC1,2}$ keeps as zero valley current. The summation circuit is shown in the right part of Fig. 9, in which $R_{S1} = R_{S2}$, $I_{S1} = I_{S2}$. The emulated inductor current signal I_{EIC2} flows through resistor R_{S2}, and is then converted into the voltage drop across resistor R_{S2}. The differential output of the summation circuit is given by

$$V_{OP} = V_{REF} + (V_{GS14} + I_{S1}R_{S1}) \tag{21}$$

$$V_{ON} = V_{FB} + I_{EIC2}R_{S2} + (V_{GS15} + I_{S2}R_{S2}) \tag{22}$$

where V_{GS14} and V_{GS15} are the gate-source voltage of transistors M_{14} and M_{15}, respectively. The current flowing through transistor M_{14} or M_{15} is equal to $I_{EIC1,2} + I_{S1,2}$, so V_{GS14} is equal to V_{GS15}.

D. PWM COMPARATOR

The summation voltage V_{ON} is compared with the reference voltage V_{OP} to generate the off-time signal by using a PWM comparator with schematic shown in Fig. 10. The comparator consists of two stages including a fully differential

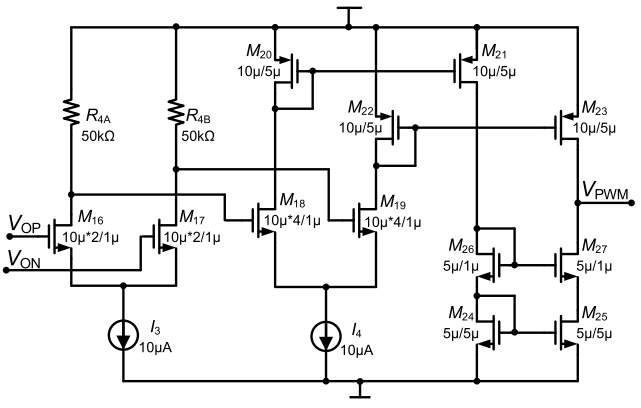
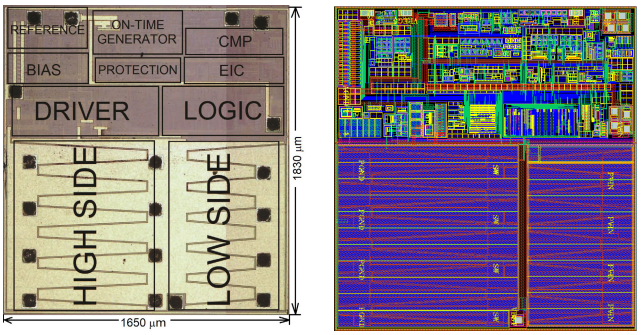
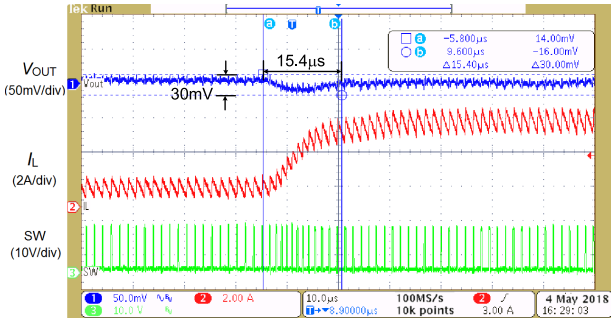


FIGURE 10. PWM comparator.

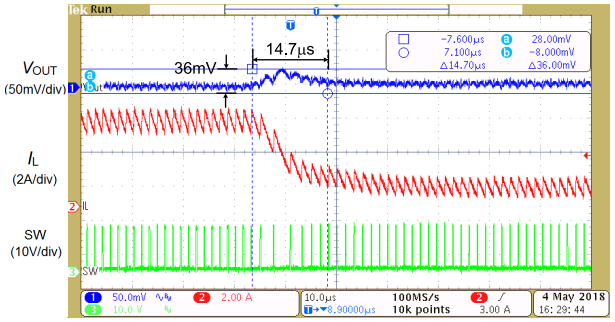


(a) (b)

FIGURE 11. (a) Chip microphotograph. (b) Chip layout.



(a)



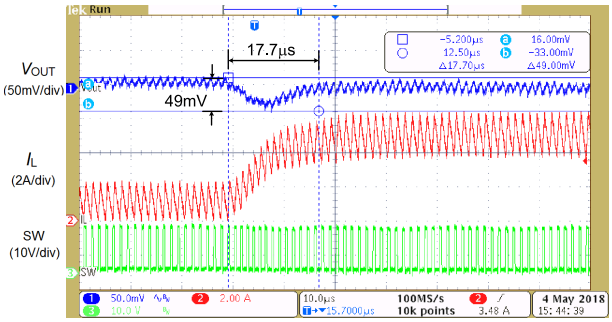
(b)

FIGURE 12. Measured load transient response under the condition of V_{IN} = 12 V, V_{OUT} = 1.05 V. (a) Load changes from 1 A to 5 A. (b) Load changes from 5 A to 1 A.

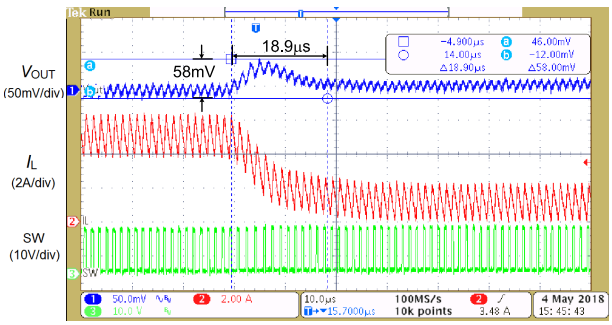
comparator followed by a symmetrical comparator to ensure high gain and wide bandwidth. Therefore, an accurate off-time with small delay time can be achieved.

V. EXPERIMENTAL RESULTS

The proposed constant on-time buck converter has been implemented with 0.18 μm BCD process. The chip microphotograph and the layout are shown in Fig. 11, and the buck converter occupies a total silicon area of 1830 × 1650 μm^2 including two on-chip power switches. The off-chip inductor is 1.5 μH. A low-ESR multilayer ceramic capacitor (MLCC) of 22 μF is adopted as the output capacitor, and the R_{ESR} is about 10 mΩ. The input voltage is in the range from 5 V to 12 V, and the output voltage is in the range from 1.05 V to 3.3 V. The maximum load current is 5 A,



(a)



(b)

FIGURE 13. Measured load transient response under the condition of V_{IN} = 12 V, V_{OUT} = 3.3 V. (a) Load changes from 1 A to 5 A. (b) Load changes from 5 A to 1 A.

and the nominal switching frequency f_{SW} is designed around 700 kHz. An internal LDO generates a regulated voltage of 5 V for the internal analog block as their supply voltage.

The fabricated constant on-time converter has been measured under different conditions. Fig. 12 shows the load transient response at input voltage of 12 V and output voltage of 1.05 V. When the load steps from 1 A to 5 A, the output voltage is settled within 15.4 μs, and the undershoot voltage is 30 mV as shown in Fig. 12 (a). When the load steps from 5 A to 1 A, the output voltage is settled within 14.7 μs, and the overshoot voltage is 36 mV as shown in Fig. 12 (b). Fig. 13 shows the load transient response at the input voltage 12 V and output voltage of 3.3 V. When the load steps from 1 A and 5 A, the output voltage is settled within 17.7 μs, and the undershoot voltage is 49 mV as shown in Fig. 13 (a). When the load steps from 5 A and 1 A, the output voltage is settled within 18.9 μs, and the overshoot voltage is 58 mV as shown in Fig. 13 (b). The results show that the proposed constant-on time control method achieves fast load transient response without using large-ESR output capacitors. Furthermore, the results in Figs. 12-13 also imply that the output DC offset is smaller than 10 mV when the load current changes between 1 A and 5 A.

The measured steady-state waveforms are shown in Fig. 14. The results show that an output voltage ripple of smaller than 20 mV is achieved under different conditions. Furthermore, the results also show that there is no subharmonic oscillation for the control with low-ESR ceramic output capacitors, which is benefited from the emulated inductor current method

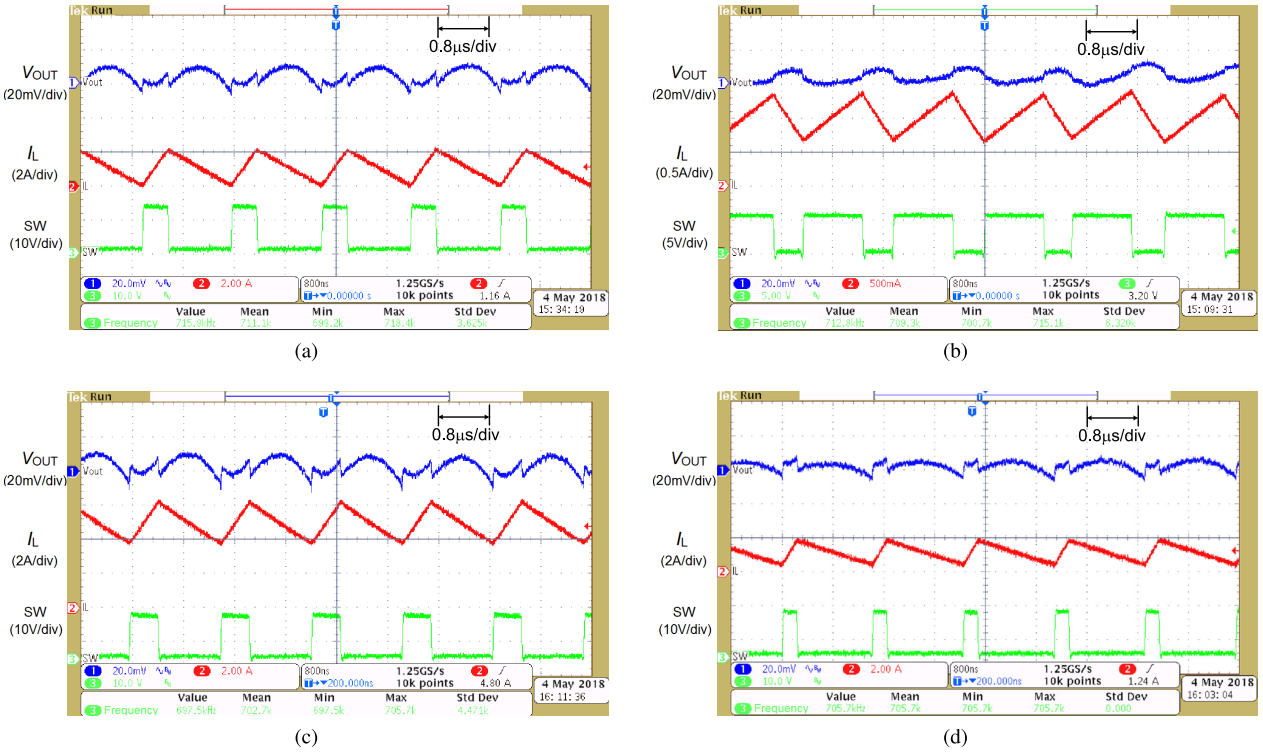


FIGURE 14. Measured steady-state waveforms under different conditions. (a) V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{LOAD} = 1 A. (b) V_{IN} changes from 12 V to 5 V. (c) I_{LOAD} changes from 1 A to 5 A. (d) V_{OUT} changes from 3.3 V to 1.8 V.

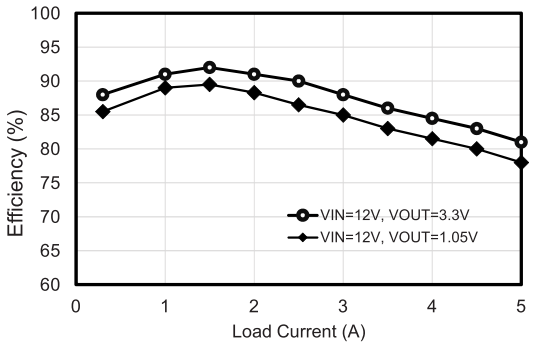


FIGURE 15. Measurement power efficiency versus load current.

has been introduced to generate the ramp signal without using large-ESR output capacitors. Under the condition of V_{IN} = 12 V, V_{OUT} = 1.05 V, and I_{LOAD} = 1 A, the switching frequency is 715.9 kHz as shown in Fig. 14 (a). When the input voltage V_{IN} is changed from 12 V to 5 V, the switching frequency is changed to 712.8 kHz as shown in Fig. 14 (b), achieving $\Delta f_{sw}/\Delta V_{IN}$ of 0.443 kHz/V. When the load current I_{LOAD} is changed to 1 A to 5 A, the switching frequency is changed to 697.5 kHz as shown in Fig. 14 (c), achieving $\Delta f_{sw}/\Delta I_{LOAD}$ of 4.6 kHz/A. When the output voltage V_{OUT} is changed to 3.3 V to 1.8 V, the switching frequency is changed to 705.7 kHz as shown in Fig. 14 (d), achieving $\Delta f_{sw}/\Delta V_{OUT}$ of 6.8 kHz/V. Therefore, the switching frequency exhibits a low variation relative to the change of V_{IN}, V_{OUT}, and I_{LOAD} with the compensated constant-on time generator.

TABLE 1. Performance summary and comparison.

Reference	[4]	[16]	[22]	[24]	This work
Control	Quasi-V^2	COT	AOT	PCT	COT
Process (nm)	350	28	180	28	180
V_{IN} (V)	2.7-3.3	3.3	2.7-3.6	3.3	5-12
V_{OUT} (V)	0.9-2.1	1.05	1-1.2	1.05	1.05-3.3
f_{SW} (MHz)	3	2.5	1	2.5	0.7
Max. I_{LOAD} (A)	0.5	1.7	1.1	1.7	5
ΔI_{LOAD}	0.45	1.4	0.7	1.4	4
L (μH)	2.2	1	N/A	1	1.5
C_{OUT} (μF)	4.4	4.7	N/A	4.7	22
R_{ESR} (mΩ)	<30	4	N/A	N/A	10
Max. Efficiency	93%	94%	88.2%	89%	92%
Transient T_R(μs)	2.8	5	10	10	15.4
Offset V_{OS}(mV)	20	4	N/A	N/A	10
$\Delta f_{SW}/\Delta I_{LOAD}$	N/A	N/A	52	5.7	4.6
FoM_1	2.67	2.38	N/A	1.19	2.53
FoM_2	0.38	2.98	N/A	N/A	3.9

$FoM_1 = \frac{L \cdot \Delta I_{LOAD} \cdot 10^2}{C_{OUT} \cdot f_{SW} \cdot T_R}$ $\quad FoM_2 = \frac{L \cdot \Delta I_{LOAD} \cdot 10^2}{C_{OUT} \cdot f_{SW} \cdot V_{OS}}$

The measured power efficiency is shown in Fig. 15, and the maximum efficiency of 92% is achieved at the load current of 1.5 A and output voltage of 3.3V. Two figure of merits (FoMs) are defined to evaluate the dynamic and static performance, respectively [16], [17]. A large FoM_1 represents fast transient response, and a large FoM_2 represents low-output DC offset. The performance summary and

comparison among the state-of-the-art constant on-time buck DC-DC converters are summarized in Table 1. The proposed converter has achieved fast load transient response, low-output voltage DC offset, and pseudo-constant switching frequency.

VI. CONCLUSION

This paper proposes a fully integrated emulated inductor current injection method to improve the system stability for constant on-time buck converters with low-ESR output capacitors. The output DC offset caused by ripple injection variation is eliminated by introducing a valley voltage detector. In addition, a comparator delay compensation technique for the on-time generator is presented to alleviate the switching frequency variation. The small-signal model and design criteria are derived for system stability design. The proposed converter has achieved fast transient response and low-output voltage ripple.

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