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Experiment on VCSEL Composed of Special Structure DBRs in Integrated Optoelectronic Chip

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ABSTRACT In this paper, we have demonstrated the feasibility of the proposed integrated chip by the experiments on its laser part of Vertical-cavity Surface-emitting Laser (VCSEL). The success of the integrated chip depends on the special designed cavity-in DBR, and the VCSEL's resonant cavity is composed by the cavity-in DBRs. With a gold reflector on top of the original integrated chip wafer to improve the Q value of the VCSEL's resonant cavity, the VCSEL is successful to lase. Its threshold current is 3 mA, the slope efficiency is 0.84 W/A and the estimated maximum light power is 30 mW. The experiment illustrates that the cavity-in DBR is reasonable and practical and makes foundation for the realization of the integrated chip in single-fiber bi-directional optical interconnects.

INDEX TERMS Vertical cavity surface emitting lasers, p-i-n diode, integrated optoelectronics, gold reflector.

I. INTRODUCTION

Vertical-cavity surface-emitting laser (VCSEL) exhibits great performance in short-reach data communications, such as low power consumption, high energy efficiency, easily to couple into the optical fiber due to its circular and non-astigmatic beam and low cost of manufacturing [1]. Since VCSELs still are and will continue to be dominant laser sources in the data centers, researchers have made efforts to improve the performance of the VCSELs as well as the whole optical fiber transmission link [2]–[7]. Remarkably, new transceivers of the monolithic lateral integration of VCSEL with different kinds of photodetectors at 850 nm wavelength were developed by Ulm University for single-fiber full-duplex optical communications [8]–[10]. Recently, our group has originally proposed several vertical integrated optoelectronic chip pairs for short-reach single-fiber bi-directional optical interconnects based on VCSEL structure [11]–[15]. The proposed integrated chips not only can enhance the utilization efficiency of the optical fiber, and so will reduce the amount of the fibers by half, but also simplify the fabrication process and lower the package costs. The integrated chip structure proposed in this paper is composed of VCSEL and PIN photodetector (PIN-PD), which transmits and receives optical signals simultaneously over two different wavelengths. Since the VCSEL is on top of the PIN-PD, both of the reflectors of VCSEL are special designed for two functions. One is to provide high reflectivity around lasing wavelength, and the other is to provide the reflectivity as low as 0% for allowing the incident light around receiving wavelength into the PIN-PD as much as possible. For this reason, a special structure of VCSEL's DBR is designed and analyzed [11], [12]. This kind of DBR is named as cavity-in DBR. For instance, the VCSEL's DBR of one terminal chip is constituted by inserting a $\lambda/4$ DBR, which has its central reflection wavelength λ of 850 nm setting at the chip's transmitting wavelength, into a low Q value resonant cavity, which has its resonant wavelength setting at the chip's receiving

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wavelength of 805 nm. For the other terminal chip, the functions of two wavelengths are exchanged and 850 nm wavelength is for receiving and 805 nm wavelength is for transmitting. Both of top mirror and bottom mirror of the VCSEL are constituted by cavity-in DBRs.

The feasibility of the proposed integrated chip depends on this new kind of cavity-in DBR structure. Since the integrated chip is designed for a transceiver, compared with the function of detecting optical signals, the laser function is more critical and essential to realize. The cavity-in DBRs constitute the resonant cavity of the VCSEL, and therefore if the VCSEL could lase, it illustrates the cavity-in DBR structure is feasible and then the integrated chip can be realized. Since ignoring the material losses in high-doping DBR in simulation results in the low Q value of the VCSEL's resonant cavity of as-grown wafer, the originally designed top-emitting VCSEL fails to work. To improve the Q value of the VCSEL's resonant cavity, a gold reflector is sputtered on the top mirror, and the VCSEL is finally successful to lase from bottom. Even though the VCSEL with a gold reflector emits from bottom not top, the results also can illustrate that the proposed cavity-in DBR structure is reasonable and practical, and the integrated chip is feasible and can be realized completely.

In this paper, the structure of the proposed integrated chip will be depicted at first, and then the fabrication process of the chip with a gold reflector will be described. We give an analysis on the Q value of VCSEL without and with a gold reflector by simulation. The difference of the Q values provides the reason of the VCSEL performance's change from failure to success. Finally, the characteristic of the VCSEL with a gold reflector is given in detail.

II. STRUCTURE OF INTEGRATED CHIP

The integrated chip structure composed of VCSEL and PIN-PD was grown on a (100) GaAs substrate by Metal-Organic Chemical Vapor Deposition (MOCVD). The PIN-PD consists of three layers of p-$Al_{0.2}Ga_{0.8}As$, i-GaAs and n-$Al_{0.2}Ga_{0.8}As$. Above the PD, the bottom mirror of the VCSEL is a cavity-in DBR, consisting of 25 pairs of $Al_{0.15}Ga_{0.85}As$/-$Al_{0.9}Ga_{0.1}As$ with an n-type doping concentration of 2×10^{18} cm^{-3} and a central wavelength of 850 nm, in a low-Q cavity with its resonant wavelength of 805 nm. The low-Q cavity is constituted by two three pairs of AlGaAs DBRs with it central wavelength of 805 nm. There are 3 pairs of 8 nm/10 nm thick GaAs/$Al_{0.3}Ga_{0.7}As$ quantum wells (QWs) in the active region to emit 850 nm light. On the two sides of the QWs, $Al_{0.3}Ga_{0.7}As$ layers with different thickness are used as cladding layers. The QWs and the cladding layers constitute the cavity with 1.5 λ of cavity length, in which λ is the central resonant wavelength of 850 nm. Above this region, a 30 nm thickness of $Al_{0.96}Ga_{0.04}As$ is deposited which will be used to form the current confinement aperture with wet oxidation process. Then 21.5 pairs of 4×10^{18} cm^{-3} p-type doped $Al_{0.15}Ga_{0.85}As$/$Al_{0.9}Ga_{0.1}As$ DBR are grown as the top mirror, which is also a cavity-in DBR. It consists of 17 pairs of $Al_{0.15}Ga_{0.85}As$/$Al_{0.9}Ga_{0.1}As$

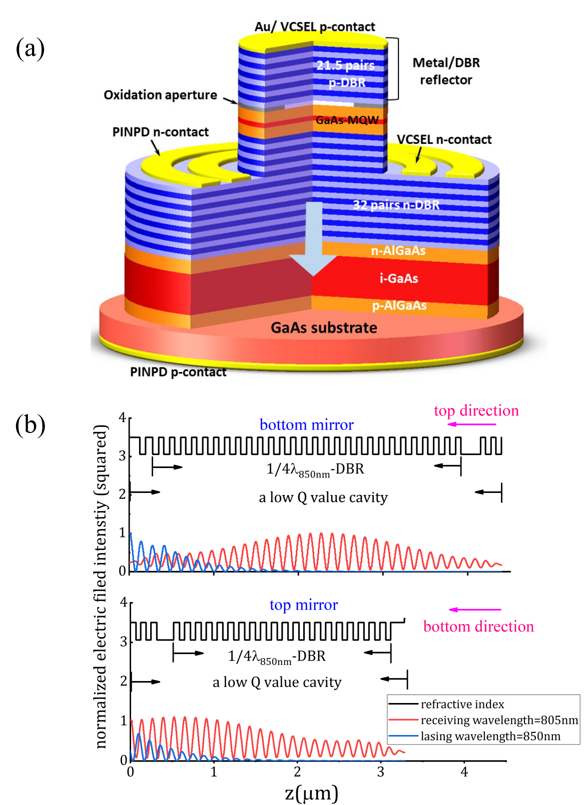

FIGURE 1. **(a) Schematic layout of the integrated chip structure composed of VCSEL and PIN-PD with a gold reflector; (b) Normalized electric filed intensity (squared) of 850nm (blue lines) and 805nm (red lines)wavelength distributed in bottom mirror and top mirror, respectively; refractive index profiles are shown in black lines.**

with a central wavelength of 850 nm, in a low-Q cavity with its resonant wavelength of 805 nm. The low-Q cavity is constituted by a three pairs of AlGaAs DBR with it central wavelength of 805 nm and the semiconductor/air interface. In Fig. 1b, the light power distribution of lasing wavelength of 850 nm and receiving wavelength of 805 nm in bottom mirror and top mirror, respectively, is shown. Almost all the light of 850 nm is reflected by DBRs, but most of the incident light of 805 nm penetrates the DBRs.

The integrated chip with a gold reflector is fabricated as following. Firstly, a 2000 Å thickness of Au metal layer is sputtered on the patterned epitaxial wafer, forming the metal reflector as well as VCSEL's top mirror. The SiN_x layers are deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and patterned as the mask to define the PD mesa and VCSEL mesa. The mesa is dry etched with Inductively Coupled Plasma (ICP) etching machine. The remained SiN_x layer is used as a protection mask of wet oxidation process. The 30 nm-thick $Al_{0.96}Ga_{0.04}$ As layer is then wet oxidized at 350 ° to realize optical and electrical confinement with an 18 μm-diameter aperture. Polyimide (PI) is used to fill the etched groove, and then it is patterned and etched to form the windows for n-contact electrodes of VCSEL and PD. Both of the n-contact electrodes of VCSEL and PD are sputtered on the same mesa plane. Finally, the GaAs substrate is thinned

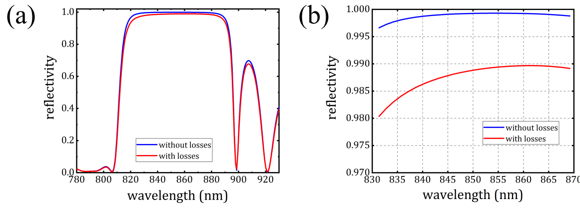

FIGURE 2. Simulation reflectance spectrums of the bottom mirror without losses (blue solid line) and with an absorption coefficient $\alpha = 100\ cm^{-1}$ (red solid line).

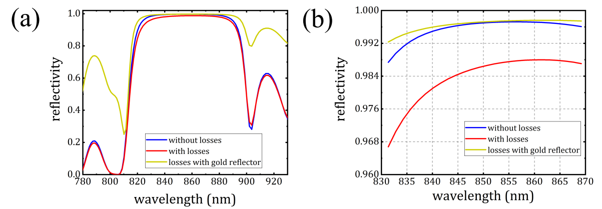

FIGURE 3. Simulation reflectance spectrums of the top mirror without losses (blue solid line), with an absorption coefficient $\alpha = 200\ cm^{-1}$ (red solid line) and with a gold reflector (yellow solid line).

and then the p-contact electrode of PIN-PD is evaporated. The schematic layout of the finished chip with a gold reflector is shown in Fig .1. The diameter of the VCSEL mesa is 24 μm and that of the PIN-PD mesa is 60 μm.

However, the VCSEL of as-grown wafer fails lasing. After consideration, there are some reasons for this result. The reflectance spectrums of the top mirror and bottom mirror are shown in Figs. 2a and 3a. Since the reflectivity is as low as 0% at the range of the receiving wavelength of 780∼810 nm, it pulls down the reflectivity around the lasing wavelength of 850 nm to some extent. So compared with the 1/4 λ thick of DBR with the same number layers, the reflectivity of the cavity-in DBR structure of the integrated chip is actually a little lower. Besides, the doping-induced losses in DBR are omitted in the design simulation, and the reflectivity of DBR in reality is lower than that of DBR in simulation. To find out the difference exactly, we make a theoretical analysis on the reflectivity of the top mirror and bottom mirror and the cavity quality factor Q of the VCSEL. Considering n-type and p-type doping-induced losses in AlGaAs DBR of VCSEL, we simulated the reflectance spectrum of the mirrors with adding the absorption coefficients of the DBR layers [16]. For n-type doping concentration of $2\times10^{18}\ cm^{-3}$, the absorption coefficient in simulation is set as $100\ cm^{-1}$, and for p-type doping concentration of $4\times10^{18}\ cm^{-3}$, this absorption coefficient is $200\ cm^{-1}$. The blue lines in Figs. 2-3 describe the reflectance spectrums of top mirror and bottom mirror without adding losses, while red line describe the spectrums of mirrors with adding losses. Both of the spectrums around 805 nm wavelength of receiving optical signal give a low reflectivity, but around 850 nm wavelength of transmitting optical signal give a high reflectivity. Without losses, the reflectivity of top mirror and bottom mirror is 99.71% and 99.93%, respectively. However, adding losses in DBR, which means the grown DBR in reality, results in a decrease of the reflectivity to 98.68% and 98.89%. Therefore, the difference of the reflectivity between the DBR in simulation and that in reality is 1.03% and 1.04%. According to the formula of the cavity quality factor Q shown in (1), we obtained the Q value of the VCSEL optical resonance cavity of being about 2738, with an effective cavity refractive index of 3.53 [17].

$$Q = \frac{2nL_c}{\lambda}\frac{\pi}{1-\sqrt{R_1R_2}} \quad (1)$$

where L_c is the length of the cavity, λ is the wavelength of light in vacuum, n is the effective refractive index of the layers, and R_1 and R_2 is the reflectivity of the top mirror and bottom mirror, respectively.

To improve the Q value of the optical cavity, a gold reflector is sputtered on the top mirror. With this reflector on the p-doped DBR, the reflectivity of the top mirror clearly increases from 98.68% to 99.73%, shown in the yellow line of Fig. 3a. And the Q value increases from 2738 to 4851 and it is about 1.8 times than that of the original cavity.

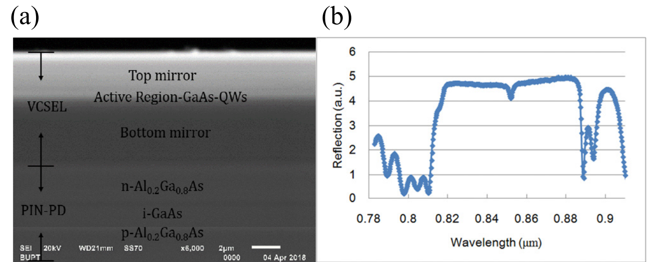

FIGURE 4. (a) As-grown wafer of the proposed integrated chip; (b) Reflection spectrum of as-grown wafer by MOCVD.

III. EXPERIMENTS AND RESULTS

The as-grown wafer and its reflectance spectrum are shown in Fig. 4, and it illustrates that the resonance peak of the cavity is located around 852 nm.

Since a gold reflector is sputtered on the top mirror, the characteristic of the VCSEL can not be measured directly. So we use the integrated PIN-PD to measure the output light of the VCSEL. The emitting light from VCSEL is detected by PIN-PD and be converted to photocurrents. Fig. 4 shows that the test schematic diagram to measure the performance of the fabricated VCSEL. The finished wafer is fixed on the probe station. A microscope is used to screen good chips with less defects and locate the probes to the VCSEL and PD electrodes. Then the selected device is current injected for VCSEL lasing and the VCSEL's light is detected by the integrated PIN-PD.

Since the location of VCSEL's bottom electrode and PIN-PD's top electrode is at the same plane, we make an extra testing experiment to make sure that the leakage current from VCSEL to PIN-PD and the dark current of PIN-PD itself are excluded. The VCSEL is shortened, and then the current of PIN-PD as the injected current increases is tested, as shown in Fig. 6a. After the calibration of the PIN-PD, we obtained the relationship between the net photocurrent of the PIN-PD

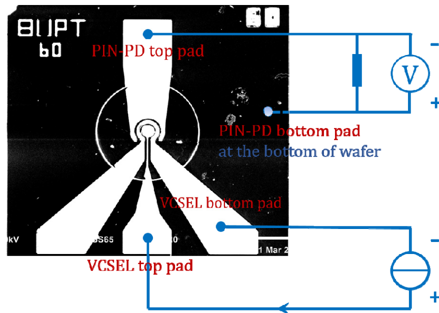

FIGURE 5. Test schematic diagram of the VCSEL's performance using PIN-PD integrated with it; Note that the PIN-PD's bottom electrode is at the bottom of the wafer and both of bottom electrode of VCSEL and top electrode of PIN-PD are ground electrode.

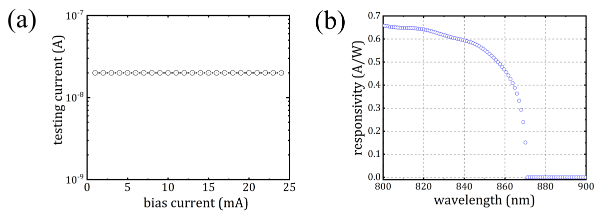

FIGURE 6. (a) Leakage current from VCSEL to PIN-PD and the dark current of the PIN-PD; (b)Simulation responsivity of PIN-PD by using Silvaco TCAD Atlas.

and the drive current of the VCSEL as shown in Figs. 7a-7b. We convert the photocurrent $I_{photocurrent}$ to light power P_{light} according to (2).

$$P_{light} = I_{photocurrent}/R \tag{2}$$

where R is the responsivity of PIN-PD. In the calculation, its value is about 0.55 A/W, which accounts for an absorption quantum efficiency (AQE) of 78.0% at 852 nm demonstrated by Dupuis N, shown in Fig. 6b [18]. Therefore, we can obtain the estimated L-I-V (Light power-Current-Voltage) characteristic, shown in Figs. 7c-7d.

In Figs. 7b and 7d, it is clearly shown that the threshold current is 3 mA. At the beginning of the lasing part, the light power is relatively low which is caused by the transverse mode competition. Besides, the location of the metal as well as contact is off-center. Therefore, the whole wafer is not well performed as designed. At start, the injected current distribution is dispersive, and so there are several modes to obtain gain simultaneously. At the current of 3 mA, only the gain of the fundamental mode gets to the threshold value, and then this mode emits. But unfortunately, the gain is so small that the emitted light power is much low. Meanwhile, none of the high-order transverse modes get to emit yet. Before the high-order modes begin to emit, there are some fluctuations that illustrate the transverse mode competition. At the location of the 13 mA current, several transverse modes get to threshold gain at the same time that result in a big step. There are several factors to cause the serious transverse modes competition phenomenon. One is the non-uniformity of the current injection due to the off-centered metal, and one

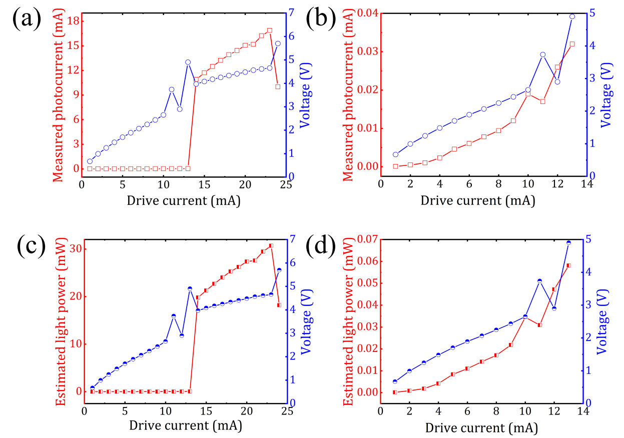

FIGURE 7. Measured photocurrent from PIN-PD (red curve) and voltage (blue curve) of VCSEL versus drive current at a range of (a) 0-24 mA and (b) 0-13 mA at the room temperature and CW lasing condition. The light power (red curve) transferred from photocurrent and voltage (blue curve) versus current (L-I-V) characteristics at a range of (c) 0-24 mA and (d) 0-13 mA, respectively.

is the large and non-uniform oxidation aperture. Expect for these two factors, the multi-cavity effect caused by cavity-in DBR may aggravate the mode competition. However, based on the simulation results of the VCSEL in the integrated chip, there is no jump in L-I-V curves theoretically. Moreover, the composite-resonator vertical-cavity lasers, which also have multiple-cavity effect, perform similarly with general VCSELs, so it illustrates that the jump phenomenon can be completely eliminated [19]–[21]. Therefore, we think that by reducing the oxidation aperture radius [22] and optimizing the fabrication, the jump may disappear. After this, transverse modes get to stable output, where the slope efficiency is 0.84 W/A. The estimated maximum output power is as high as 30 mW.

IV. CONCULSION

In conclusion, the feasibility of the proposed integrated chip has been demonstrated by the experiment of its laser part of VCSEL. The success of the integrated chip mainly depends on the new kind of cavity-in DBR structure. Meanwhile, the cavity-in DBRs constitute the resonant cavity of the VCSEL. However, the Q value of the VCSEL's resonant cavity of as-grown wafer is low, but with a gold reflector on top of the integrated chip to improve the Q value the VCSEL is successful to lase. This experiment result has demonstrated that the cavity-in DBR structure is reasonable and practical and thus the integrated chip can be realized definitely. Next, the cavity-in DBR will continue to be optimized to improve the Q value of the VCSEL's resonant cavity and make the VCSEL emit from top so that the integrated chip pairs can be applicable to the single-fiber bi-directional optical interconnects.

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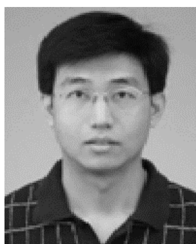

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