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Investigations on Driver and Layout for Paralleled GaN HEMTs in Low Voltage Application

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ABSTRACT Gallium nitride is becoming more popular in low-voltage applications. Gallium nitride (GaN) high electron mobility transistors (HEMTs) has positive temperature feature. It makes parallel application feasible for GaN HEMTs. Meanwhile, paralleled GaN HEMTs will increase the power handling capability and the efficiency of the converter. The parasitic parameters of both driving and power loop layout are critical which need to be equalized and minimized in GaN HEMT parallel operation. The parameters mismatch of the parallel branch will lead to significant effect on the dynamic characteristics and bring thermal problem of the GaN HEMTs. This paper focuses on the design of paralleled low-voltage enhancement GaN HEMT, and evaluates the effect of the parasitic inductances in both driver and power loops. The LT-spice and ANASYS Q3D Extractor simulation are carried out to analysis the effect of the unbalance parameters. The design guidelines for driver and PCB design are summarized as well. Finally, a 300W isolated DC-DC converter is built to verify the analysis and simulation on parallel operation.

INDEX TERMS Solar energy, parasitic parameters, paralleling, enhancement, DC-DC converter, driver design, low-voltage GaN HEMT.

I. INTRODUCTION

The newly wide bandgap (WBG) semiconductors, especially Gallium Nitride (GaN) high electron mobility transistors (HEMTs), have more potentials to feature with higher operating frequency, lower on-state resistance and higher temperature capability compared with Si device [1]–[4]. GaN HEMTs provide the possibility to reduce conduction loss and switching loss drastically, improve the capability of higher temperature and increase switching frequency, especially in low-voltage application [5]–[7].

The most conventional category of GaN HEMTs is enhancement mode (E-mode) and depletion mode (D-mode) according to the physical structure [8], [9]. Due to current production process limitation, GaN HEMTs with high current ratings are not yet available. The current rate of low-voltage E-mode GaN HEMTs is about 40A for the 200V devices, greatly limiting the popularization and application of GaN HEMTs [10]. Fortunately, the GaN HEMTs have positive temperature behavior of on-state resistance (R_{ds_on}), which makes parallel application feasible [11], [12]. Meanwhile, paralleling of GaN HEMTs will increase the current handling capability and decrease the conduction loss of the converter.

There are two main challenges in paralleled high-speed WBG, the potential uneven circuit layout and the imbalance of the devices [13]–[15]. On the one hand, the current sharing characteristics of paralleled GaN HEMTs are greatly influenced by R_{ds_on} and V_{th} [16]. Unequal R_{ds_on} will result in different steady-state currents, while different V_{th} will lead to unbalanced transient currents. On the other hand, uneven or asymmetrical circuit layout will lead to different parameters of both power loop and driving loop. Two major influencing factors of ringing are identified and optimized design for half bridge circuit is carried out in [17]. In [18], the effects of common source inductance and the Miller capacitance are considered to avoid the ringing of the GaN driving circuit.

A number of researches on paralleled SiC and GaN HEMTs are properly proposed and implemented in power electronics converters [19]–[22]. The dynamic behavior and the unbalance of parallel connected SiC MOSFETs have been discussed in [20] and [21]. However, these parallel operation methods could not be directly applied in the GaN HEMTs

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parallel applications, because the GaN HEMTs have lower driving voltage and lower gate threshold voltage (V_{th}). There are many studies on high voltage GaN HEMTs in paralleled application, but few on low voltage GaN HEMTs [23]–[26]. In [23], a half-bridge double pulse circuit is demonstrated and the four paralleled GaN HEMTs (650V/60A) realized hard switching transition. In [26], a buck converter with low-voltage GaN HEMTs in parallel connection is prototyped. Switching speed and on-resistance should be balanced in the parallel application. In [27], a three-level driving method for synchronous rectifiers based on low voltage GaN is proposed. And it will increase the efficiency of the LLC resonant converter.

In our work, we focused on the design of low voltage enhancement GaN HEMTs in parallel connection, and evaluated the effect of the parasitic inductances in both power and driving loops, especially the unbalancing of the paralleled branch. We design two low-voltage enhancement GaN HEMTs (EPC2010) in parallel implementations in the microinverter to achieve the power level. This paper is organized as follows. In Section II, the characterization of low-voltage enhancement GaN HEMTs and the modeling of the driving circuit are briefly reviewed. Further, the impact of parasitic parameters is analyzed. In Section III, The LT-Spice and ANASYS Q3D Extractor simulation are carried out to analysis the parasitic inductances influence in the unsymmetrical parallel branches. The design guidelines for PCB design are summarized as well. Further, a 300 W PV microinverter with paralleled GaN HEMTs is built to validate the feasibility and effectiveness of the analysis. Finally, the conclusion of the paper is given.

II. CHARACTERISTIC AND MODEL OF ENHANCEMENT GAN HEMTS

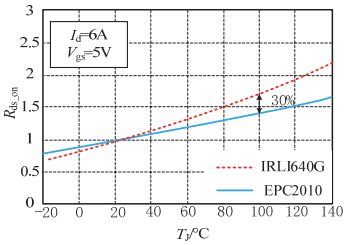
A. CHARACTERISTIC OF ENHANCEMENT GaN HEMTS

The GaN HEMTs have more potentials to feature with lower conduction impedance, better reverse recovery characteristics, and lower switching loss compared with Si devices. The comparison between Si MOSFET and GaN HEMTs is shown in Tab. 1. The safety threshold for the drive voltage of GaN HEMTs is only 1V. Because the voltage value to achieve full conduction is 5V, while the maximum allowable driving voltage is 6V. In addition, the parasitic parameters of the driving circuit can further result in voltage overshoot, which may lead to overvoltage. it is important to consider the effect of the parasitic parameters in the driving circuit.

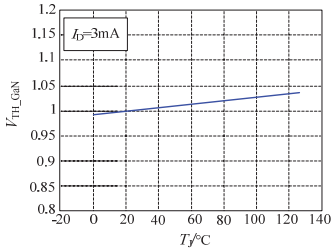
The influence of temperature on the on-state impedance is a most critical factor in determining whether GaN HEMTs are suitable for paralleling application. The R_{ds_on} vs. junction temperature T_J for the enhancement GaN HEMTs is shown in Fig.1(a). The test condition is that the driving voltage V_{gs} is 5V and the drain current I_d is 6A. The entire operation temperature range is considered from 0°C to 130°C. It can be seen that the R_{ds_on} of enhancement GaN HEMTs has a positive temperature characteristic, which is similar to the

TABLE 1. Key parameters of GaN HEMTs and Si M.

Symbol	Quantity	EPC2010	IRLI640G
V_{ds}	Drain to source voltage	200 V	200 V
I_d	Continuous current	12 A	10 A
R_{ds_on}	On resistance	25 mΩ	180 mΩ
V_{gs}	Gate to source voltage	-5V to 6V	±10 V
V_{th}	Gate threshold voltage	1.4V	2V
C_{iss}	Input capacitance	480 pF	1800 pF
C_{oss}	Output capacitance	270 pF	400 pF
C_{rss}	Reverse transfer capacitance	9.2 pF	120 pF
Q_{rr}	Source to drain recovery charge	0 uC	4.8 uC



(a) R_{ds_on} vs. T_J

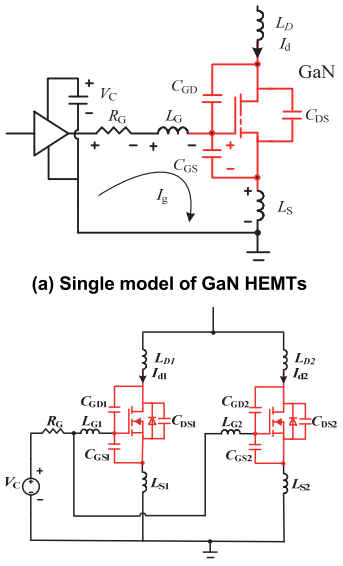


(b) V_{th} VS. T_J

FIGURE 1. Enhancement GaN HEMTs EPC2010 normalized parameters VS junction temperature.

Si MOSFET. The on-state impedance value increases as the junction temperature increases. The R_{ds_on} of IRLI640 is seven times that of EPC2010. This means that under the same conditions, the conduction loss of GaN HEMT will be much lower than that of Si MOSFET. Therefore, the positive temperature characteristics facilitate the use of GaN HEMTs in parallel.

The threshold voltage of the enhancement GaN HEMTs is only 1.4V, so a small difference will make the turn on and off time of the paralleling GaN HEMTs inconsistently. The influence of temperature on the threshold voltage is another key factor in parallel application of GaN HEMTs. Fig.1(b) shows the normalized threshold voltage V_{th} VS. T_J of the GaN HEMTs, and the temperature range is still from 0°C to 130°C. The V_{th} of enhancement GaN HEMTs also has a positive temperature coefficient. When the threshold voltages of paralleling devices are not consistent, the GaN HEMTs with lower threshold voltage will turn on and sustain all the dynamic current for a short time. Furtherer, the threshold voltage will increase as the junction temperature increases,



(a) Single model of GaN HEMTs

(b) Paralleling model of GaN HEMTs

FIGURE 2. Equivalent model of the enhancement GaN HEMTs.

and finally the threshold voltage of paralleling devices will be equal. Then, the parallel devices will be turned on at the same time. It can be concluded that the enhancement GaN HEMTs is suitable for parallel applications for the positive temperature coefficient of the threshold voltage.

B. EQIVALENT MODEL OF GaN HEMTS

The single equivalent model of the enhancement GaN HEMTs is shown in Fig.2(a). Parasitic parameters including parasitic inductance and capacitance are considered in the model. R_G is the gate resistance, L_G represents the gate inductance, L_D and L_S represent the drain inductance and the common source inductance respectively. C_{GD}, C_{DS} and C_{GD} represent gate-drain capacitance, drain-source capacitance, and gate-drain capacitance respectively. I_d and I_g are the drain-source current and gate current of the GaN HEMTs respectively. V_C is the voltage of the gate driver.

The model of paralleling GaN HEMTs is shown in Fig. 2(b). Parasitic inductance and capacitance are also considered in the model. L_{D1} and L_{D2} are the drain inductance, L_{G1} and L_{G2} represent the gate inductance, L_{S1} and L_{S2} are the common source inductance, R_G is the gate resistance.

C. THE INFLUENCES OF PARASITIC INDUCTANCE IMBALANCE

The voltage generated by L_S and L_G will feedback effect on the gate voltage V_{gs} during the transient switching process. The channel current increase gradually since V_{GS} reaches V_{th}, and the turn on process can be explained as follow.

$$V_{GS} = V_C - V_{L_G} - i_g R_g - V_{L_S} \tag{1}$$

$$I_g = \frac{V_C - V_{GS} - V_{L_G} - V_{L_S}}{R_G} \tag{2}$$

$$i_{d1} - i_{d2} = L_{S2}\frac{di_{S2}}{dt} - L_{S1}\frac{di_{S1}}{dt} \tag{3}$$

The completely turn on time will increase for the influence of L_S and L_G. Consequently, the GaN HEMTs with smaller parasitic inductance turns on faster and carries more current in the parallel application. Similarly, the turn off process is also affected by L_S and L_G, as shown in equation (4) and (5). The GaN HEMTs with smaller Ls turn off earlier and carries less current. What's more, the transient switching process will become slower.

$$V_{GS} = V_{L_G} + i_G R_g + V_{L_S} \tag{4}$$

$$I_g = \frac{-V_{GS} + V_{L_G} + V_{L_S}}{R_G} = \frac{-V_{GS} + \frac{di_d}{dt}(L_G + L_S)}{R_G} \tag{5}$$

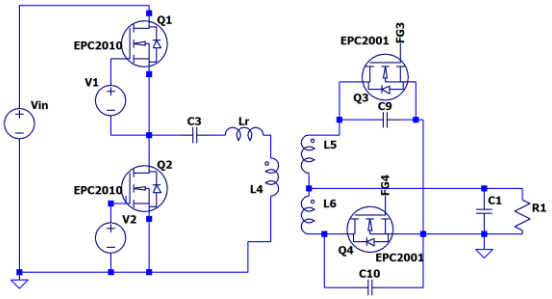
III. SIMULATION AND EXPERIMENTAL VERIFICATIONS

A. PARASITIC INDUCTANCE SENSITIVITY SIMULATION OF THE DRIVER CIRCUIT

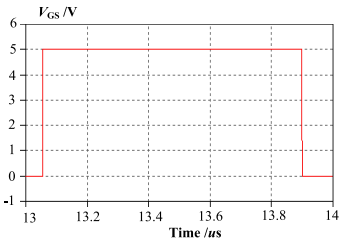
Firstly, the simulations of the influence of parasitic parameters on the drive circuit are carried out, as shown in Fig.3. The LT-Spice based EPC2010 model provided by the manufacture is used in all the following simulations. The wiring diagram based on LT-Spice using in this simulation is shown in Fig.3 (a). The simulation conditions are that the input voltage is 25V, the input current is 8A, the output voltage is 45Vand the switching frequency is 500kHz and the gate resistance is zero. The load type is pure resistive in this simulation. The switching frequency and the gate resistance remain unchanged, but the inductance is changed. The L_S and L_G are both zero in Fig.3(b), L_G equals 200pH and L_S is 5nH in Fig.3(c), and L_G equals to 500pH and L_S is 5nH in Fig.3(d).

The variation of gate-to-source voltage is shown in Fig.3. As we can see, the transient switching process is about 2ns when there are no parasitic parameters in Fig.3(b). While, the time of the transient switching process increase with the increase of parasitic parameters. The time of turn on is about 26ns, the time of turn off is about 43ns in Fig.3(c). The transient switching process becomes slower and the gate voltage waveforms appear oscillation. The peak value of the gate voltage increases significantly, as shown in Fig.3(c) and Fig.3(d). When the L_G is more than 10nH, the overshoot of the gate voltage will exceed the threshold voltage. Simulation results of the effect of L_S and L_G on switching losses of Q_1 is shown in Fig.4 (e). The test condition is same as the simulation above. Therefore, the actual circuit should minimize the parasitic inductance L_G of the drive circuit. The parasitic inductance L_G and L_S are critical and sensitive to the operation of the GaN HEMTs. Therefore, the actual circuit should minimize the parasitic inductance.

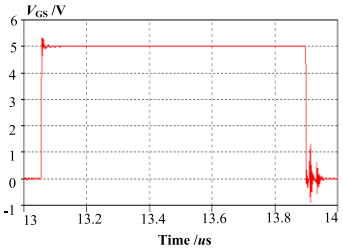
Further, the influence of $R_{G\_}$ is also considered and the simulation results are shown in Fig.4. In the simulation, the L_G and L_S are 3nH and 200pH respectively. The simulation conditions of Fig.4 are the same as Fig.3. The switching frequency is 500kHz and the load type is also pure resistive in this simulation. It can be seen that the overshoot of V_{gs} is significantly reduced with the increase of the drive resistance. When the drive resistance is greater than 2 ohms, the drive voltage has no oscillation and its turn-on speed is about 30 ns.



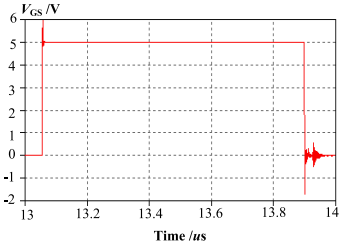
(a) wiring diagram based on LT-Spice



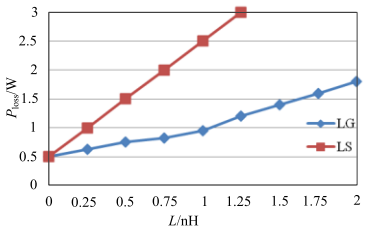
(b) L_S=0nH, L_G=0pH



(c) L_S=5nH, L_G=200pH



(d) L_S=5nH, L_G=500pH

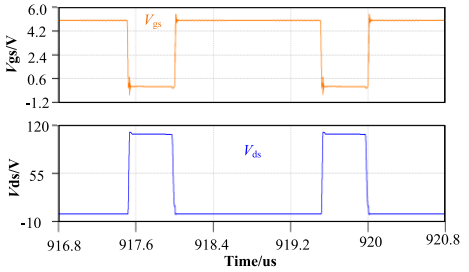


(e) *The effect of L_S and L_G on switching losses*

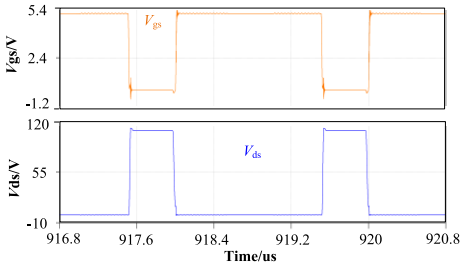
FIGURE 3. Simulation of parasitic inductance influence on the driver circuit.

B. PARALLEL SIMULATION BASED ON GaN HEMTS

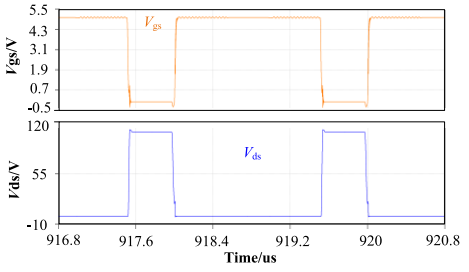
To address the impact of the parasitic inductance imbalance in parallel application, the simulated source currents I_{S1} and I_{S2} waveforms of the paralleled GaN HEMTs are shown in Fig.5. The wiring diagram based on LT-Spice using in this simulation is shown in Fig.5 (a). The simulation conditions are that



(a) R_G=1Ω



(b) R_G =2Ω



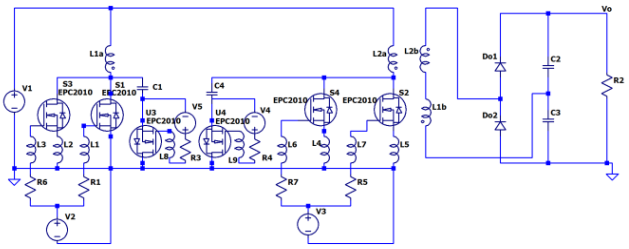
(c) R_G =5Ω

FIGURE 4. Waveforms of EPC2010 with different R_G.

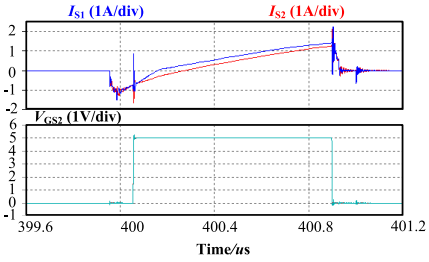
the input voltage is 25V, the output voltage is 380V, the input current is 8A, and the switching frequency is 100kHz, the load type is pure resistive in this simulation. The paralleled devices have different L_S. According to the simulation results, the imbalance of the L_S will impact the currents of the paralleled GaN HEMTs. For the case of the 2nH mismatch of the L_S, the sharing currents of the paralleled devices will be 13% difference, as shown in Fig.5(a). And, the currents will differ by 30% if the difference of L_S is 4nH, as shown in Fig.5(b). In addition, there will be current oscillations between the paralleled GaN HEMTs.

C. EXPERIMENTS BASED ON LM5114

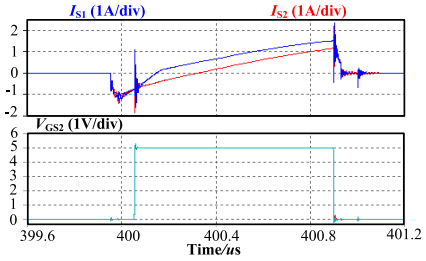
To further prove effectiveness of the simulation results, the drive circuit based on LM5114 is designed, which is shown in Fig.6. The driving circuit schematic of LM5114 is shown in Fig.6(a), and the PCB layout based on LM5114 is shown in Fig.6(b). The experimental results with 200kHz, 400kHz and 500kHz are given in Fig.7, Fig.8 and Fig.9, respectively. The experimental condition is that turn on resistance is 5.1Ω, the turn off resistance is 1.8Ω, and the input voltage is 40V. At 200kHz, the performance of drain-source



(a) wiring diagram based on LT-Spice

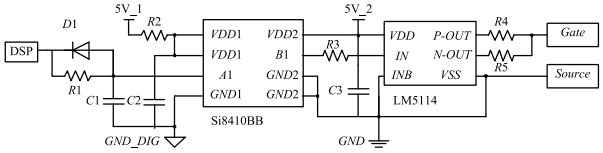


(b) L_{S1}=1nH, L_{S2}=3nH, $R_{G\_}$ =1Ω L_G=200pH

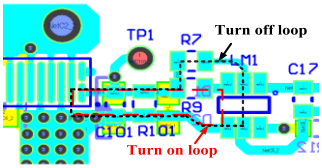


(c) L_{S1}=1nH, L_{S2}=5nH, $R_{G\_}$ =1Ω L_G=200pH

FIGURE 5. Parallel simulation results based on GaN HEMTs.



(a) Driving circuit schematic of LM5114



(b) PCB layout based on LM5114

FIGURE 6. The driving diagram and two-layer PCB layout based on LM5114.

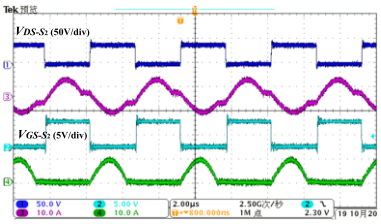


FIGURE 7. Experimental results based on LM5114 at 200kHz.

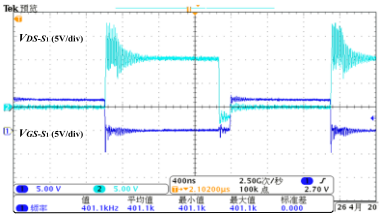
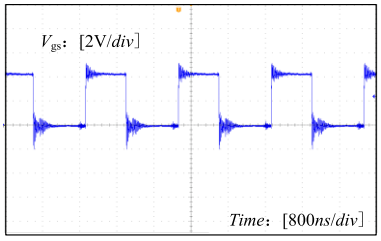
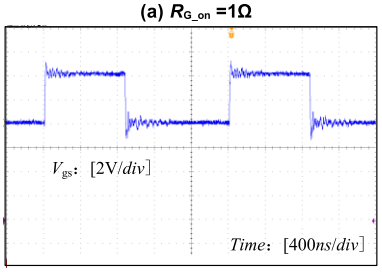


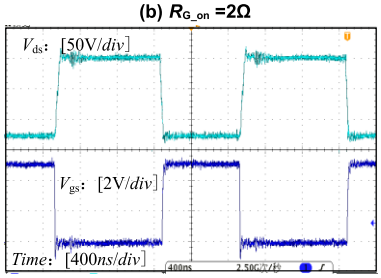
FIGURE 8. Experimental results based on LM5114 at 400kHz.



(a) R_{G_on} =1Ω



(b) R_{G_on} =2Ω



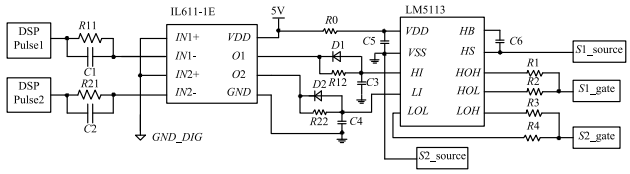
(c) R_{G_on}=5Ω

FIGURE 9. Experimental results based on LM5114 with different R_{G_on}.

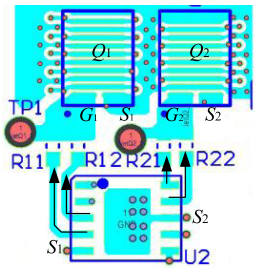
voltage V_{DS} is good and the gate voltage V_{GS} is within the maximum gate-source voltage 6V, as shown in Fig.7.

In order to achieve meaningful experimental results, the experiments at 400kHz are also given, as Fig.8. Compared with previous experimental results, it can be seen the V_{DS} and V_{GS} oscillate significantly at 400kHz. The parasitic inductance has obvious influence on the circuit performance as the switching frequency increases. The parasitic inductance L_S is 7nH with Q3D Extractor.

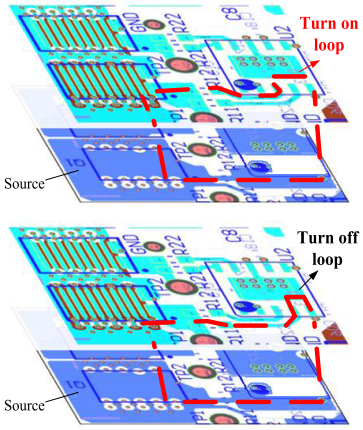
To further verify the impact of the drive resistance, experiments with different turn on registers are carried out at 500 kHz, shown in Fig.9. As the drive resistance increases, the overshoot of the gate voltage decreases. The experimental results are the same as the simulation results, which proves



(a) Driving circuit schematic of LM5113



(b) PCB layout based on LM5113



(c) Drive loop of the design

FIGURE 10. Optimization drive circuit based on LM5113.

the correctness of the simulation analysis. However, if the L_S is greater than 10nH, the oscillation will not be suppressed and the gate voltage will exceed 6V. This may easily lead to device failure.

D. EXPERIMENTS BASED ON LM5113

In order to improve the performance of paralleled GaN HEMTs in high switching frequency, we adopt the driver chip LM5113 and optimize the layout design as shown in Fig.10. The driving circuit schematic of LM5113 is shown in Fig.10(a), and the PCB layout based on LM5114 is shown in Fig.10(b). What's more, the driving loop of the circuit is shown in Fig.10(c). The parasitic inductance L_G and L_S are further reduced comparing with the layout based on LM5114. The area of the driving loop is only the product of the length of the single-layer driving circuit and the thickness of the PCB board, which greatly reduces the area of the driving circuit. As a result, the parasitic inductance parameters are reduced. The simulation results of Q3D Extractor show that the parasitic inductance of the drive circuit decreases to only 2nH after optimization.

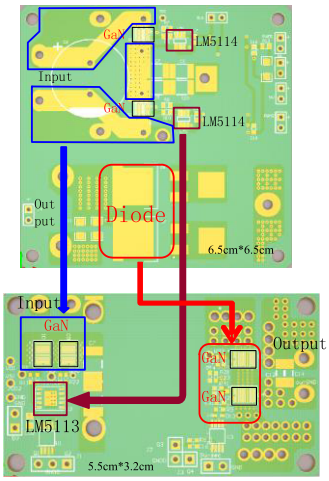


FIGURE 11. Optimization design of the PCB.

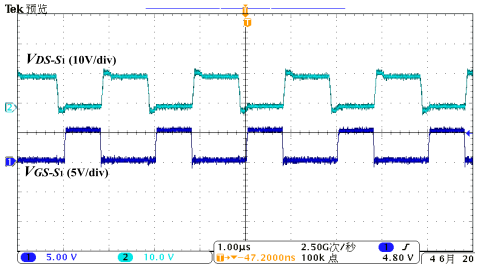
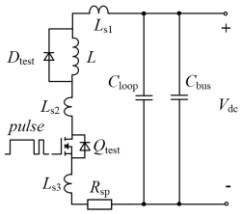


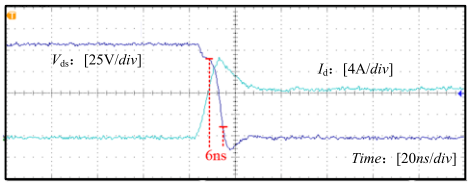
FIGURE 12. Experimental results based on LM5113 at 500kHz.

The PCB layouts are optimized base on the PCB design guideline in [28]. The PCB layouts before and after optimization are shown in Fig.11. The second version of the PCB base on LM5114 is a two-layer board with a length and width of 6.5 cm; the second version of the PCB base on LM5113 is a four-layer board with a length and width of 5.5 cm and 3.2 cm, respectively. It can be seen that the layout of the first version has larger loop area and larger parasitic parameters. A ground plane is added to the PCB based on LM5113 to reduce the loop area of the drive loop. At the same time, the package of components in the driver circuit are also changed from 0603 package to the 0402 package. The drive loop area is further reduced. The parasitic parameters are significantly reduced after optimization. The experimental results at 500kHz based on LM5113 is shown in Fig.12. To make the comparison fairly, other experimental conditions are consistent with the previous ones. It can be clearly seen that the stability of V_{GS} and V_{DS} is significantly improved after optimization and waveforms have almost no oscillation. The anti-interference ability of the circuit increases as the parasitic parameters decrease.

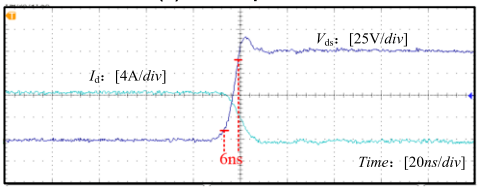
We tested the switching characteristics of EPC2010 based on the double pulse circuit, which is shown in Fig.13. The test conditions are that the input voltage is 25V, the drive resistance is 1Ω, the drain current is 8A, and the switching



(a) Double pulse circuit



(b) turn on process



(c) turn off process

FIGURE 13. Experimental results based on double pulse circuit.

TABLE 2. Simulation parasitic values of Epc2010 with Q3D extractor.

Parameter	DCR/mΩ	DCL/nH	ACR/mΩ	ACL/nH
Loop of $Q_{7\text{-}1}$	8.72	54.27	3.4	37.2
Loop of $Q_{7\text{-}2}$	10.05	54.26	3.5	37.5
Loop of $Q_{8\text{-}1}$	10.34	77.15	4.4	57.5
Loop of $Q_{8\text{-}2}$	11.25	78.37	4.5	58.6

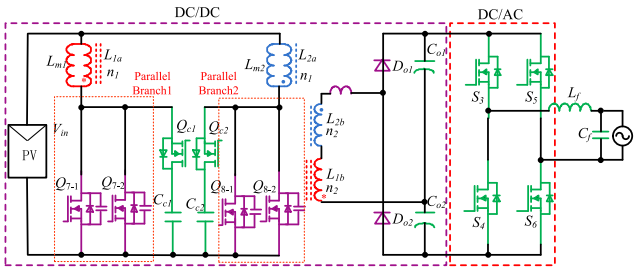
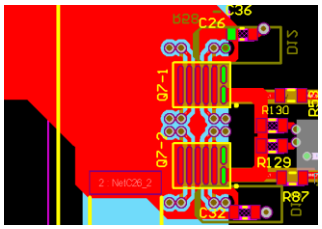


FIGURE 14. The topology of microinverter circuit based on GaN HEMTs.

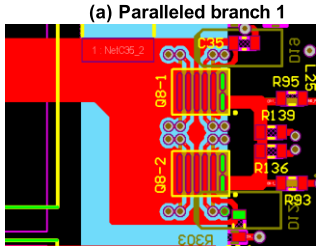
frequency is 500kHz. The driver chip is LM5113. During the turn on process, the current rise time is about12 ns, and the current change rate di/dt is about 3000 A/μs. The fall time of the drain-source voltage V_{ds} is about 6 ns, and the voltage change rate is about 16.7V/ns, as shown in Fig.13 (b). During the turn off process, the rise time of the drain-source voltage V_{ds} of EPC2010 is also about 6ns, as shown in Fig.13(c).

E. EXPERIMENTS BASED ON PARALLELED GaN HEMTS

The hardware setup of the 300W microinverter based on paralleled EPC2010 is evaluated. The paralleling circuit is shown in Fig.14. The main switches are working on hard switching condition, but active clamping circuit is added to reduce switching losses. The typical PCB layouts for the two

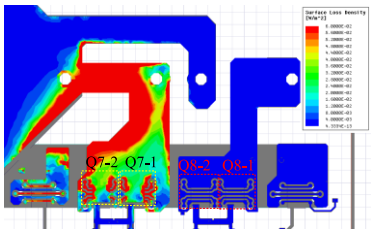


(a) Paralleled branch 1

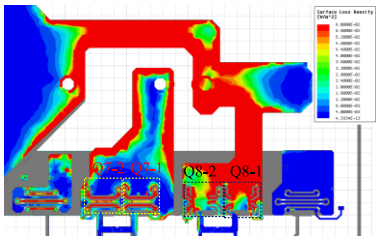


(b) Paralleled branch 2

FIGURE 15. 2-D view of two paralleled PCB branches.



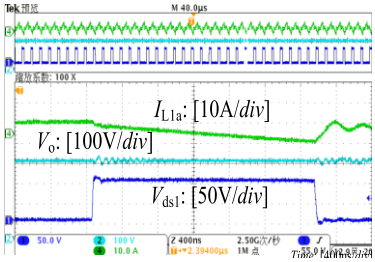
(a)Paralleled branch 1



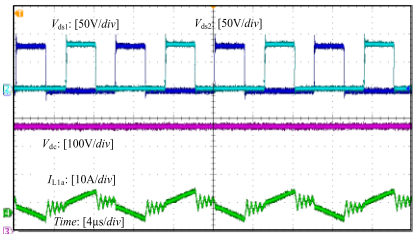
(b) Paralleled branch 2

FIGURE 16. FEM simulation of the two paralleled branches.

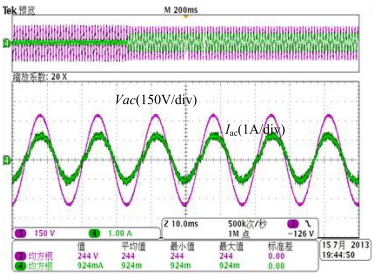
paralleled branches are shown in Fig. 15. The other loops of the circuit are symmetrical. However, the drain source's PCB width of the two branches are asymmetrical. Therefore, the asymmetrical layout of the parallel GaN HEMTs may cause unbalance of parasitic inductances. What's more, it will also cause thermal problems and effect the dynamic performance of the GaN HEMTs. In order to obtain parasitic inductances of the parallel branches, the FEM simulation of the PCB is implemented with ANSYS Q3D Extractor. The simulation results of the parasitic parameters of the four switch loops are shown in Table 2, where the two branches have different DCL and ACL. The asymmetry of branch 2 is stronger than branch1. In addition, the parasitic parameters of branch 2 is larger than branch 1. The surface loss density simulation results of the parallel branches are shown in Fig. 16, where loss density of Q_{8-1} is larger than Q_{8-2} and loss density of branch 2 is much larger than branch 1.



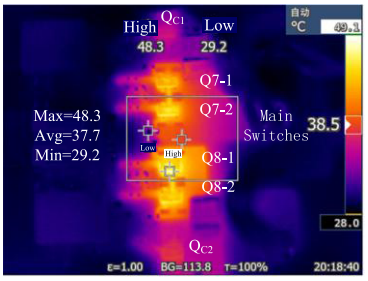
(a) DC/DC stage waveforms of the microinverter



(b) V_{ds}, V_{dc} and I_{L1a} of the DC/DC stage



(c) DC/AC stage waveforms of the microinverter



(d) Temperature result of paralleled GaN HEMTs

FIGURE 17. Experimental results of microinverter based on paralleled GaN HEMTs.

To further verify the correctness of the analysis and FEM simulations, experiments are carried out. The experimental conditions are that the input voltage is 25V, the output voltage is 380V, the input current is 8A, and the switching frequency is 100kHz, the load type is pure resistive in this simulation. The two stage experimental results of the microinverter is shown in Fig.17(a), Fig.17(b) and Fig.17(c). The power level of this test is 300W, the input and output voltage of the DC/DC stage are 25V and 380V, respectively. The grid voltage is 220V. The drain voltage V_{ds} of the main switches, the inductors current I_{L1} and the DC voltage V_{dc} is shown in Fig.17(b). The temperature test result at room temperature is shown in Fig.17(d). As we can see that the temperature of Q_{8-1} and Q_{8-2} are higher than Q_{7-1} and Q_{7-2}, which caused by the parasitic inductance difference of the branches. The greater ACL and DCL difference of the paralleled GaN HEMTs, the higher of the temperature. Therefore, the PCB layout should be as symmetrical as possible and the ACL and DCL difference of the paralleled GaN HEMTs should not exceed 20%. The greater the difference in parasitic parameters of the parallel branches, the greater the influence on the current sharing.

IV. CONCLUSION

This paper focuses on the design of paralleled low-voltage enhancement GaN HEMTs, and evaluates the effect of the parasitic inductances in both driver and power loops. The LT-spice and ANASYS Q3D Extractor simulation are carried out to analysis the effect of the unbalance parameters. Further, a 300W PV microinverter with paralleled GaN HEMTs is built to validate the feasibility and effectiveness of the analysis. Close observation indicates that the main contributions over the conference paper includes:

(1) The parasitic inductance of the driver side should not exceed 5nH when the frequency is up to 500kHz. Otherwise, the drive overvoltage will occur.

(2) The loops of the circuit should be as symmetrical as possible.

(3) The ACL and DCL difference of the paralleled GaN HEMTs should not exceed 20%.

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