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A Three-Level Dual-Active-Bridge Converter With Blocking Capacitors for Bidirectional Electric Vehicle Charger

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ABSTRACT In order to solve the considerable issues of air pollution, climate warming and fossil energy shortage, many governments around the world have formulated policies to encourage the development of electric vehicles over the past decade. This paper proposes a three-level dual-active-bridge (DAB) converter with blocking capacitors for bidirectional electric vehicle charger. In the proposed three-level DAB converter, two blocking capacitors are placed in series with the two windings of the transformer, respectively. Both of the two three-level bridges can operate in four modes, and generate square waves with four kinds of amplitude. Therefore, the proposed three-level DAB converter can adapt to the wide voltage range of electric vehicle. A working mode selection algorithm is developed to minimize the transformer RMS current of the three-level DAB converter. The optimal working mode can be selected in real time according to the voltage ratio and the active power. Finally, experimental results are presented to verify the feasibility and the advantage of the proposed three-level DAB converter.

INDEX TERMS Asymmetric, blocking capacitor, dual-active-bridge, three-level.

I. INTRODUCTION

Air pollution, global warming, and incremental energy cost are considerable issues of the present world. All these challenging concerns are directly linked to heavily utilize fossil fuels. Researchers all around the world spend a lot of time and energy to reduce the reliance on the fossil fuels and replace them with clean solutions [1]–[4]. Electric vehicle (EV) is a kind of green transportation with lesser emissions and better fuel economy, and has the potential to replace traditional fuel vehicles in the future [5]–[7].

In order to popularize EVs, a convenient, high-efficiency and high-power charging infrastructure is indispensable. Charger systems are classified into off-board and on-board types with unidirectional or bidirectional power flow. Bidirectional charging enables the vehicle-to-grid (V2G) capability, allowing EVs to inject energy into the grid. With the bidirectional charging system, EV can play a role of peak shaving and valley filling for a power grid and even provide electric energy for emergency backup during a power outage [8]–[12]. Fig.1 shows a general bidirectional EV charger, which is often composed of a bidirectional Power Factor Control (PFC) rectifier, and a bidirectional isolated DC-DC converter. This paper mainly studies the bidirectional isolated DC-DC converter. In order to make it applicable to different types of battery, the output voltage should be wide enough. Usually, the charging voltage is 200V to 500V for light-duty vehicles, and 400V to 750V for heavy-duty vehicles. For 3-phase AC grid connecting system, the DC bus voltage of the EV charger is usually as high as 750V.

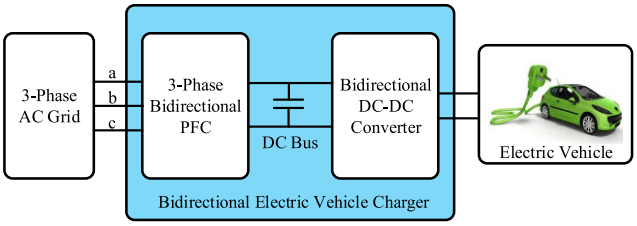

FIGURE 1. A diagram of a general bidirectional EV charger.

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Si-based MOSFETs in this voltage level have large on-resistance and output capacitance, which leads to large conduction loss and switching loss. IGBT can meet this voltage level, but it reduces the switching frequency and the power density due to the trailing current effect. Therefore, the traditional silicon-based power semiconductors are not suitable for this application. The SiC-based MOSFET is an excellent candidate because of lower on-resistance, higher withstand voltage, lower switching loss and better thermal characteristics compared with Si devices. An in-depth and comprehensive analysis of a SiC devices based bidirectional EV charger was reported in [13]. Nevertheless, the cost of SiC MOSFET is very high until now. Therefore, to meet high DC bus voltage with low cost, it is necessary to develop an improved topology. In [14], a bidirectional input series output parallel (ISOP) EV charger was presented. However, the EV charger cannot meet the requirement of heavy-duty vehicles because the output voltage is below 500V. An alternative approach to reduce the voltage stress of power devices is to apply the three-level structure to the conventional bidirectional isolated DC-DC topology. Three-level bidirectional isolated DC-DC converters have been reported by some researchers [15]–[25]. Literature [15] studied the modulation strategy of the neutral point clamped (NPC) dual-active-bridge (DAB) converter to minimize the loss. In [16], a control algorithm was developed to ensure that the voltage stress of each switch is half of the port voltage, and the detailed operation principle of the three-level DAB converter with DPS control was presented. The soft switching range of the three-level DAB converter was analyzed and expanded in [17]–[19]. Literature [20], [21] investigated the characteristics of the three-level three-phase DAB converter. Nevertheless, none of the bidirectional three-level DC-DC converters mentioned above have an enough wide output voltage range for electric vehicles.

Considering the above mentioned problem, this paper proposes a three-level DAB converter with blocking capacitors for bidirectional EV charger. The main contribution of the paper lies in 3 points:

(1) A novel three-level DAB converter is proposed by placing two blocking capacitors in series with the two windings of isolation transformer, respectively. By combining the working modes of the two three-level bridges, the ''voltage-match'' can be achieved in many cases. Therefore, the conversion efficiency of the proposed three-level DAB converter is improved over a wide output voltage range.

(2) An optimal mode selection algorithm is proposed based on the minimum transformer RMS current. With this algorithm, the optimal working mode can be selected in real time according to the voltage ratio and the active power.

(3) A prototype was built to verify the feasibility of the three-level DAB converter with blocking capacitors. The experimental results proved that the proposed converter can operate as we expect, and the efficiency of the proposed converter changes little (<5%) over a wide output voltage range.

This paper is organized as follows. In Section II, the three-level DAB converter with blocking capacitors is proposed. In Section III, the working mode selection algorithm is introduced in detail. In Section IV, some guidelines about selection of the blocking capacitors are presented. Experimental results obtained from a 3.5kW prototype are described in Section V. Finally, Section VI provides the conclusion.

II. PROPOSED THREE-LEVEL DAB CONVERTER

A. THREE-LEVEL DAB CONVERTER WITH BLOCKING CAPACITORS

The proposed three-level DAB converter with blocking capacitors is shown in Fig. 2. It consists of two three-level full bridges, an intermediate frequency transformer, an auxiliary inductor, and two blocking capacitors. L represents the sum of the auxiliary inductance and the transformer leakage inductance. n is the transformer turns ratio. C_{b1} and C_{b2} are two blocking capacitors which are used to offset the DC component produced by the two three-level full bridges. In actual use, the V_2 DC port is connected to EV, the voltage of which varies over a wide range, such as 200V to 750V. The V_1 DC port is connected to the output port of a PFC rectifier, which usually keeps a constant voltage.

Compared with the SiC-based two-level DAB converter, the three-level structure of the proposed converter increases hardware complexity and reduces reliability. Nevertheless, this disadvantage can be overcome by optimizing component selection and PCB design. In terms of cost, the proposed converter has a great advantage because the price of SiC-based MOSFET is very high.

B. THE WORKING MODES OF THE THREE-LEVEL FULL BRIDGES

Unlike the conventional three-level DAB converter, the two three-level full bridges of the proposed converter may generate voltage waveforms with nonzero mean value. Taking as an example the primary full bridge, the blocking capacitor C_{b1} is used to offset the DC component of v_{AB}. Obviously, the average voltage of the capacitor C_{b1} is equal to the mean value of v_{AB} in steady state. In practical use, the voltage fluctuation of the capacitor is usually negligible because the capacitance is large enough. Therefore, we assume that the capacitor voltage is constant in the steady state.

For convenience of discussion, all diodes and switches are considered ideal devices. In steady state, the DC-link capacitors, and the flying capacitors, have the same voltage, 0.5 V_1. The three-level leg can operate in four switching states, as shown in Table 1 and Fig.3. For instance, the positive voltage level could be achieved by turning on S1 and S2 and turning off S3 and S4. If the voltage of the flying capacitor C_5 is lower than that of the DC-link capacitor C_1, the capacitor C_1 will charge the capacitor C_5 via the switch S_1 and the diode D_2, as Fig.3 (b) shows. Otherwise, the diode

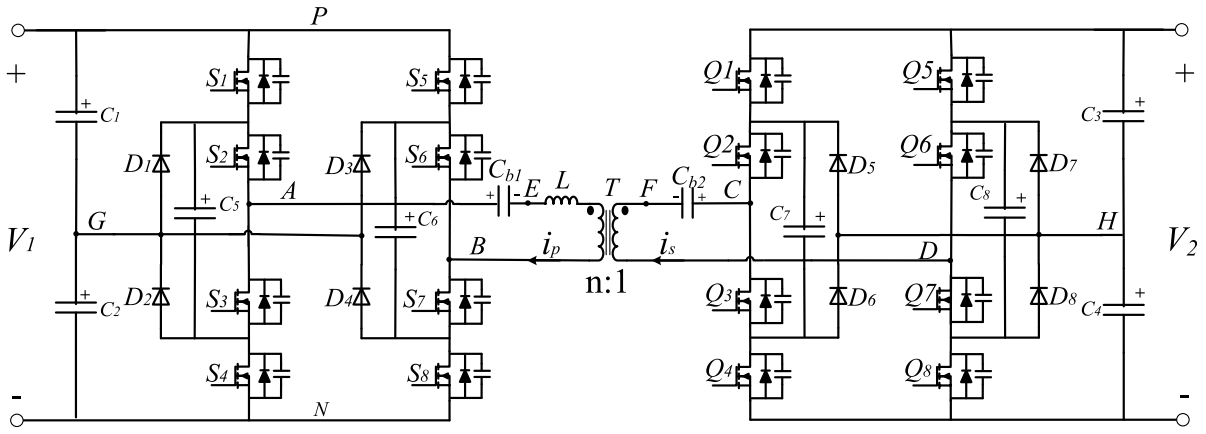

FIGURE 2. The three-level DAB converter with blocking capacitors.

TABLE 1. Switching states of a three-level leg.

State	S1	S2	S3	S4	v_{AG}
P	On	On	Off	Off	$0.5V_1$
O_1	On	Off	On	Off	0
O_2	Off	On	Off	On	0
N	Off	Off	On	On	$-0.5V_1$

D_1 is off, and the voltage of C_5 remain unchanged, as Fig.3 (a) illustrates. For the other three switching states, there are also two cases.

For State P and State N, the output current i_p has no effect on the voltage of the flying capacitor C_5. For State O_1 and State O_2, i_p has different effects on the voltage of the flying capacitor. For example, if i_p is positive, C_5 will be charged in State O_1 and discharged in State O_2. Therefore, the two zero-level switching states should be selected alternately in order to keep the flying capacitor voltage equal to $0.5V_1$.

Through freedom combinations of the two three-level legs, there are 16 possible switching states for the three-level full bridge. As Fig.4 presents, by selecting appropriate switching states, the three-level full bridge can operate in four working modes. The blocking capacitor voltage v_{Cb1} is equal to 0 in Mode A and Mode C, and equal to $0.25V_1$ in Mode B and Mode D. v_{EB} is the difference between v_{AB} and v_{Cb1}. As a consequence, v_{EB} is a symmetric square wave with the amplitude equal to V_1, $0.75V_1$, $0.5V_1$ and $0.25V_1$. Fig.4 shows the details clearly.

Just like other three-level flying-capacitor converters, it is necessary to control the flying capacitor voltage. The deviation of the flying capacitor is harm to the converter performance in some aspects. It increases the voltage stress of the switches, which may cause permanent damage. Furthermore, the deviation will disturb the transformer current and lead to significant increase of circulating power. Therefore, the two zero-level switching states, O_1 and O_2, are used in turn in order to keep the flying capacitor voltage equal to $0.5V_1$, as shown in Fig.4.

C. PHASE SHIFT MODULATION

With the method described in Part B, two symmetric square waves, v_{EB} and v_{FD} can be generated by the two three-level full bridges. Similar to the conventional DAB converter, phase shift modulation (PSM) is applied to the three-level DAB converter with blocking capacitors, as Fig.5 shows. v'_{FD} is the primary-referred voltage of v_{FD}. The phase-shift angle between the two bridges is used to control the power flow of the proposed three-level DAB converter. To facilitate the discussion below, we define the working mode of the three-level DAB converter is Mode x-y, where x is the working mode of the primary full bridge and y is that of the secondary full bridge.

Obviously, the optimal operating point occurs when the amplitude of v_{EB} is equal to that of $v'_{FD,}$, which is usually called ''voltage-match''. Low circulating power and theoretical full load ZVS for all the power switches can be achieved under the optimal operating point condition. For the sake of discussion, the voltage ratio, K, is defined as the follow equation.

$$K = \frac{nV_2}{V_1} \tag{1}$$

Because the amplitudes of v_{EB} and v'_{FD} both have four possible values, the ''voltage-match'' can be achieved in many cases. Fig.6 shows all ''voltage-match'' points and corresponding working modes. It can be observed that the ''voltage-match'' points range from 0.25 to 4. This means that the three-level DAB converter with blocking capacitors is suitable for wide output voltage range applications.

D. VOLTAGE CONTROL OF THE FLYING CAPACITORS AND THE DC-LINK CAPACITORS

When the converter operates, it is necessary to keep the voltages of flying capacitors (C_5 C_6 C_7 and C_8) and DC-link capacitors (C_1 C_2 C_3 and C_4) equal to half of the DC-link voltage. To achieve that, two zero-level switching states, O_1 and O_2, are used in turn. Since the operation principles of the two full bridges are identical, the balance principle of the

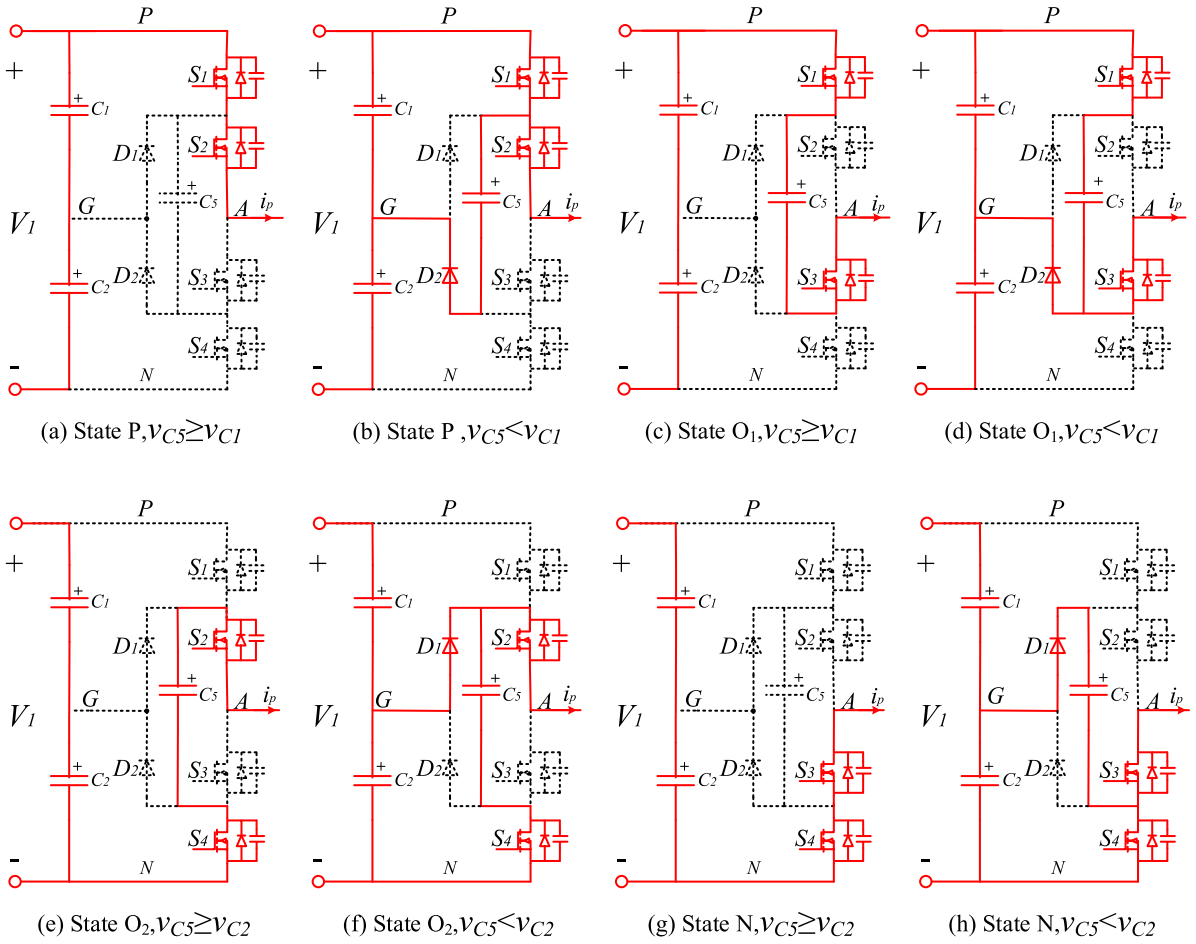

FIGURE 3. Four switching states of a three-level leg.

capacitance voltage will be discussed with the primary full bridge as an example. To facilitate the analysis of voltage balance principle, the two DC-link capacitors C_1 and C_2 are split into two three-level legs. As Fig. 7 shows, C_1 is split into C_{11} and C_{12}, and C_2 is split into C_{21} and C_{22}. Then, there are two DC-link capacitors and a flying capacitor in each three-level leg. According to the four working modes of the primary bridge described in Section II B, there are three kinds of switching sequence for each three-level leg.(a) Only positive-level and negative-level switching states, no zero-level switching state, such as P-N-P-N. (b) Combine positive-level switching state (or negative-level switching state) with zero-level switching states, such as P-O_1-P-O_2. (c) Only zero-level switching states, such as O_1-O_1-O_2-O_2. For these three cases, the principle of voltage balance will be analyzed in detail in the following paragraphs. To facilitate discussion and analysis, it is assumed that in two consecutive switching cycles, the waveforms of the primary transformer current i_p are identical.

When the switching sequence is P-N-P-N, the voltage waveforms of DC-link capacitors and flying capacitor are shown in Fig. 8. Since zero-level switching state is not included in the switching sequence, the output current of bridge i_p has no effect on the voltages of flying capacitor and DC-link capacitors. The voltages of the three capacitors are all equal to $0.5V_1$.

When the switching sequence is P-O_1-P-O_2, the voltage waveforms are shown in Fig. 9. During the time interval $[t_0, t_2]$, the switching state is P, i_p has no effect on flying capacitor voltage. Since the voltage of flying capacitor C_5 is higher than that of the DC-link capacitor C_{11}, C_{11} will not charge C_5. Therefore, the voltages of the three capacitors remain unchanged in this time interval. During the time interval $[t_2, t_\alpha]$, the switching state is O_1, i_p charges (or discharges) C_5 through S_1 and S_3. Since the voltage of C_5 is still higher than that of C_{11}, C_{11} will not charge C_5. Therefore, voltages of the two DC-link capacitors remain unchanged in this time interval. Beginning at t_α, the voltage of C_5 is lower than that of C_{11}, and C_{11} charges C_5 through diode D_2. Therefore, v_{C11} decreases and v_{C21} increases. During the time interval $[t_4, t_6]$, the switching state is P, i_p has no effect on the flying capacitor voltage. C_{11} continues charging C_5 until v_{C11} equals to v_{C5}. Then, the three capacitor voltages all remain unchanged. During the time interval $[t_6, t_8]$, the switching

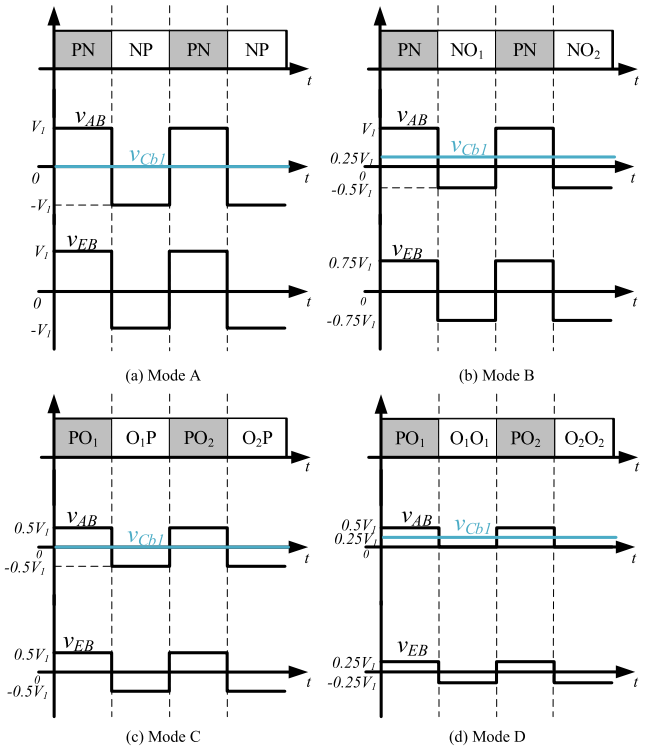

FIGURE 4. Four working modes of each three-level full bridge. v_{EB} is a symmetric square wave with the amplitude equal to V_1, $0.75V_1$, $0.5V_1$ and $0.25V_1$.

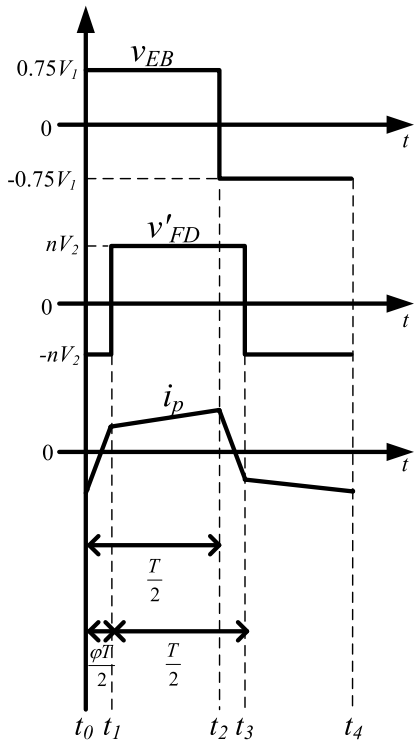

FIGURE 5. The main waveforms of the proposed three-level DAB converter in Mode B-A. The phase-shift angle between the two bridges is used to control the power flow of the converter.

state is O_2, i_p charges (or discharges) C_5 through S_2 and S_4. Meanwhile, because the voltage of C_5 is lower than that

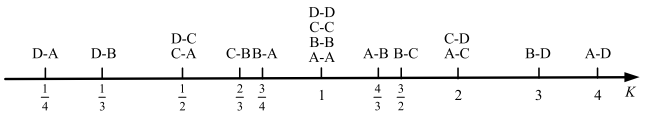

FIGURE 6. "Voltage-match" points and corresponding working modes for the three-level DAB converter with blocking capacitors.

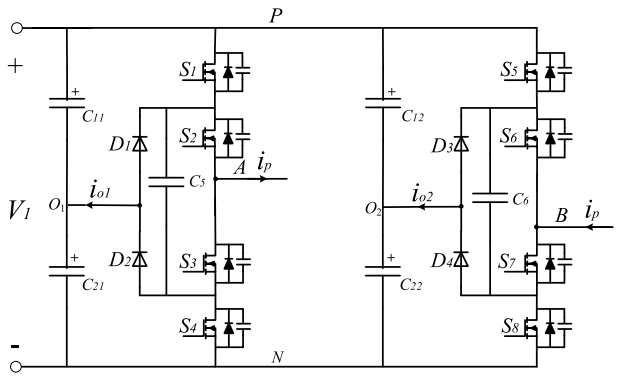

FIGURE 7. Two DC-link capacitors C_1 and C_2 are split into two three-level legs.

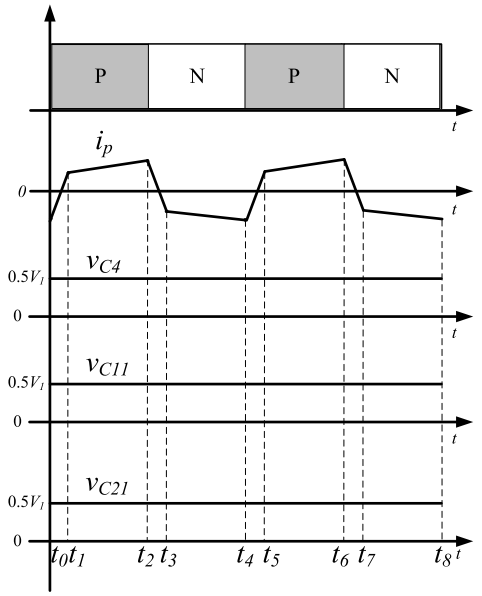

FIGURE 8. The voltage waveforms of the DC-link capacitors and the flying capacitor when the switching sequence is P-N-P-N.

of C_{21}, C_{21} charges C_5 through diode D_1. Therefore, v_{C12} decreases and v_{C11} increases. After the voltage of C_5 is higher than that of C_{21}, the two DC-link capacitors remain unchanged.

When the switching sequence is O_1-O_1-O_2-O_2, the voltage waveforms are shown in Fig. 10. During the time interval $[t_0, t_4]$, the switching state is O_1, i_p charges (or discharges) C_5 through S_1 and S_3. At the beginning and ending of this time interval, the voltage of C_5 is lower than that of C_{11}, and C_{11} charges C_5 through diode D_2. Therefore, v_{C11} decreases and v_{C21} increases. In the middle of the time interval, voltage of C_5 is higher than that of C_{11}, and the two DC-link capacitor voltages remain unchanged. During the

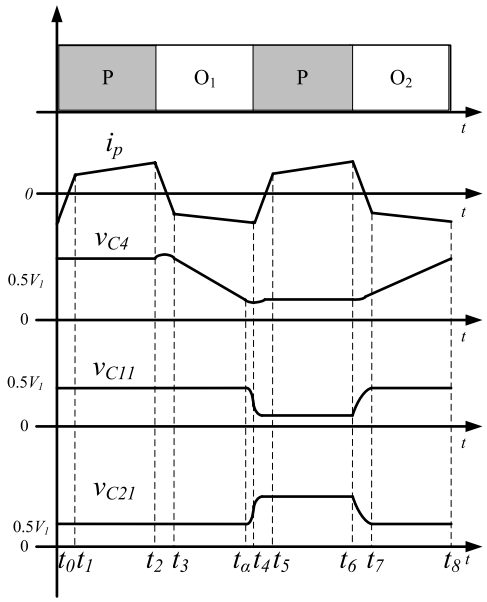

FIGURE 9. The voltage waveforms of the DC-link capacitors and the flying capacitor when the switching sequence is P-O_1 -P-O_2.

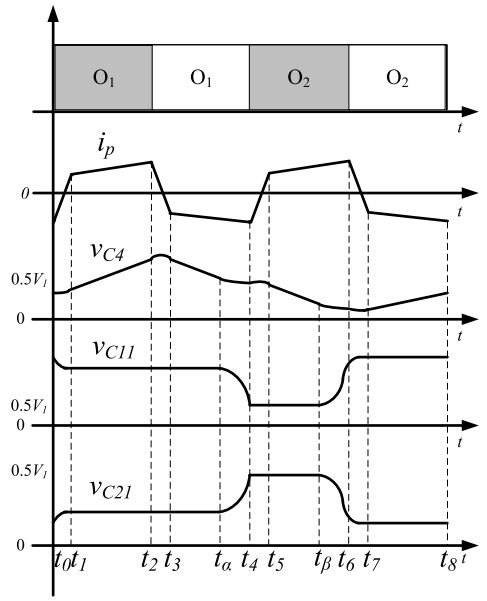

FIGURE 10. The voltage waveforms of the DC-link capacitors and the flying capacitor when the switching sequence is O_1-O_1-O_2-O_2.

time interval $[t_4, t_8]$, the switching state is O_2, i_p charges (or discharges) C_5 through S_2 and S_4. In the middle of the time interval, the voltage of C_5 is lower than that of C_{21}, and C_{21} charges C_5 through diode D_1. Therefore, v_{C21} decreases and v_{C11} increases. At the beginning and ending of this time interval, the two DC-link capacitor voltages remain unchanged.

To sum up, for these three switching sequences, the voltages of flying capacitor and two DC-link capacitors can be restored to the initial value after two switching cycles. Therefore, the voltages of two DC-link capacitors and two flying capacitors in the primary three-level bridge are balanced. For the same reason, the voltages of two DC-link capacitors and two flying capacitors in the secondary three-level bridge can also be controlled as $0.5V_2$.

III. SELECTION OF OPTIMAL WORKING MODE

There are 16 working modes for the three-level DAB converter with blocking capacitors. The conduction and copper losses generated in the converters are proportional to the square of the transformer RMS current [26]. Therefore, in order to decrease the loss, we choose the working mode which possesses the smallest transformer RMS current as the optimal working mode.

In the following paragraphs, we deduce the expressions of the primary transformer current i_p, the active power P and the RMS value of i_p, taking Mode B-A as an example.

Fig.5. shows the detailed current and voltage waveforms of Mode B-A, where T is the switching period and φ is the phase shift ratio. The differential equation to illustrate the dynamics of $i_{\mathrm{p}}(t)$ is

$$\begin{cases} L\dfrac{di_p(t)}{dt} = 0.75V_1 + nV_2 \quad (t_0 < t < t_1) \\ L\dfrac{di_p(t)}{dt} = 0.75V_1 - nV_2 \quad (t_1 < t < t_2). \end{cases} \tag{2}$$

Due to the symmetry of the switch sequence, the inductor current is also symmetrical.

$$i_p(t_0) = -i_p(t_2) \tag{3}$$

From (2) and (3), the inductor current can be represented as

$$i_p(t) = \begin{cases} \dfrac{0.75V_1 + nV_2}{L}(t - t_0) - \dfrac{(2nV_2\varphi - nV_2 + 0.75V_1)T}{4L} \\ \qquad (t_0 < t < t_1) \\ \dfrac{0.75V_1 - nV_2}{L}(t - t_3) + \dfrac{(2nV_2\varphi - nV_2 - 0.75V_1)T}{4L} \\ \qquad (t_1 < t < t_2). \end{cases} \tag{4}$$

Then the transmission power is calculated by averaging in half switching cycle.

$$P_{B-A} = \frac{1}{T/2}\int_{t_0}^{t_2} v_{EB}(t) i_p(t) dt = \frac{1.5V_1}{T}\int_{t_0}^{t_2} i_p(t) dt \tag{5}$$

Substituting (1), (4) into (5), we have

$$P_{B-A} = \frac{3nV_1V_2T}{8L}\varphi(1 - \varphi). \tag{6}$$

For the sake of discussion, the normalized power is defined as the following equation

$$P^*_{B-A} = \frac{P_{B-A}}{P_{base}} = 3\varphi(1 - \varphi), \tag{7}$$

where

$$P_{base} = \frac{nV_1V_2T}{8L}. \tag{8}$$

Obviously, P^*_{B-A} is a quadratic function of φ. P^*_{B-A} reaches the maximum value when φ is 0.5. We have

$$P^*_{B-A,\max} = \frac{3}{4} \tag{9}$$

TABLE 2. The values of k_x and k_y for different working modes.

Mode	k_x	k_y
A	1	1
B	0.75	0.75
C	0.5	0.5
D	0.25	0.25

With the same method, we obtain the P^* and $P^*_{\max}$ for the other modes, as the following equations

$$P^*_{x-y} = 4k_x k_y \varphi(1-\varphi), \tag{10}$$
$$P^*_{x-y,\max} = k_x k_y, \tag{11}$$

where k_x is the ratio of the amplitude of v_{EB} to V_1, and k_y is the ratio of the amplitude of v_{FD} to V_2. According to Section II B, the values of k_x and k_y are listed in Table 2.
The RMS value of i_p can be calculated by the following equation.

$$I_p^2 = \frac{1}{T/2}\int_{t_0}^{t_2} i_p^2(t)dt \tag{12}$$

Substituting (4) into (12), we have

$$I_p^2 = \frac{T^2}{48L^2}[-6nV_1V_2\varphi^3 + 9nV_1V_2\varphi^2 + (0.75V_1 - nV_2)^2]. \tag{13}$$

For the sake of discussion, the normalized square of I_P is defined as the following equation,

$$I_p^{2*} = \frac{I_p^2}{I_{base}^2} = \frac{1}{3}[-6\varphi^3 + 9\varphi^2 + \frac{(0.75-K)^2}{K}], \tag{14}$$

where

$$I_{base} = \frac{\sqrt{nV_1V_2}T}{4L}. \tag{15}$$

With the same method, we obtain the $I_p{}^*$ for the other working modes, as the following equation.

$$I^*_{p,x-y} = \sqrt{\frac{1}{3}[-8k_xk_y\varphi^3 + 12k_xk_y\varphi^2 + \frac{(k_x - k_yK)^2}{K}]} \tag{16}$$

Using equation (10), (11) and (16), the working mode which possesses the smallest transformer RMS current can be found out easily. The detailed algorithm is as follows.

Step 1: According to the actual working condition, figure out the normalized active power P^* and the voltage ratio, K.

Step 2: Comparing P^* with the max active power of each working mode (according to (11)), determine the set of feasible working modes, S.

$$S = \{(x,y)|P^* \le P^*_{x-y,\max}\} \tag{17}$$

Step 3: For each working mode in S, calculate the phase shift ratio φ, using (10)

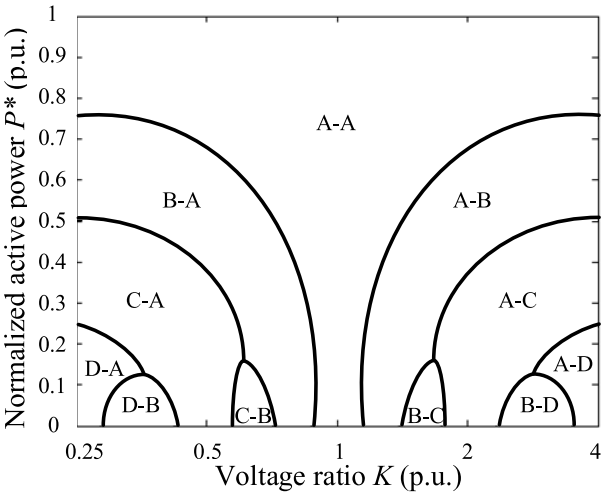

FIGURE 11. The result of the working mode selection for the proposed three-level DAB converter.

Step 4: For each working mode in S, figure out the normalized transformer current $I_p{}^*$, using (16) and φ obtained in Step 3.

Step 5: Find out the minimum of $I_p{}^*$, and determine the working mode which possesses the smallest transformer RMS current.

Fig.11 illustrates the result of the working mode selection. For ease of understanding, log coordinate is used for K axis. A total of 11 working modes appear in the result. The other five working modes are B-B, C-C, D-D, C-D and D-C. They are eliminated because of higher transformer RMS current. For example, the transformer RMS current of Mode B-B is always higher than that of Mode A-A. In practical application, a look-up table method can be used to reduce the computational load of the controller.

IV. SELECTION OF THE BLOCKING CAPACITORS

The blocking capacitors are important components of the proposed three-level DAB topology. To select appropriate blocking capacitors, the following three points should be considered. Since the operation principles of the two full bridges are identical, the selection of the blocking capacitors will be discussed with the primary full bridge as an example.

A) The rated voltage of the capacitor should be higher than $0.25V_1$, because the maximum of the capacitor voltage is $0.25V_1$. However, the capacitor voltage may be as high as V_1 if the drive signals of power devices are incorrect. Therefore, a capacitor with rated voltage higher than V_1 is suggested in the early stage of prototype development. After the correctness of the drive signals is validated, a capacitor with rated voltage higher than $0.25V_1$ can be used.

B) The capacitor is charged when i_P is positive and discharged when i_P is negative. The capacitance should be large enough to keep the capacitor voltage in a certain range, such as $0.05V_1$. Otherwise, the primary current

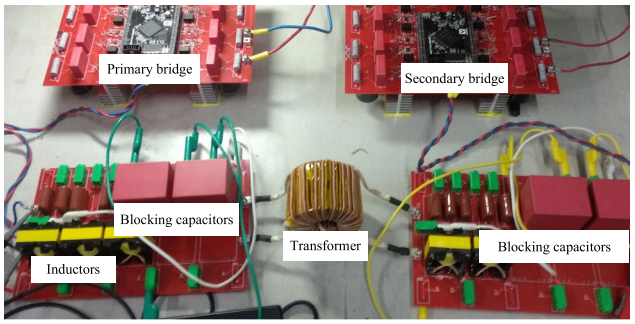

FIGURE 12. A 3.5kW prototype of the proposed three-level DAB converter with blocking capacitors.

waveform will no longer be piecewise linear, and the converter will not operate as we expect.

C) Electrolytic capacitor is not recommended. The equivalent series resistance will lead to a significant loss. What's more, negative voltage may destroy the electrolytic capacitor. Film capacitance and multilayer ceramic capacitor are recommended.

Obviously, the blocking capacitors lead to an increase in the volume of the circuit. However, compared with the power semiconductor devices (16 MOSFETs and 8 diodes), the additional blocking capacitors do not take up a lot of volume. The power density of the proposed converter is close to that of the traditional three-level DAB converter.

V. EXPERIMENT

A 3.5kW hardware prototype was built to validate the proposed converter. The input voltage is 750V DC. Output DC voltage is from 200V to 700V. The switching frequency is 50kHz. The transformer turns ratio is 5:3. The two blocking capacitors are 200μF. Fig. 12 is a photo of the hardware prototype. A DC power supply is connected to the V_1 DC port of the converter. A DC electronic load is connected to the V_2 DC port of the converter. The main waveforms were measured by a Tektronix Oscilloscope DPO4034.

A. THE EXPERIMENTAL VERIFICATION OF THE THREE-LEVEL DAB CONVERTER WITH BLOCKING CAPACITORS

Fig. 13 shows the four working modes of the primary full bridge in the three-level DAB converter. It is observed that v_{EB} had the same AC component as v_{AB}, and the DC component of v_{EB} was zero. This means that the blocking capacitor compensated the DC component of v_{AB} as we expect. As a result, v_{EB} was a symmetric square wave with the amplitude equal to V_1, $0.75V_1$, $0.5V_1$ and $0.25V_1$. The voltages of the flying capacitors of the primary three-level bridge are presented in Fig.14. It can be seen that the two flying-capacitor voltages were both close to $0.5V_1$, as we expected. The waveforms of the secondary bridge are similar to those of the primary bridge, and are not shown here.

When the output voltage V_2 varied from 200V to 700V, and the output current was set as 5A, the working mode selection

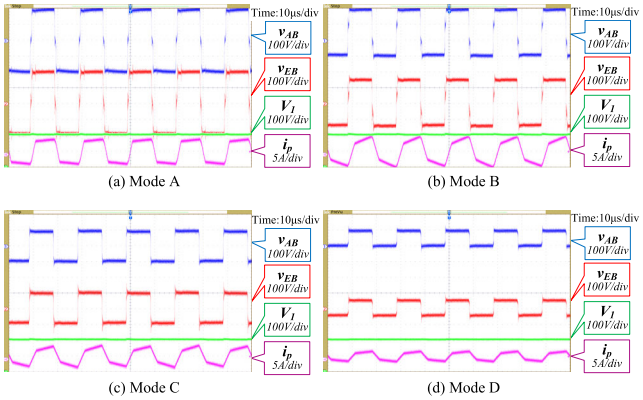

FIGURE 13. Four working modes of the primary bridge in the three-level DAB converter with blocking capacitors.

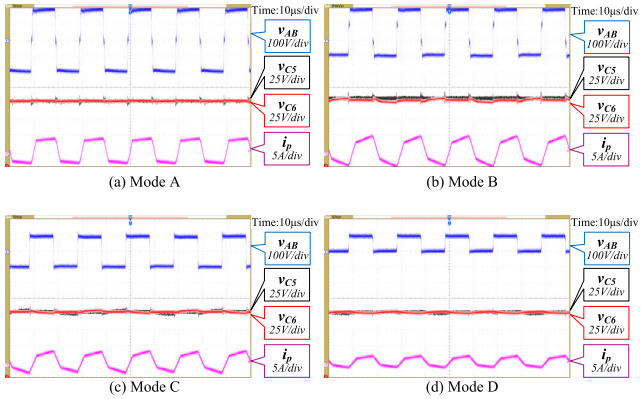

FIGURE 14. The voltage balance of the flying capacitors for the four working modes of the primary full bridge.

TABLE 3. Working mode selection results for the prototype when the output current is 5A.

V_2	200V	300V	400V	500V	600V	700V
Mode	C-A	B-A	A-A	A-A	A-B	A-B

results are shown in Table 3. Fig.15 illustrates the main waveforms of the three-level DAB converter with blocking capacitors. It is observed that the two three-level bridges generated bridge voltages as described in Section II, and the phase-shift modulation was applied to control the active power. All the waveforms above proved that the proposed three-level DAB converter with blocking capacitors can work steadily in a wide output voltage range as we expect.

B. THE EFFICIENCY OF THE PROPOSED CONVERTER

The efficiency of the proposed converter was measured by a WT3000 power analyzer. Fig.16 shows the results. The efficiency was always higher than 92.5%, and the difference between the maximum efficiency and the minimum efficiency was less than 5%, which means that the proposed converter is suitable for wide output voltage range applications.

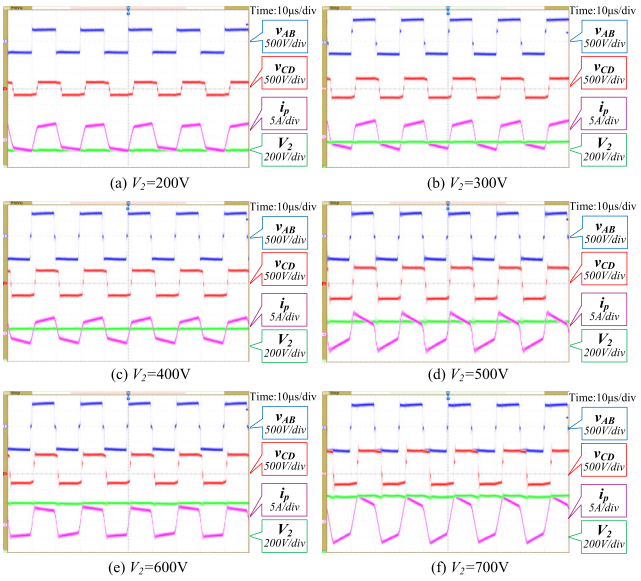

FIGURE 15. The main waveforms of the three-level DAB converter with blocking capacitors when the output voltage V_2 varied from 200V to 700V and the output current was set as 5A.

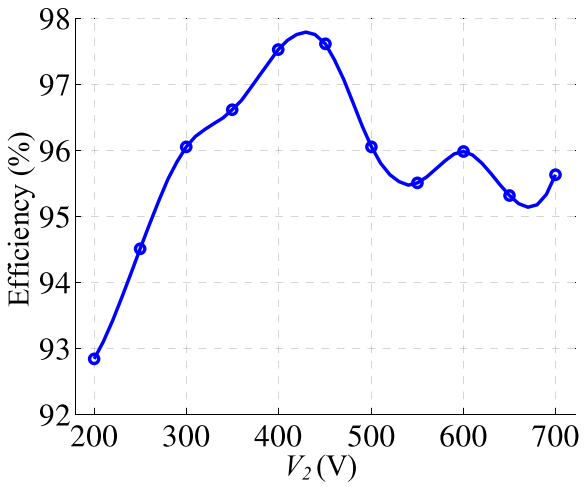

FIGURE 16. Experimental curves of efficiency with respect to V_2 for the three-level DAB converter with blocking capacitors when the output current was 5A.

VI. CONCLUSION

In this paper, a three-level DAB converter with blocking capacitors is proposed for bidirectional EV charger. By inserting a blocking capacitor in the primary loop and the secondary loop of the three-level DAB converter respectively, the proposed topology adapts to wide output voltage range applications. An optimal mode selection algorithm is proposed based on the minimum transformer RMS current. A 3.5W hardware prototype was built to validate the proposed converter. Experimental results show that the converter can operate stably in a wide output voltage range, and the efficiency of the proposed converter changes little (<5%) over a wide output voltage range. Moreover, the flying capacitor voltages of the converter are balanced well by selecting different switching states in different switching cycles.

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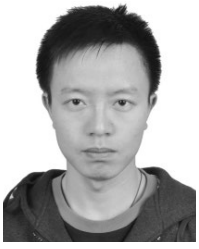

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