IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 7, 2019, accepted November 26, 2019, date of publication November 29, 2019,
date of current version December 13, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2956876

FPGA Implementation of Distance-Independent Symbol Timing Synchronization in IM/DD OFDM-PON

XIAOYI CHEN[1], MINGYI GAO[1], (Senior Member, IEEE), YANPING SHA[1], JI ZHANG[1], ERXI FANG[1], AND HONGLIANG REN[2]

[1]Suzhou Key Laboratory of Advanced Optical Communication Network Technology, School of Electronic and Information Engineering, Soochow University, Suzhou 215006, China
[2]College of Information Engineering, Zhejiang University of Technology, Hangzhou 310023, China

Corresponding author: Mingyi Gao (mygao@suda.edu.cn)

This work was supported in part by the Suzhou Industry Technological Innovation Project under Grant SYG201809, in part by the Priority Academic Program Development of Jiangsu Higher Education Institutions, in part by the Open Fund of the Institute of Information Photonics and Optical Communications (IPOC), Beijing University of Posts and Telecommunication (BUPT), under Grant 2017B001, in part by the National Natural Science Foundation of China Project under Grant 61307082, and in part by the Jiangsu Government Scholarship for Overseas Studies.

ABSTRACT Intensity modulation/direct detection (IM/DD) orthogonal frequency division multiplexing (OFDM) is very suitable for high-speed cost-sensitive passive optical network (PON) applications. However, real-time OFDM systems are sensitive to synchronization bias, and thus symbol timing synchronization (STS) becomes a critical issue. We proposed a proportional-sign cross-correlation (PS-CC) STS algorithm with the advantages of distance-independence and low resource utilization. In the proposed PS-CC STS algorithm, the sign operation is applied instead of the multiplication operation with high computational complexity to decrease the resource utilization and the characteristic of low resource utilization will drive its application in real-time systems. Meanwhile, we use field programmable gate array (FPGA) to design a baseband IM/DD OFDM receiver with pipeline structure and built a universal loop test system, which is applied to implement the proposed PS-CC STS algorithm and evaluate its performance. In the experiment of a 16-QAM OFDM-PON system, a 30-km fiber transmission only results in 1.98% ripple on the peak amplitude of correlation, which verifies the distance-independence of the proposed method.

INDEX TERMS Orthogonal frequency division multiplexing, symbol timing synchronization, field programmable gate array.

I. INTRODUCTION

To meet the rapid growth in bandwidth demand, passive optical network (PON) based on orthogonal frequency division multiplexing (OFDM) technology has attracted much attention. The OFDM-PONs have the advantages of high spectral efficiency, anti-dispersion and flexible resource allocation [1]. In the intensity modulation/direct detection (IM/DD)-OFDM systems, only one set of real signals is required for transmission, and the OFDM receiver does not need to recover the carrier. Therefore, only a few low-cost devices are needed in IM/DD-OFDM communication, which is very suitable for cost-sensitive PON applications with many optical network unit (ONU) nodes [2], [3]. However, the OFDM system is sensitive to the synchronization offset. Such a synchronization offset will lead to inter symbol interference (ISI) and inter carrier interference (ICI), which causes the serious deterioration in bit-error-ratio (BER) performance of signals [4]. Synchronization offset includes sampling clock offset (SCO) and symbol timing synchronization (STS) in IM/DD-OFDM. The digital method of SCO compensation in frequency domain has been developed [5].

The STS algorithms are mainly based on correlation operation [6]–[10]. It is convenient to utilize the auto-correlation STS algorithms to realize carrier synchronization, which is not required in IM/DD-OFDM system. Meanwhile, the structure and the calculation of training sequences are complex, and the influence of noise is doubled when only

The associate editor coordinating the review of this manuscript and approving it for publication was Pallab K. Choudhury.

real signals are transmitted [6], [7]. In comparison with the auto-correlation STS algorithms, the cross-correlation (CC) STS algorithms are more suitable for IM/DD-OFDM PON [8]. However, two issues are still unsolved. First, the amplitude of correlation operation highly depends on the received power. Thus, widespread distributed ONU nodes will cause large variations of the amplitude. Second, amounts of multiplication operations increase the computation overhead. For the field programmable gate array (FPGA)-based real-time OFDM-PON systems, the STS algorithms with low resource utilization are significant for the low-cost architectures [8]–[10].

In order to reduce the computational complexity, the operations of symbols' XNOR or addition/subtraction have been used instead of multiplication operation [11]. Nevertheless, amplitude information of received data is neglected in the operations of bit XNOR or signed bit extracting, which reduces the sharpness of the amplitude peak because of the lost amplitude information. Furthermore, amplitude detection of received symbols avoids the correlation operation with computational complex multipliers but the amplitude threshold must be selected strictly [10]. Therefore, a cross-correlation-based STS method with the lower resource-utilization and power-independence will be important in IM/DD-OFDM PON. We proposed a simple proportional-sign cross-correlation (PS-CC) STS algorithm with lower power-independence and verified its feasibility in the conventional OFDM-PON system [12].

In this work, we designed a baseband FPGA IM/DD OFDM receiver to implement the proposed PS-CC STS algorithm. Based on the developed FPGA platform, we measured the correlation values of the peak PS-CC, mean PS-CC, peak CC and mean CC STS algorithms with the increasing fiber length from 0 km to 30 km. The measured results show that the proposed PS-CC STS algorithm has low power dependence and only 1.98% variation of peak amplitude is induced by the 30-km fiber transmission. Meanwhile, we measured the constellation diagrams of the transmitted 16 quadrature amplitude modulation (QAM) signal in the cases of back-to-back (BTB) and 30-km fiber transmission to verify the effectiveness of the FPGA hardware architecture. Finally, BER curves were measured to analyze influences of system parameters.

The rest of the paper is organized as follows. Section II describes the STS principles of the conventional correlation and the proposed proportional-sign cross-correlation. Section III illustrates the experimental setup, the FPGA verification platform and the involved FPGA blocks. Section IV shows the results of FPGA implementation. Finally, the conclusions are drawn in Section V.

II. THEORY OF SYMBOL TIMING SYNCHRONIZATION

In this section, we introduce the conventional auto-correlation and cross-correlation methods of symbol timing synchronization and analyze their pros and cons. In order to deal with the issues of computation complexity and power-independence, we propose the proportional-sign cross-correlation method. In the proposed method, we utilize sign operation instead of multiplication operation to decrease the resource utilization. Meanwhile, the cross-correlations between local symbols and received symbols are normalized to mitigate the influence of unbalanced powers caused by various fiber paths in OFDM-PON systems.

A. CONVENTIONAL SYMBOL TIMING SYNCHRONIZATION

The conventional methods of symbol timing synchronization mainly are based on autocorrelations of received signals. The received sequence consists of the cyclic prefix, the training sequence for synchronization and the OFDM symbols. The autocorrelation profile of the received signal is obtained by multiplying it with its time-shifted copy, written as [6],

$$M(d) = |P(d)|^2 \Big/ (R(d))^2 \tag{1}$$

where

$$P(d) = \sum_{k=0}^{N/2-1} r^*(d+k)r(d-k) \tag{2}$$

$$R(d) = \sum_{k=0}^{N/2-1} |r(d+k)|^2 \tag{3}$$

where $r(d)$ is the received d-th symbols, k is integer and N is the length of the training sequence for synchronization. The synchronization is implemented by searching the maximum value of the received signal's autocorrelation amplitude as the location of the training sequence for synchronization. By designing the training sequence for synchronization, the autocorrelation profile can be optimized to achieve more accurate timing synchronization [6]. However, the fourth-power operation of the received symbols requires more computational cost and the computational complexity will scale significantly with the increase of symbols.

Meanwhile, the timing synchronization can also be realized by cross correlations of received signals, given by

$$M(d) = \sum_{k=0}^{N-1} r(d+k)s(d) \tag{4}$$

where $s(d)$ and $r(d)$ are the local and received d-th symbols, respectively. However, the cross-correlation method in Eq. (4) still requires many multiplication operations between local symbols and received symbols. Moreover, ONU nodes in OFDM-PON system are always distributed widely and therefore different fiber paths will cause various power losses. Thus, the powers' unbalance of receiver signals will have an important influence on the amplitude of the correlation operation in Eq. (4).

B. PROPOSED PROPORTIONAL-SIGN CROSS-CORRELATION SYMBOL TIMING SYNCHRONIZATION

Figure 1 shows the OFDM frame structure of the proposed PS-CC STS scheme. The frame is composed of the cascaded

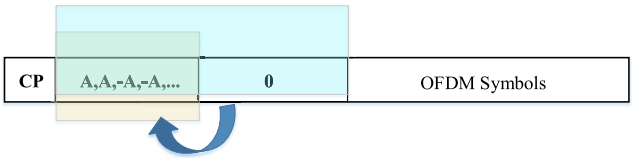


FIGURE 1. OFDM frame structure of the proposed PS-CC STS scheme.

cyclic prefix (CP), training sequence for synchronization and OFDM symbols. The CP is normally used as the guard band between successive symbols to mitigate ISI. The training sequence for synchronization consists of N/2 bipolar no return-to-zero (BNRZ) with amplitude of A and N/2 zeros, where N/2 zeros are utilized to speed up the convergence of the proposed PS-CC STS method and N is the number of the carriers. In comparison with other short repetitive training sequences, the frame structure in Fig.1 is quite simple.

In order to avoid the usage of multiplication operation with high computational complexity, we use the sign operation in the proposed PS-CC STS scheme. The cross-correlation is written as,

$$C(d) = \left| \sum_{k=0}^{N/2-1} sign\left[s\left(N/2-1-k\right)\right] \cdot r(d-k) \right| \quad (5)$$

where $s(k)$ and $r(k)$ are the local and received k-th symbols, respectively.

In most OFDM-PON systems, the users are generally widely distributed and therefore the powers of the receivers vary with fiber distances between the users and the optical line terminal (OLT). In order to mitigate the influence of powers' variation, C in Eq. (5) is normalized, given by

$$R(d) = \frac{C(d)}{\left(\sum_{m=0}^{N-1} C(d-1-m)\right) \Big/ N} \quad (6)$$

where N is an integer power of 2 and the shift operation in hardware is utilized to avoid additional division of the average operation.

An approximate constant amplitude peak can be achieved from Eq. (6) for widely distributed users with various received powers from various fiber transmission distances. On the contrary, the conventional CC STS algorithm must search the maximum value in the data window larger than the length of an OFDM frame to mitigate the influence of the receiving power inconsistency [13]. Larger processing delay will be induced when the algorithm searches the maximum value. Meanwhile, more carriers will consume more storage resources in the real-time hardware system.

Finally, according to Eq. (7), when $R(d)$ is larger than the decision threshold, the current data is the first sampled point of the frame head, i.e., the training sequence for synchronization, and the initial position of m-th OFDM symbol can be found by removing the training sequence and the CP before each OFDM symbol.

$$d_s(m) = \arg_d \{R(d) > T_h\} + N_s \cdot m \quad (7)$$

where $d_s(m)$ is the first sampled data of m-th OFDM symbol. $\mathrm{Arg}_d\{\}$ is the argument of $R(d)$, where the values of $R(d)$ larger than T_h are included. T_h is the predetermined decision threshold, and N_s and m denote the symbol length and serial number of each OFDM symbol, respectively.

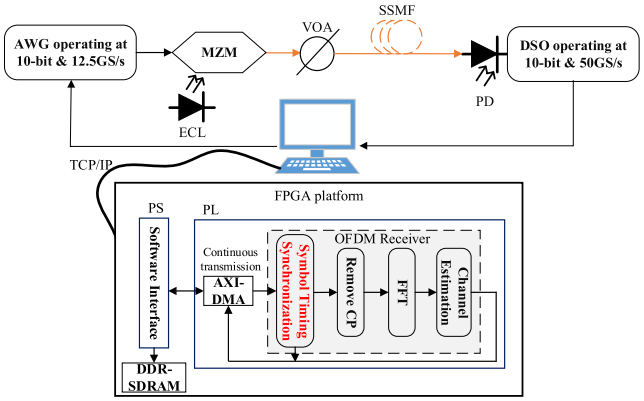


FIGURE 2. Experimental setup and FPGA platform.

III. EXPERIMENTAL SETUP AND FPGA IMPLEMENTATION

In this section, we illustrate the experimental setup of the proposed symbol timing synchronization in the 16-QAM IM/DD OFDM-PON system and explain its FPGA implementation.

A. EXPERIMENTAL SETUP

Figure 2 shows the experimental setup and FPGA platform. The transmitted OFDM digital signal is generated offline through MATLAB and loaded into a 50-GSamples/s arbitrary waveform generator (AWG) with 10-bit digital-to-analog converter (DAC). The signal is modulated to the optical carrier of the external cavity laser (ECL) by the Mach-Zehnder modulator (MZM). The launched power into the standard single mode fiber (SSMF) is adjusted to 0 dBm by a variable optical attenuator (VOA). We use 7-km, 24-km and 30-km SSMFs to emulate the scenarios, where various users have different distances from the OLT. The fiber attenuation, fiber dispersion at 1550 nm, fiber nonlinear coefficient and fiber polarization mode dispersion are 0.2 dB/km, 18 ps/nm·km, 1.2 $W^{-1}km^{-1}$ and 0.2 ps/$\sqrt{}$km. At the receiver end, the optical signal is converted into the electrical signal by a photodetector (PD). After that, the digital signal is acquired by the analog-to-digital converter (ADC) in 50-GSamples/s real-time digital storage oscilloscope (DSO).

Multiple identical data frames sent by the AWG and acquired by the DSO, are stored in personal computer (PC). The data interaction is implemented between the PC and the FPGA platform in the form of transmission control protocol/internet protocol (TCP/IP) network packets.

The functions of FPGA-based digital signal processing (DSP) include the symbol timing synchronization,

TABLE 1. Parameters of the OFDM receiver.

Parameter	Value
Number of Fast Fourier Transform points	128
Number of OFDM symbols per frame	100
Number of effective data carrier	32
Modulation format	16-QAM
Length of training sequence for synchronization	128
Data bit width of input fixed point (equivalent to ADC precision)	10-bit
System's clock frequency	100-MHz

the removal of CP, the subcarrier demultiplexing through fast Fourier transform (FFT), the data extraction, the channel estimation based on least squares, the QAM de-mapping and the decoding, as shown in Fig. 2.

B. FPGA VERIFICATION PLATFORM

In this work, ZYNQ is used as the core processor of the FPGA platform, which is divided into two parts, i.e., processing system (PS) and programming logic (PL).

The PS completes the data-interaction function of the system, and all operations are realized by controlling hardware resources with embedded software. First, the PC transmits multiple data frames to the network interface of PS side. In the process of receiving data, the PS transfers the received data to double data rate synchronous dynamic random-access memory (DDR-SDRAM). After the cache is completed, advanced extensible interface (AXI) direct memory access (DMA) continuously transfers data to the PL side, simulating the real-time data acquired by the ADC. After processed by the PL, the data is transmitted to the PC to complete the hardware loop verification.

The PL part of ZYNQ is the hardware implementation of related algorithms in the receiver. This part adopts the pipeline parallel architecture to meet the demand of real-time processing. The specific parameters of the OFDM receiver are shown in Table 1.

C. THE PROPOSE PS-CC BLOCK

In order to reduce the processing delay and the hardware resources, the calculation method in the receiver is the fixed-point operation. It is feasible for a fixed-point number to achieve the tradeoff between higher computational accuracy and lower hardware resource.

The STS part was implemented in the system generator (SG) environment by using the model-based design method. The operations with the requirement of high flexibility were designed by Verilog hardware description language (HDL) and imported into the environment in the form of black box.

Figure 3 shows the top-level hardware model of the STS. From left to right, it consists of four parts: calculation of the absolute correlation peak $C(d)$ of Eq. (5), calculation of the relative correlation peak $R(d)$ of Eq. (6), threshold detection and data extraction by removing the training sequence for

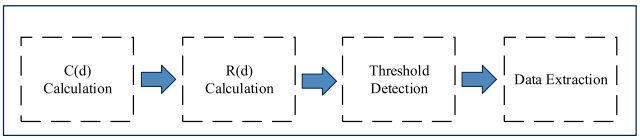


FIGURE 3. Top-level hardware architecture of STS.

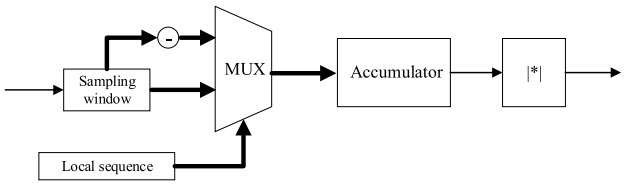


FIGURE 4. Hardware architecture of $C(d)$ calculation.

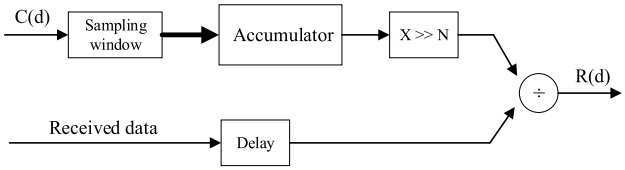


FIGURE 5. Hardware architecture of $R(d)$ calculation.

synchronization. Figure 4 and Figure 5 show the hardware architectures of the first two modules in Fig. 3.

The module of $C(d)$ calculation has the similar structure as that of the cascaded integrator-comb (CIC) filter, as shown in Fig. 4. First, multiple data in parallel are yielded in the module of sampling window. After that, in correlation module, the symbolic operation is performed on the data at the corresponding position of the local sequence. Then, in the module of accumulator, sum operation is implemented. Finally, in the absolute module, the absolute values of the sum results are taken.

The first half of $R(d)$ calculation module is similar as that of $C(d)$ calculation module, both of which are summed in a module of sampling window, as shown in Fig. 5. The difference is that the sum results in Fig. 5 are shifted to the right by 7 bits to average the sum results with low hardware resources, as required in Eq. (6). To calculate the proportional values, a divider intellectual property (IP) core is called to yield the results.

In the proposed STS block, the modules of the sampling window, the accumulator and the correlation are the black boxes designed with HDL and other functions are built from the available modules.

D. OTHER BLOCKS

In addition to the STS module, the designed OFDM receiver in this work also includes other DSP operations, such as removal of CP, FFT, data extraction and channel estimation, QAM de-mapping and decoding.

In order to simplify the design, only simple least squares channel estimation is used to obtain the channel frequency

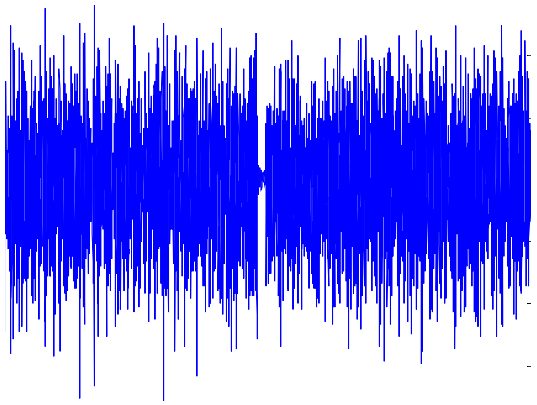


FIGURE 6. Waveform of the transmitted 16-QAM OFDM signal.

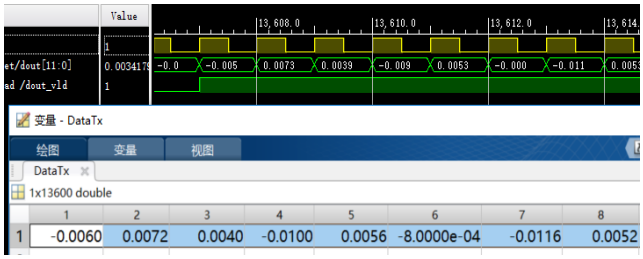


FIGURE 7. Simulation results of MATLAB and FPGA.

response. We use 10% OFDM symbols as the training sequence for channel estimation.

IV. IMPLEMENTAL RESULTS

Figure 6 is the waveform of the transmitted 16-QAM OFDM signal. The gap between OFDM frames in Fig.6 is caused by the training sequence for synchronization with N/2 zeros.

Figure 7 shows the compared results between the data in MATLAB and FPGA. In Fig. 7, the first row is the waveform of the system clock, as shown in yellow. The second row is the extracted data (dout) after the STS algorithm by MATLAB. The third row is the waveform of the enable signal (dout_vld) and its high-level indicates that the data of the corresponding clock cycle is valid in FPGA. The data (DataTx) in the table of Fig. 7 is the extracted data after the STS algorithm by FPGA. As shown in the Fig. 7, the MATLAB data dout (−0.005, 0.0073, 0.0039, −0.009, 0.0053, −0.000, −0.011, 0.0053) are consistent with the FPGA data DataTx (−0.0060, 0.0072, 0.0040, −0.0100, 0.0056, −8.0000e-04, −0.0116, 0.0052), and the trivial difference is caused by the quantitative errors.

Figure 8 shows the calculated results of internal correlation calculation of FPGA using integrated logic analyzer (ILA). The results are displayed in analog form and there is an obvious correlation peak, as shown in Fig. 8.

Figure 9 shows the peak and average values of correlation operation with the increasing fiber length from 0 km to 30 km. The peak PS-CC values denote the maximum amplitude value of correlation in Eq. (6) and the mean PS-CC values are their average values, as shown by the red circle-marked solid curve and the red circle-marked dashed curve in Fig. 9, respectively. The peak CC and the mean CC values represent the maximum amplitude values of correlation in Eq. (4) and their average values, as shown by the blue diamond-marked solid curve and the blue diamond-marked dashed curve in Fig. 9, respectively.

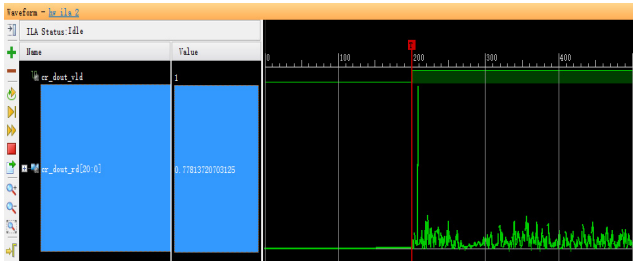


FIGURE 8. Synchronization results captured by ILA.

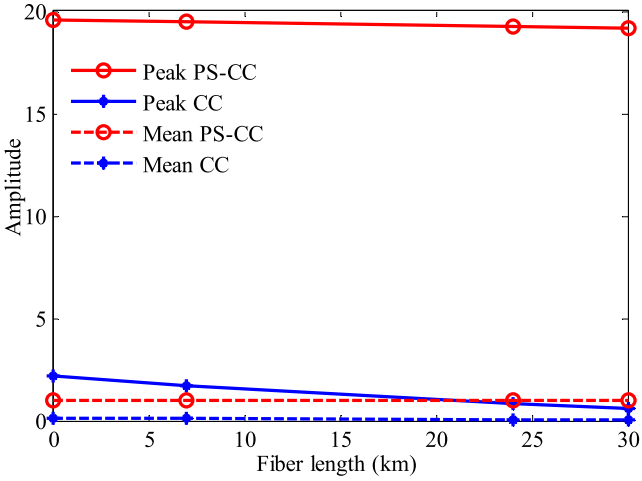
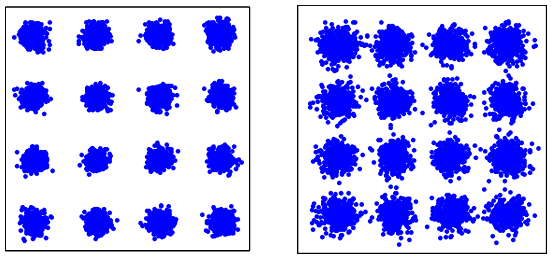


FIGURE 9. Measured correlation amplitudes vs. fiber length (km).

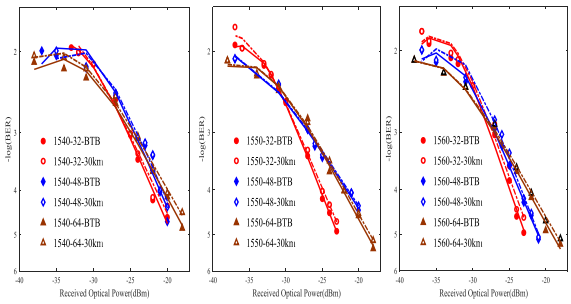
It can be seen in Fig. 9, the difference between the peak and average values of the correlation operation is larger. The variation of peak values is smaller in the PS-CC STS scheme than that in the conventional CC STS scheme. Compared with the BTB case, 30-km fiber transmission only introduces 1.98% variation of peak amplitude when the PS-CC STS is used. Therefore, the detection threshold T_h in Eq. (7) of the proposed PS-CC STS method can be set to a constant over a wide range, which is more suitable for the IM/DD OFDM-PON system. The detection threshold depends on the measured results in Fig. 9 and can be any constant between the peak value and the average value, as shown by the circle-marked solid curve and the circle-marked dashed curve in Fig. 9.

The constellation diagrams of 16-QAM signals after channel equalization in the cases of BTB and 30-km fiber transmission are shown in Fig. 10, where the proposed PS-CC STS is used. The constellation diagram becomes worse with the increase of the fiber length because of the accumulated fiber dispersion and the decreased signal power. From these constellation diagrams, it is obvious that the proposed PS-CC



(a) BTB (b) 30 km fiber transmission

FIGURE 10. Constellation diagrams of BTB and 30-km fiber transmission.



(a) 1540.003nm (b) 1550.036nm (c) 1560.038nm

FIGURE 11. Measured BER vs. received optical power (dBm) curves in the cases of BTB and 30-km fiber transmission at 1540.003 nm, 1550.036 nm and 1560.038 nm with 32, 48 and 64 data subcarriers.

STS method correctly finds the starting position of each OFDM symbol and the subsequent DSP operations are successfully completed.

Moreover, we investigate influences of OFDM system's parameters such as the data rate, the fiber transmission and the wavelength of optical carrier on BER performances based on the experimental setup in [12]. The noise level of the signal is controlled by cascaded variable optical attenuator and erbium-doped fiber amplifier for BER measurement. Figure 11 shows the measured BER curves versus the received optical power. The data rate is changed by varying the number of data subcarriers. In Fig.11, 32, 48 and 64 data subcarriers are used and the number of total subcarriers is 128. In the 12.5-Gbaud 16-QAM experiment, the 1/16 symbol redundancy is used as the cyclic prefix and 1/10 symbols are used as the training sequence for channel estimation. If there are 32 data subcarriers, the effective net data rate is 10.55 Gb/s (12.5Gbaud×4 × 32/128 × 15/16×9/10). By increasing the data subcarriers, the effective net data rate can be increased.

From Fig.11, it can be seen that all signals have similar BER behaviors. Signals with less data subcarriers suffer less interference and therefore have better BER performance with steeper curves, as shown by circle-marked curves and triangle-marked curves. The 30-km fiber transmission causes trivial power penalty, as shown by solid curves and dashed curves in Fig.11. The signal at 1550.036 nm with 32 data subcarriers has better BER performance than that at 1540.003 nm and 1560.038 nm, as shown by the BER curves in Fig.11(a), (b) and (c).

TABLE 2. Utilization of hardware resource.

Name	Amount
Look up table (LUT)	9691
Look up table random access memory (LUTRAM)	738
Flip flop (FF)	13209
Block random access memory (BRAM)	12
DSP Slice (DSP 48E1)	21

Table 2 shows the amount of the used hardware resource after logic synthesis in the Vivado tool. Only 21 DSP48E1 are used for logical and arithmetic operations and most of them are applied to implement the FFT operation. Therefore, less hardware resource is arranged for the proposed symbol timing synchronization.

V. CONCLUSION

The PS-CC algorithm utilizes the normalized cross-correlation operation between the received symbols and the sign values of the local symbols and searches constant amplitude peaks for symbol timing synchronization. We designed the FPGA-based OFDM receiver to implement the proposed PS-CC scheme. The performance of power independence in the PS-CC scheme has been evaluated by measuring variation of peak amplitude in the cases of various fiber transmission and only 1.98% variation of peak amplitude over 30-km fiber transmission is observed. Meanwhile, the effectiveness of the developed FPGA hardware architecture has been verified by measuring the constellation diagrams of the transmitted 16-QAM signal. The characteristics of power independence and low resource utilization give the proposed PS-CC STS scheme more opportunities for real-time FPGA-based OFDM-PON application.

ACKNOWLEDGMENT

The authors would like to thank Prof. M. Yasin Akhta Raja from the University of North Carolina Charlotte for helpful comments and the anonymous reviewers for valuable ideas.

REFERENCES

[1] Y. Dong, R. Giddings, and J. Tang, "Hybrid OFDM-digital filter multiple access PONs," *J. Lightw. Technol.*, vol. 36, no. 23, pp. 5640–5649, Dec. 1, 2018.

[2] W. Mondal, D. Roy, S. Dutta, and G. Das, "Economic analysis of TWDM PONs: A sustainability and policy-making perspective," *IEEE/OSA J. Opt. Commun. Netw.*, vol. 11, no. 3, pp. 79–94, Mar. 2019.

[3] Y. Li, J. Han, and X. Zhao, "Performance investigation of a cost- and power-effective high nonlinearity tolerance OFDMA-PON scheme based on sub-nyquist sampling rate and DFT-spread," *IEEE Access*, vol. 7, pp. 43137–43142, 2019.

[4] Y. Mostofi and D. C. Cox, "Mathematical analysis of the impact of timing synchronization errors on the performance of an OFDM system," *IEEE Trans. Commun.*, vol. 54, no. 2, pp. 226–230, Feb. 2006.

[5] Z. Zhang, Q. Zhang, Y. Li, Y. Song, J. Zhang, and J. Chen, "A single pilot subcarrier-based sampling frequency offset estimation and compensation algorithm for optical IMDD OFDM systems," *IEEE Photon. J.*, vol. 8, no. 5, Oct. 2016, Art. no. 7804209.

[6] B. Park, H. Cheon, C. Kang, and D. Hong, "A novel timing estimation method for OFDM systems," *IEEE Commun. Lett.*, vol. 7, no. 5, pp. 239–241, May 2003.
[7] M. Bi, X. Zhuo, X. Fu, X. Yang, and W. Hu, "Cellular neural network encryption scheme for time synchronization and CPAs resistance in OFDM-PON," *IEEE Access*, vol. 7, pp. 57129–57137, 2019.
[8] X. Q. Jin and J. M. Tang, "Optical OFDM synchronization with symbol timing offset and sampling clock offset compensation in real-time IMDD systems," *IEEE Photon. J.*, vol. 3, no. 2, pp. 187–196, Apr. 2011.
[9] X. Duan, R. P. Giddings, M. Bolea, Y. Ling, B. Cao, S. Mansoor, and J. M. Tang, "Real-time experimental demonstrations of software reconfigurable optical OFDM transceivers utilizing DSP-based digital orthogonal filters for SDN PONs," *Opt. Express*, vol. 21, no. 16, pp. 19674–19685, 2014.
[10] J. Peng, Y. Sun, H. Chen, T. Xu, Z. Li, Q. Zhang, and J. Zhang, "High-precision and low-complexity symbol synchronization algorithm based on dual-threshold amplitude decision for real-time IMDD OFDM-PON," *IEEE Photon. J.*, vol. 11, no. 1, Feb. 2019, Art. no. 7201514.
[11] J. Valls, J. Corral, J. S. Bruno, and V. Almenar, "Low-complexity time synchronization algorithm for optical OFDM PON system using a directly modulated DFB laser," *IEEE/OSA J. Opt. Commun. Netw.*, vol. 11, no. 7, pp. 1025–1033, Nov. 2015.
[12] X. Chen, "Proportional sign-cross-correlation for symbol timing synchronization of OFDM-PON," in *Proc. 24th OptoElectron. Commun. Conf. (OECC) Int. Conf. Photon. Switching Comput. (PSC)*, Fukuoka, Japan, Jul. 2019, pp. 1–3.
[13] M. Chen, J. He, J. Tang, X. Wu, and L. Chen, "Real-time 10.4-Gb/s single-band optical 256/64/16QAM receiver for OFDM-PON," *IEEE Photon. Technol. Lett.*, vol. 26, no. 20, pp. 2012–2015, Oct. 15, 2014.

XIAOYI CHEN received the M.Eng. degree from Soochow University, Suzhou, China, in 2019. His current research interests include FPGA and communication systems.

MINGYI GAO (M'10–SM'13) received the Ph.D. degree in information and communication engineering from Shanghai Jiao Tong University, Shanghai, China, in 2007. From 2007 to 2009, she was a Research Fellow with the Japan Society for the Promotion of Science, The University of Tokyo, Tokyo, Japan. From 2009 to 2013, she was with the National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan. Since 2013, she has been with Soochow University, Suzhou, China. Her current research interests include optical communication, signal processing, FPGA, and machine learning.

YANPING SHA is currently pursuing the M.Eng. degree with the School of Electronic and Information Engineering, Soochow University, Suzhou, China. His current research interests include optical OFDM communication systems, channel coding, and FPGA.

JI ZHANG received the B.Sc. degree in microelectronics from the Department of Computer Science, Peking University, China, in 1989. From 1989 to 1994, he was with the Institute of Acoustics, Chinese Academy of Science, for ASIC designing of a booth-wallace tree multiplier. From 1994 to 1996, he was with Beijing SJC Electronic Design Co. Ltd., to develop PC interface program and VME BUS interface board. From 1996 to 1997, he was with Ultmost to design VCD product. From 1998 to 2000, he was a Technical Advisor with the China Integrated Circuit Design Center (CIDC) for MPEG2 chip design verification. From 2000 to 2001, he was with Tsinghua Himage Tech Ltd., as a Director of the EDA Laboratory, IC Department, Research Institute, Tsinghua University, Shenzhen, to develop DVB-S product. From 2001 to 2002, he was with Beijing Haier IC Design Co. Ltd., as a Chief Technical Advisor to develop the embedded system for DVT SoC and SoC Chip verification. From 2002 to 2004, he was with BLX CPU Ltd., as a Vice President of engineering to lead the team for software, system, SoC, and IC backend design. From 2004 to 2006, he was with Celestial semiconductor/Grandview semiconductor (Spin off) as a Director of technical marketing. From 2006 to 2010, he was with Telegene Tech Ltd., to develop products and solutions for multimedia as a Research and Development Team Leader. Since 2010, he has been with Soochow University, Suzhou, China. His current research interests include FPGA and DSC-chip development.

ERXI FANG received the Ph.D. degree in signal and information processing from Soochow University, Suzhou, China, in 2017. He is currently an Associate Professor with Soochow University. His research interests include the embedded systems and medical image processing.

HONGLIANG REN received the M.Sc. degree in optical engineering from Zhengzhou University, Henan, China, in 2004, and the Ph.D. degree from Shanghai Jiao Tong University, Shanghai, China, in 2008. He is currently an Associate Professor of information and communication engineering with the Zhejiang University of Technology. His current research interests include communication signal processing and optical sensing.