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Electro-Thermal-Mechanical Multiphysics Coupling Failure Analysis Based on Improved IGBT Dynamic Model

JIANBO ZHOU, BING LI, YIGANG HE, WEIBO YUAN, JIACHENG LIU, AND HUADONG NI
School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China

Corresponding author: Bing Li (libinghnu@163.com)

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ABSTRACT Failure of the power device can have a very large impact on the entire power circuit. IGBT as the main power device, ensuring its reliability becomes more and more important. In different environments, there will be large differences in the failure rate of IGBTs. Therefore, studying the failure mechanism of IGBT is of great significance to ensure the reliability of IGBT. Firstly, the IGBT dynamic model is constructed and the model is improved to correct the power consumption error. Then the IGBT finite element model is used to analyze the electro-thermal-force of different material layers, at the same time, the distribution of stress and temperature between different materials are analyzed. Finally, the JavaScript script is used to generate random defects of the solder layer, and the effects of different defects of the solder layer on the weakest part of the IGBT are studied, including voids, cracks, and solder layer falling off. The results of the analysis show that after the IGBT defects reach a certain level, the solder layer voids, the solder layer fall off, and the solder layer cracks have a great influence on the IGBT junction temperature and stress. Among them, shedding and cracks have a greater influence on the stress of the solder layer.

INDEX TERMS IGBT, dynamic model, electro-thermal-mechanical, three-dimensional finite element.

I. INTRODUCTION

Insulated Gate Bipolar Transistor (IGBT) is a power semiconductor device which has a fully controlled type with high input impedance, fast switching speed, low driving power, simple drive circuit, high current density, and reduced saturation voltage [1]–[3]. IGBT is widely used in new energy [4], high-speed rail [5], military [6],etc. Power devices in these fields have a harsh working environment and require high reliability [7], [8]. The failure of power electronics is closely related to the application scenario. Different analysis models should be constructed for different applications. It takes a lot of time for the reliability experiment process and consumes a lot of human and financial resources [9], [10]. Therefore, it is especially important to improve the accuracy of IGBT model power calculation. [11].

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IGBTs are usually made up of different materials that are distributed between different levels, and the coefficients of thermal expansion between the materials are also different. During the temperature cycling process, the solder layers and bond wires that are weak in material properties are broken and fall off. [12]–[14] shows that IGBT solder layer defects are usually started from the edge. The maximum stress points are distributed at the diagonal corners of the chip. The failure probability of thermal stress concentration points is higher than in other parts. IGBT power consumption is the main cause of the chip's heat generation, and the power consumption calculation accuracy directly determines the IGBT junction temperature and stress field distribution accuracy [15]. Current methods for fitting IGBT device temperatures include mathematical fitting methods such as Foster and Cauer models, as well as simulations based on 3D finite elements [16]. The power consumption simulation error of these methods is large, and Direct measurement of chip junction

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temperature requires sophisticated instrumentation, and the result also has an error [17]. H. Daou and M. Ameziani have made some progress in simulating the power consumption curve of IGBT through Simplorer and Q3D, but there is still a big error [18]. Scholars have proposed many improved models to estimate the IGBT failure mechanism. However, there are still many problems.

To address the thermal stress analysis problem, the finite element model was developed to solve multiple physical coupling situations [19]. The finite element analysis is to solve the constraint relationship between physical formulas, then decompose a realistic three-dimensional model into small units, and solve the solution of each unit to solve the solution of the whole model [20]. The literature confirms that finite element analysis can accurately reflect the heat and thermal stress generated in the operation of IGBT devices, also can help us to understand the relationship between these parameters [21], [22]. However, it is often difficult to obtain actual IGBT operating parameters, and the extraction of physical parameters requires a large amount of financial and material resources [23].

Some good choices to analyze the thermal characteristics of IGBTs are the Faster and Cauer model [24]. The Cauer model can characterize the physical structure of the IGBT model, and there is a correspondence between the Cauer model and the different layer materials of the IGBT [11], [25]. However, the Foster model cannot. The Cauer model is usually used to predict the thermal resistance. The commonly used Cauer model is 4th orders, Ze Wang and Wei Qiao improved the prediction accuracy by the 7th-order Cauer mode [26]. The Carl model also has drawbacks that rely heavily on the geometry of the chip [27], [28]. Sometimes the chip supplier does not directly provide the chip size. The data on the chip's datasheet is needed to eliminate this error.

This paper proposes to improve the dynamic model and improve the shortcomings in the literature. Firstly, the IGBT power consumption and heat generation rate are obtained by dynamic model simulation, then the heat distribution and stress distribution are obtained by the finite element model, and the accuracy of the simulation is verified by experiments. Section II and section III is the power simulation and finite element model, section IV is the simulation experiment result, section V is a conclusion.

II. CORRECTION OF IGBT DYNAMIC MODEL

The IGBT dynamic model is shown in Figure 1.

The dynamic model usually consists of an electrical model, an oscillating cancellation model, and a reverse diode electrical model. Model construction parameters are often derived from datasheets.

In practical applications, V_{CE} and I_C are important parameters for measuring IGBT power consumption, and V_{ce} can be obtained directly from the voltage difference between V_E and V_C. Therefore, the accuracy of IGBT voltage and diode current determines the accuracy of the dynamic model. In the

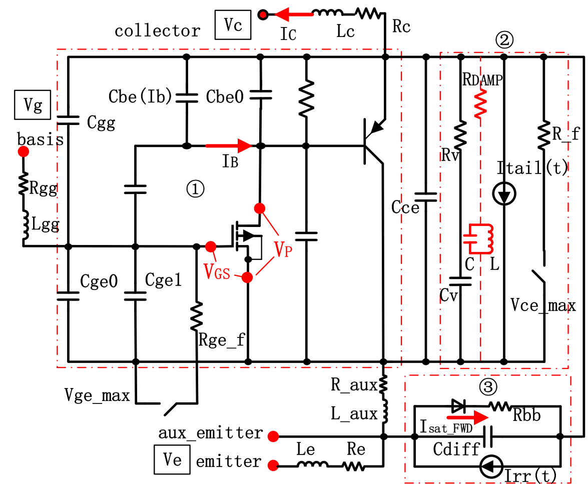

FIGURE 1. correction curve of the dynamic switching process.

model, the saturation voltage drop of the FET is V_{sat}:

$$V_{sat} = A_FET \cdot (V_{GS} - V_P)^{M_FET} \quad (1)$$

where M_FET is the FET saturation index, and the A_FET and M_FET are temperature dependent. V_P is the pinch-off voltage at the rated temperature of the FET, that is, the voltage between the drain and the source, and V_{GS} is the threshold voltage of the FET, that is the voltage between the gate and the source.

$$I_{sat} = \frac{K}{2}(V_{GS} - V_P)^{N_FET} \quad (2)$$

where K is the transistor temperature and N_FET is the transfer characteristic index of the FET. Normally, I_D has different operating states and is therefore represented by different formulas, and I_D can be used for the calculation of the collector current.

When the device is in the linear region, the FET's continuous leakage current is:

$$I_D = I_{sat}(1 + V_{DS} \cdot KML)(2 - \frac{V_{DS}}{V_{sat}})\frac{V_{DS}}{V_{sat}} \quad (3)$$

The FET's continuous leakage current is:

$$I_D = I_{sat}(1 + V_{DS} \cdot KML) \quad (4)$$

where V_{DS} is the drain voltage,I_{sat} is the FET drain current, and KML is the channel length modulation factor of the FET.

I_C is the collector current, and its calculation accuracy determines the accuracy of the final power consumption. Its value can be obtained by formula (5). I_B is the FET reference current and is typically taken as $I_B = I_D$.I_B can also be obtained from equation (6):

$$I_C = I_B BN \quad (5)$$

$$I_B = I_{sat}\left(e^{\frac{V_{BE}}{(V_T M_BJT)}} - 1\right) \quad (6)$$

where V_T is the turn-on voltage at the rated temperature, M_BJT is the BJT ideal factor at the rated temperature,

and BN is the gain of BJT at the rated temperature. V_{BE} is the BJT base current. M_BJT is the ideal factor, and the saturation current I_{sat} depends on the temperature. The formula of voltage V_T calculated by:

$$V_T = \frac{k \cdot (T_N + 273)}{q} \tag{7}$$

where k is the Boltzmann constant, $k = 1.381\text{E-}23 \cdot m^2 \cdot s^{-2} \cdot K^{-1}$; q is the basic charge, $q = 1.602^{-19}$C, T_N is the current temperature.

Reverse diode quiescent current (I_{FWD}) can describe diode steady-state current, I_{FWDSAT} is the drain current of the diode, and V_T is the voltage applied across the diode.

$$I_{FWD} = I_{FWDSAT} \cdot \left(e^{\frac{V_{FWD}}{(M_FWD \cdot V_T)}} - 1 \right) \tag{8}$$

If the difference between the drift voltage and the junction voltage is equal to 0, it can be considered that the device has a voltage and current dynamic process:

$$SHIFT \cdot V_{DIFF} - V_{JNCT} = V^*_{JNCT} = 0 \tag{9}$$

where $SHIFT$ is the voltage drift factor. V_{DIFF} is the diffusion voltage, and V_{JNCT} is the junction voltage.

When $V*_{JNCT}$ is positive, the calculation formula of the capacitance is as follows:

$$C(V^*_{JNCT}) = C_0 \left(1 + (\beta - 1) \cdot (1 - e^{-\frac{V^*_{JNCT} \cdot \alpha \cdot (1-\delta)}{(\beta-1) \cdot V_{DIFF}}} \right) \tag{10}$$

where C_0 is the initial value of the capacitor, α is the capacitance index, β is the peak coefficient, and δ is the weighting factor when the $V*_{JNCT}$ is negative, the calculation formula of the capacitance is:

$$C(V^*_{JNCT}) = C_0 \left(\delta + \frac{1 - \delta}{(1 - \frac{V^*_{JNCT}}{V_{DIFF}}) \cdot \alpha} \right) \tag{11}$$

Introduce a damping resistor to prevent abnormal oscillations in the circuit, which is calculated as:

$$R_{DAMP} = DAMPING \sqrt{\frac{L}{C(V)}} \tag{12}$$

where $DAMPING$ is the drag coefficient. L is the parasitic inductance of the IGBT dynamic circuit, C(V) is the IGBT parasitic inductance [29].

The static and dynamic parameters of IGBT are related to its temperature distribution. When building the Simplorer model, its thermal network must be modeled. The Cauer model of the IGBT module consists of three parts, namely the thermal network of the IGBT chip to the heat sink, the thermal network of the diode chip to the heat sink, and the thermal network of the IGBT heat sink to the environment. In this paper, the IGBT and the diode use a fourth-order RC network. The radiator and the environment use a first-order RC network. The RC parameters are extracted from the thermal resistance curve of the datasheet, and the Foster RC parameters are obtained and converted to the Cauer model RC parameters.

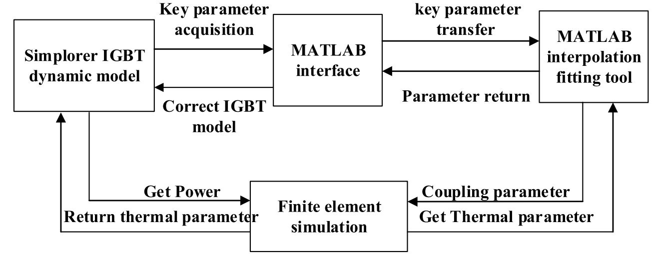

FIGURE 2. IGBT voltage and current correction flowchart.

The Foster network model, whose thermal resistance network can be described by the following equation:

$$Z_{th} = \sum_{i=1}^{n} R_{thi} \left(1 - e^{-\frac{t}{R_{thi} \cdot C_{thi}}} \right) = \frac{T_j(t) - T_c(t)}{P(t)} \tag{13}$$

where T_j(t) is the junction temperature of the device as a function of time, T_c(t) is the shell temperature as a function of time, and P(t) is the power dissipation of the device during the cooling process. The thermal resistance network RC parameters of the Cauer model can be converted by the Foster model, as shown in equation (14).

$$Z_{th} = \frac{1}{sC_1 + \frac{1}{R1 + \frac{1}{sC2 + \frac{1}{R2 + \ldots + \frac{1}{R_n}}}}} \tag{14}$$

In the traditional thermal model, the order of Cauer model is 4, and the improved Cauer model is proposed in the literature [26], which increases the order of the model to 7, and improves the calculation method of the thermal conduction angle and the heat channel.

A. IMPROVE IGBT DYNAMIC MODEL

To correct the power consumption error, a closed-loop correction model based on MATLAB and Simplorer co-simulation are proposed. The principle is shown in Fig.2:

In this regard, the parameters used to construct the IGBT in Simplorer are transferred to MATLAB. The current and voltage of the IGBT are also transferred to MATLAB through the MATLAB interface in Simplorer, and then the interpolation and fitting tools are used to calculate the correction factors of voltage and current. The 3D finite element simulation results are fed back to the dynamic model and the fitting formula to realize the multiphysics coupling closed-loop correction.

The polynomial fitting method is used to correct the IGBT voltage and current error. Equations 15 and 16 are mathematical expressions of the power correction model,

$$\begin{cases} I'_C = I_B \cdot BN \\ \quad + \dfrac{\alpha C_{ge} t^2 + \beta Rg t + m}{t^2 + q_1 t + p_1}, & t_0 < t < t_1, t_2 < t < t_3 \\ I'_C = I_B \cdot BN, & others \end{cases} \tag{15}$$

$$\begin{cases} V'_{ce} = V_{ce} \\ \quad + \dfrac{\gamma \cdot C_{ge} \cdot t^2 + \eta \cdot R \cdot g \cdot t + n}{t^2 + q_2 \cdot t + p_2}, & t_4 < t < t_5, t_6 < t < t_7 \\ V'_{ce} = V_{ce}, & others \end{cases} \tag{16}$$

During the IGBT turn-on period, where t_0 is the start time of the current and t_1 is the end time of the current,t_4 is the start time of the voltage and t_5 is the end time of the voltage. During the IGBT turn-off period,t_2 is the start time of the current and t_3 is the end time of the current, t_6 is the start time of the voltage and t_7 is the end time of the voltage. Analyze the voltage and current data in the manual before the correction. It is known that the voltage and current errors are mainly in the dynamic process, The dynamic process is divided into two parts, one is the IGBT turn-on phase and the other is the IGBT turn-off phase, In these two phases, the voltage dynamic process time in the turn-on phase is the interval (t_0,t_1), and the current is the interval (t_4,t_5). The turn-off process voltage dynamic time is the interval (t_2,t_3), and the current dynamic time is the interval (t_6,t_7). α,β,γ,η are the matching coefficient. R_g is the collector drive resistor,C_{ge} is the drive circuit capacitor, q and p are the matching coefficients in the correction [29]. The correction parameters fitted by the formula are shown in Tab 1.

TABLE 1. Key parameters of correction.

Parameters	Values	Parameters	Values
α	-2.034	p_1	-1.45 4
β	1.63	q_1	0.529 3
γ	3.623	m	-0.037 57
η	-4.419	p_2	-1.074
C_{ge}	$1.1\mu F$	q_2	0.288 6
R_g	10Ω	n	1.343

III. FINITE ELEMENT MODEL

A. ELECTRO-THERMAL-FORCE COUPLED MATHEMATICAL MODEL

There is no single physical field in nature, so this poses a challenge to the implementation of stress experiments, and the use of multiphysics analysis can approximate the coupling relationship between natural physics by the mathe- matical fitting. When IGBT is working, power consumption is the main cause of the heat generation of its devices. Due to the large difference in the thermal expansion coefficient of the materials constituting the IGBT, In the process of heat conduction, a temperature difference will occur between different materials, thus forming a stress difference. As the service life of the IGBT increases, the stress difference will cause the weak link of the IGBT material to fail. According to the heat transfer finite element theory, the heat conduction finite element equation is:

$$\begin{cases} \boldsymbol{C}^t \dot{\boldsymbol{T}} + \boldsymbol{K}^t \boldsymbol{T} = \boldsymbol{Q} \\ \boldsymbol{Q} = \boldsymbol{Q}^{nd} + \boldsymbol{Q}^c + \boldsymbol{Q}^g + \boldsymbol{Q}^j \end{cases} \tag{17}$$

where $\boldsymbol{C}^t$ is the heat capacity matrix, $\boldsymbol{K}^t$ is the heat conduction matrix, $\boldsymbol{T}$ is the node temperature, $\dot{T}$ is time vector temperature vector, $\boldsymbol{Q}^{nd}$ is the node heat flow rate vector, $\boldsymbol{Q}^c$ is facing the heat flow vector, $\boldsymbol{Q}^g$ is the heat flow rate load vector, $\boldsymbol{Q}^j$ is the heat source heat generation vector, temperature vector Q is the sum of the heat transfer vectors.

Electric field finite element equation satisfaction:

$$\boldsymbol{K}^V \boldsymbol{V} = \boldsymbol{I}^{nd} \tag{18}$$

where $\boldsymbol{K}^v$ is the conductivity matrix, $\boldsymbol{V}$ is the node voltage, $\boldsymbol{I}^{nd}$ is the current load.

When the IGBT module is working, the heat generated by the chip causes the temperature to rise, and the temperature change causes the resistance, thermal conductivity, specific heat capacity and other parameters to change, thereby generating thermo-electric coupling. The heat source $\boldsymbol{Q}^j$ of the internal heat source of the IGBT can be calculated according to the electric field equation:

$$\boldsymbol{Q}^j = \int_v \boldsymbol{N} \boldsymbol{V} \boldsymbol{g}^2 [\sigma(T)] dv \tag{19}$$

where $\boldsymbol{N}$ is the shape function matrix, $\boldsymbol{V}_g$ is the potential gradient vector matrix, σ(T) is the conductivity.

The finite element equation for thermal stress is:

$$\boldsymbol{K} \cdot a = \boldsymbol{P} \tag{20}$$

where $\boldsymbol{K}$ is the unit node force matrix, a is the node displacement, and $\boldsymbol{P}$ is the node temperature load. There is a coupling among heat conduction, electrical conduction, and thermal stress, so the iterative equations (17)~(20) can solve the multi-field coupling result.

B. THREE-DIMENSIONAL FINITE ELEMENT MODEL OF IGBT

Fig.3 shows the internal package of the IGBT, IGBTs generally consist of multiple layers of material from top to bottom, each layer has a different coefficient of thermal expansion. IGBT package consists of IGBT chip, diode chip, tin solder layer, copper layer, alumina ceramic, tin solder layer, copper substrate. The 6MBI400V-120-50 consists of 6 IGBTs and 6 diode chips. The IGBT chip is represented by T, and the diode is represented by D. The package size is often closely related to the accuracy of the simulation results, so it is necessary to collect accurate package sizes. The package size of this article is obtained by measuring the IGBT module and consulting the datasheet. The IGBT size parameters are shown in Tab.2 [30].

The chip heat flux is obtained by equation (21):

$$H = \frac{P_L}{V} \tag{21}$$

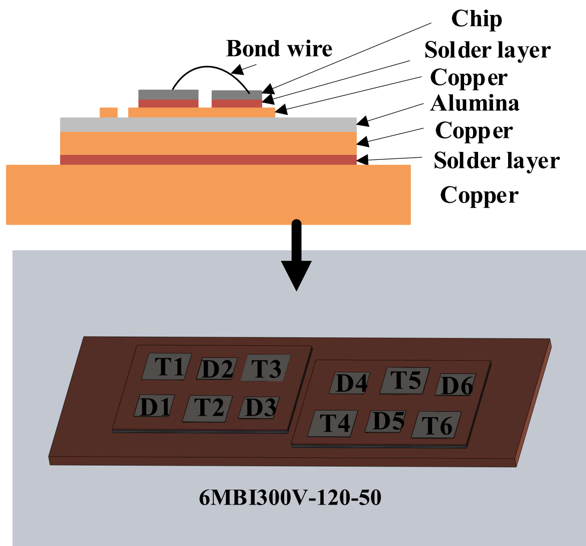

FIGURE 3. Structure of IGBT package.

TABLE 2. Layer size of IGBT.

IGBT struct	Size (mm)
Chip of IGBT	11×11×0.10
IGBT layer	11×11×0.08
Chip of Diode	9×9×0.10
Diode layer	9×9×0.08
Upper Copper	45×35×0.38
Al_2O_3	45×35×0.30
Lower copper	45×35×0.37
Solder layer	45×35×0.23
Copper Base	120×50×2.9

TABLE 3. Material properties.

Material	Cu	Al	$Ag_{3.5}Sn_{96.5}$	Al_2O_3	Si
Quality(Kg/m^{3})	8 960	2700	7400	3600	2300
Young's modulus /GPa	128	68	47.8	270	162
Poisson's ratio	0.37	0.3	0.4	0.28	0.28
Thermal Conductivity W/(m·K)	390	237	33	30	100
Specific heat capacity J/(kg·K)	400	900	234	850	900
CTE (/10-6·K-1)	16.9	21	30.2	6.5	2.5

where H stands for heat flux, P_L represents the heating power consumption of the device, and V indicates the area of the chip. The total power P_L is composed of IGBT turn-off power consumption, turn-on power consumption, and operating loss. The boundary conditions are the key factors for the accuracy of the simulation results. Therefore, it is necessary to ensure that the boundary conditions are consistent with the environmental conditions during the operation of the IGBT.

The 3D finite element simulation is limited to one cube with length, width and height are set to 120 mm, 50 mm, and 14 mm. Set a fixed constraint at the four corners of the copper substrate, and the periphery of the substrate is set to the Z-direction constraint, that is, the displacement $u_z = 0$. To simulate the real environment, set the ambient temperature to 25°C, the forced convection coefficient of the copper substrate is set to 4000W/(m2·K), and the forced convection coefficient of the four sides of the copper substrate is set to 20W/(m2·K) [29].

IV. SIMULATION EXPERIMENT AND RESULT ANALYSIS

In order to study the IGBT failure mechanism, this paper applies the dynamic model to the actual circuit.

The joint simulation of MATLAB and Simplorer is shown in Fig.4. The joint simulation includes the Simulink control module, communication module based on Simulink interface, and main circuit based on Simplorer. Among them, the communication module realizes the transmission of information between two kinds of software. Circuit parameters are shown in tab 4.

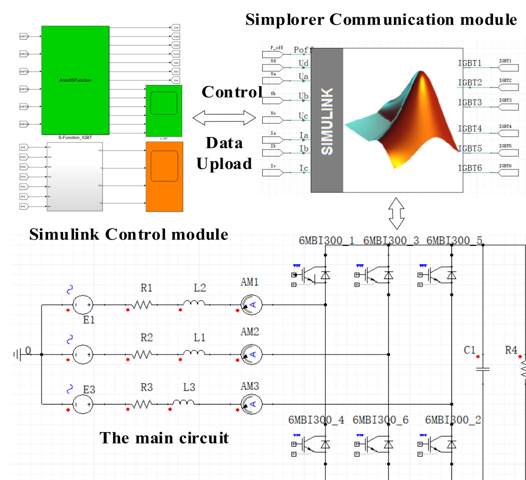

FIGURE 4. Three-phase rectification system.

TABLE 4. Parameters of rectifier system.

Component	Value
Power supply voltage	400V
Power resistance	0.0068Ω
Power Inductor	0.0023H
DC voltage	1200V
Load resistance	30Ω
Bus Capacitance	3mF

To test the voltage and current curves of the IGBT, the test platform of Fig.5 was built, which includes the power module, the drive circuit, the capacitor, the heat sink, and the oscilloscope for measuring the voltage. In the experiment, the dynamic voltage and dynamic current of the IGBT were

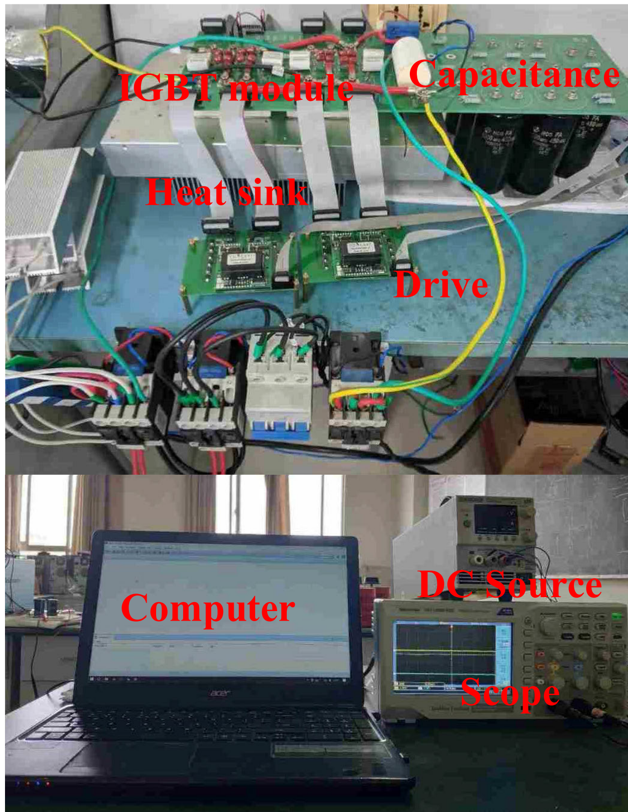

FIGURE 5. Test platform.

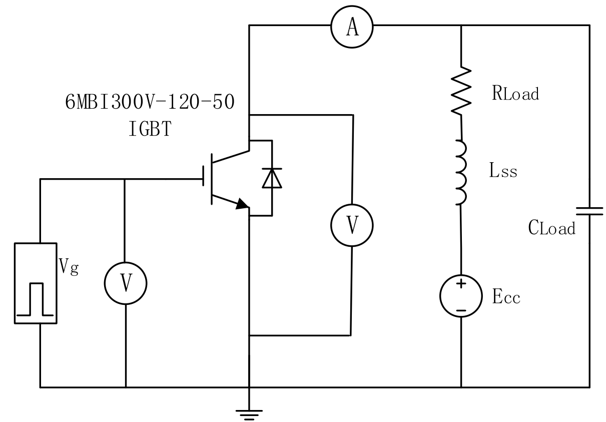

FIGURE 6. Experimental test platform simplified circuit diagram.

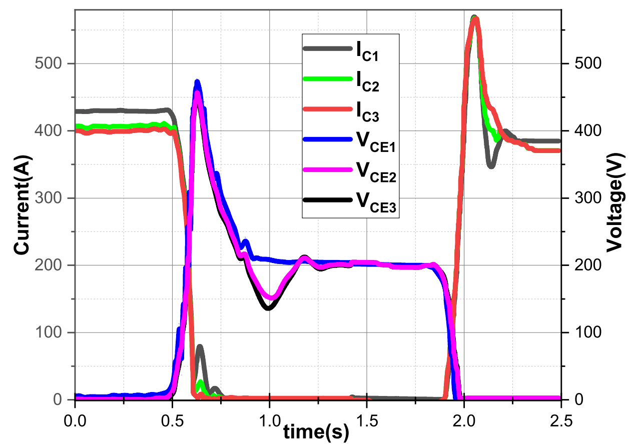

FIGURE 7. Dynamic voltage and current correction in 200V/400A.

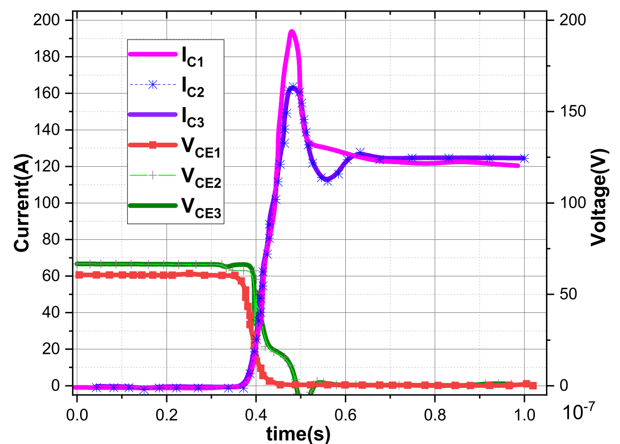

FIGURE 8. Dynamic voltage and current correction in 75V/150A.

tested, and the IGBT thermal resistance curve was calculated by voltage and current.

The experiment uses a 6MBI300V-120-50 IGBT with a rated voltage of 1200V and a rated current of 400A. Specific parameters can be found in the datasheet. The DC voltage source used can generate a DC voltage of up to 400V, using an oscilloscope with a range of 300V DC, isolated by a differential probe, and adjusted to reduce the 10X. And samples and analyzes the IGBT voltage and current through the host computer and DSP. Fig. 6 is a simplified circuit diagram of the experimental platform.

The experimental process is to let the IGBT work under a specific voltage condition by giving a pulse signal to V_g, and the pulse frequency is 10KHz. L ss is the coil inductance, and its value is 1uH. C_{Load} is a capacitive load, capacitor value selects 1mF capacitors in parallel. The load inductance(L ss) is 0.0023H, the load resistance is 2.5Ω. Ecc is the source voltage. The voltage(Ecc) and current test experiments in this paper select two working conditions: 200/400A and 75V/150A. Then compare the error relationship between the experimental data under two conditions. The experimental results are shown in Fig. 7 and Fig.8.

Fig.7 and Fig.8 are voltage and current waveforms under different operating conditions. I_{C1} is a simulation current that getting from the traditional model. I_{C2} is the current of improved simulation,I_{C3} is the current of the experiment. V_{CE1} is the simulated voltage of the traditional model. V_{CE2} is the voltage of improved simulation,V_{CE3} is the voltage of the experiment. The improved dynamic model greatly reduces power consumption errors. In this paper, the test experiments are carried out for different working conditions. When working at 75V/150A, the improved dynamic model is 5% higher

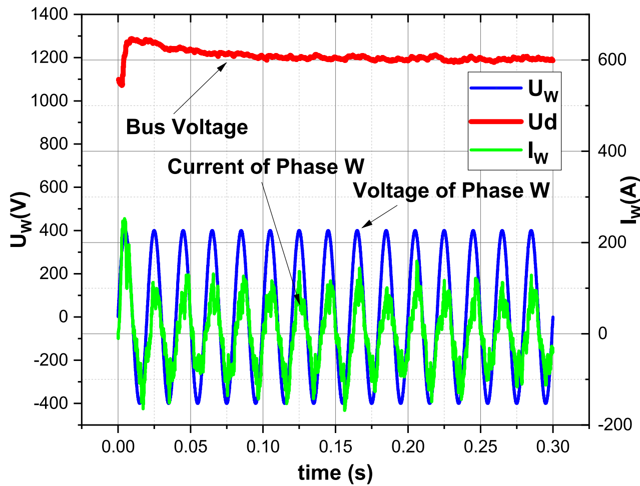

FIGURE 9. Voltage and current of phase W and voltage of DC bus.

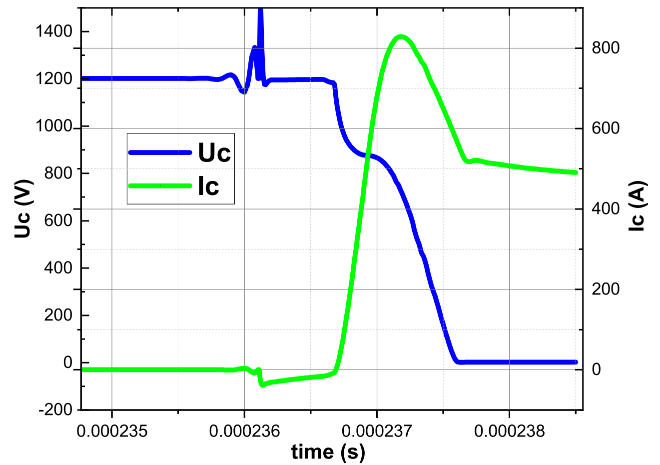

FIGURE 10. IGBT turn-on waveform.

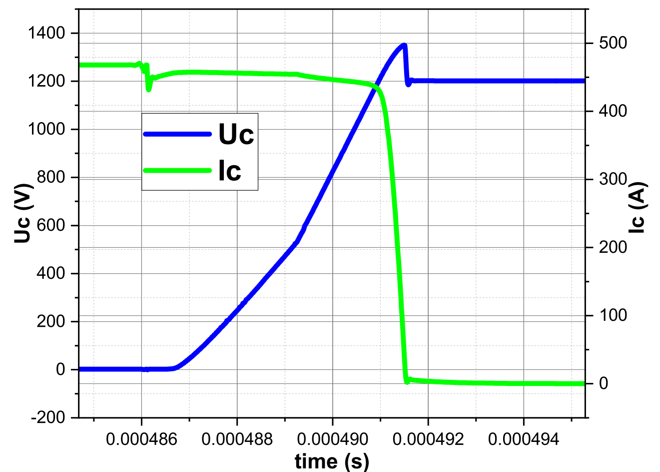

FIGURE 11. IGBT turn-off waveform.

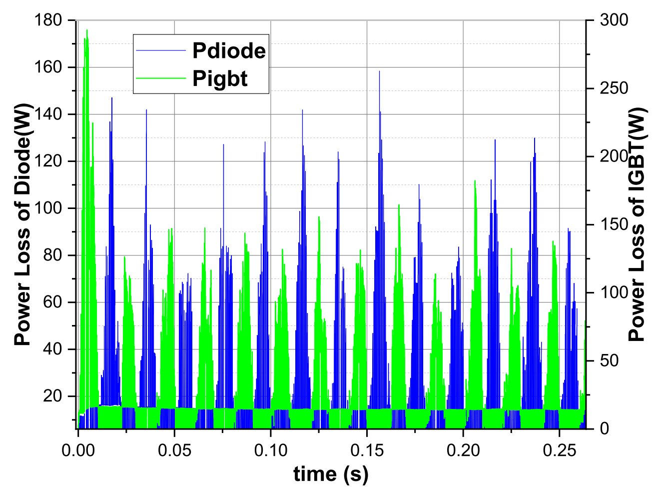

FIGURE 12. Power loss of IGBT and diode.

than the traditional model. At 200V/400A, the improved dynamic model is 8% better than the traditional model.

The simulation result waveform is shown in Fig. 9. The three-phase AC voltage has an amplitude of 400V and a current of 156A. Only the phase W waveform is given here. When the circuit starts to work, the capacitor will have a charging process, which will make the voltage rise rapidly and then gradually stabilize. Finally, the DC bus voltage stabilizes at 1200V. Fig.10 shows the IGBT turn-on process. This process is oscillating, resulting in large power consumption, where the integral of the voltage and current overlap is its power consumption. Fig.11 is the IGBT turn-off process. The power consumption calculation method is the same as the power-on process. Fig.12 is the heat power of the IGBT chip and the diode chip. The power consumption of the IGBT chip can reach 300W when the capacitor is charged. This process has an impact on the IGBT lifetime. The peak power of the diode chip is about 150W. The instantaneous power consumption of the IGBT chip and the diode chip can be integrated to obtain an average heating power of 108 W and 88.5 W. The heat flux of the IGBT chip and the diode chip is calculated by Equation (21) to be 9.36 W/mm^3 and 11.5 W/mm^3, respectively.

V. FINITE ELEMENT SIMULATION RESULT

A. DEVICE TEMPERATURE FIELD OF IGBT

The thermal simulation and experiment results are shown in Fig.13 $\sim$ Fig.17:

Due to the thermal coupling phenomenon, the temperature of the intermediate IGBT chip is higher than that of other IGBT chips. As shown in Fig. 14, the maximum temperature of the IGBT chip is 47 degrees, and there is almost no difference between the simulation results and test results. Fig.15 is the material temperature distribution curve of each layer of the device. It is shown that the diode temperature is about 5 °C higher than the IGBT chip temperature. The reason why the diode temperature is higher than the IGBT temperature is that the diode thermal resistance is greater than the IGBT thermal resistance. The temperature of the bottom surface of the chip is not much different from the surface temperature

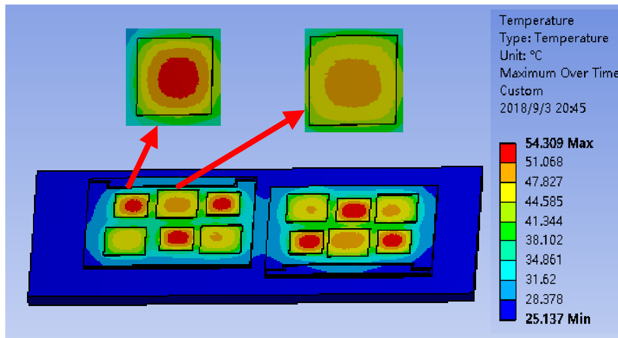

FIGURE 13. Device temperature profile.

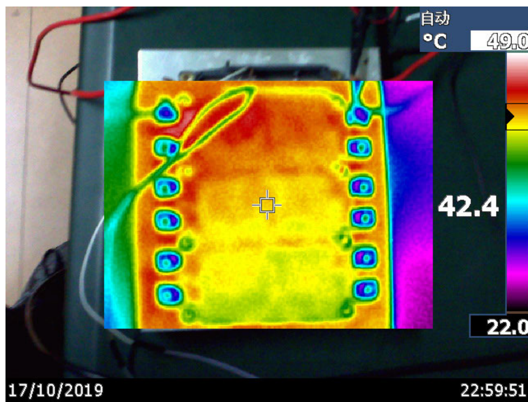

FIGURE 14. Device temperature profile.

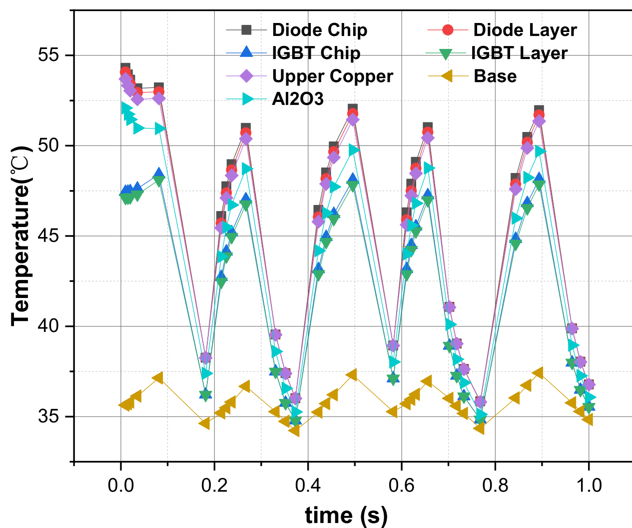

FIGURE 15. Device temperature profile of each layer.

of the solder layer, but the difference between the thermal expansion coefficient of the solder layer and the silicon chip is large, and the thermal cycle can cause large deformation of the solder layer. The temperature of the alumina ceramic substrate is about 6°C lower than the temperature of the upper layer of copper, and the thermal shock may cause the ceramic substrate to break. The temperature of the copper substrate is about 36 °C, close to the ambient temperature. Fig. 16 is a comparison of IGBT simulation temperature and experimental temperature. The analysis results show that the error between the simulation result and the experimental result is about 2 degrees, that is, the error is within 5%. Fig.17 shows the thermal resistance of different models, which are the data come from the standard test data are given in the datasheet, the improved dynamic model, improved Cauer model, the traditional Cauer model. It can be seen from the comparison results that the improved dynamic model has better accuracy than the traditional dynamic model and the improved Cauer model.

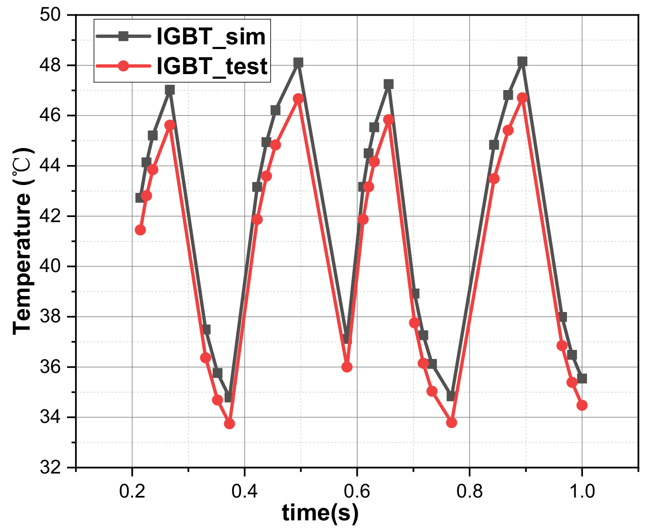

FIGURE 16. Simulation and experimental temperature comparison.

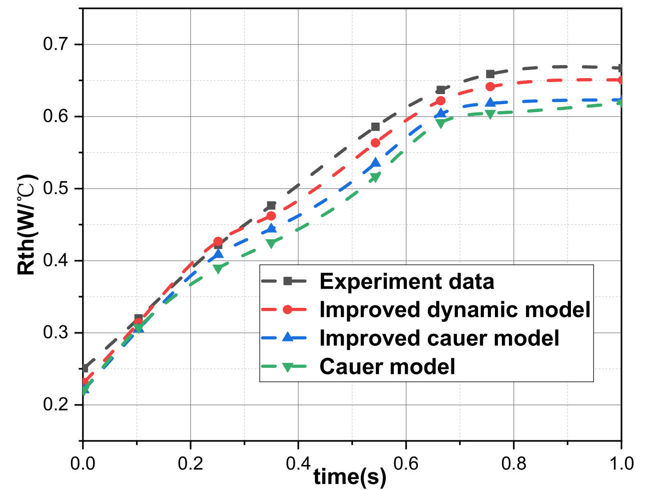

FIGURE 17. Comparison of thermal resistance results of different models.

B. IGBT STRESS DISTRIBUTION

Fig. 18 is the result of the finite element deformation analysis and Fig. 19 is the result of the stress analysis.

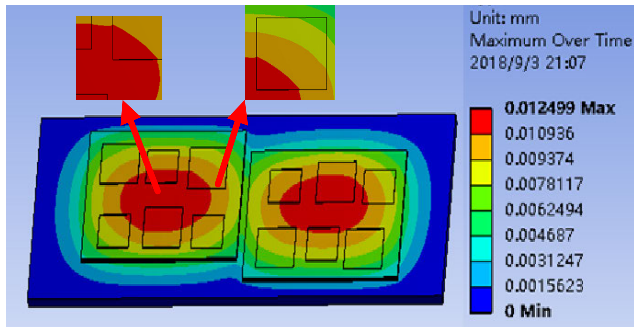

FIGURE 18. Total deformation of IGBT.

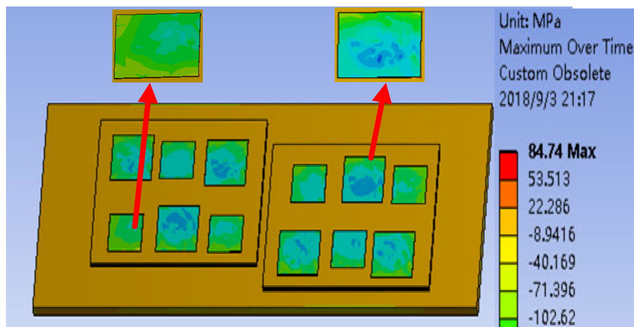

FIGURE 19. Chip solder layer stress distribution.

The deformation distribution is centered on the geometric center of the chipset and presents a circular distribution, wherein the center of the circle is up to $12.49\mu m$. The edge deformation of the device is minimal, close to $0\mu m$. When the device is subjected to large deformation changes, it may cause a breakage of brittle materials in the IGBT. In Fig.19, The maximum stress point is distributed at the edge of the device, and the minimum stress point is distributed in the center of the solder layer, and the stress becomes smaller from the edge to the center.

According to the above simulation results, IGBT holes are randomly generated in conjunction with JavaScript scripts to simulate the real condition of the solder layer, and the solder layer cracks of the same area and the solder layer peeling defects of the same area are set. Fig.20∼ Fig.24 shows the temperature curve and solder layer stress curve obtained by temperature field and stress field simulation.

It can be seen from Fig.20, the shape and size of the three defects are randomly generated by JavaScript. It is mentioned in the literature [7] that the shape of the void of the solder layer is generally circular or elliptical, the crack setting is the conclusion obtained by studying the crack formation process in [15]. Set the defect size to 0%∼20%, then analyze the solder layer temperature and stress.

In the presence of multi-field coupling, if there is a defect in the IGBT solder layer, the electric-thermal field distribution is mainly concentrated at the edge of the chip, as shown in Figure 21(b). Its maximum temperature is 170 degrees concentrated in the crack of the solder layer. the conventional

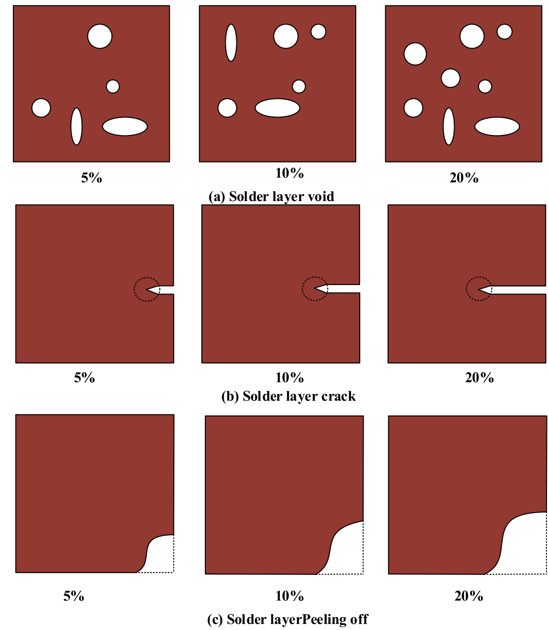

FIGURE 20. Random generation of solder layer defects by JavaScript.

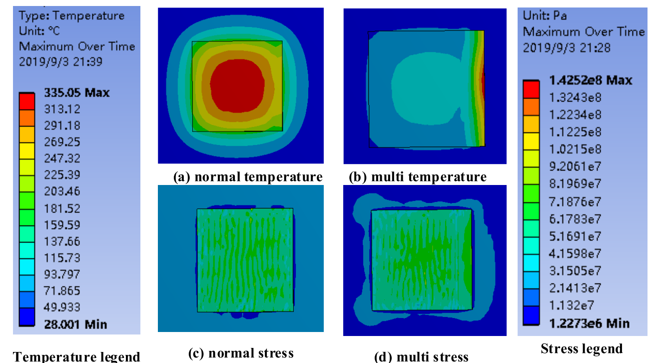

FIGURE 21. Coupling and traditional modeling of electro-thermal and electro-thermal-force field distribution.

analysis results are shown in Fig. 21 (a), the temperature is concentrated in the center of the solder layer, and the maximum temperature is 150 degrees. Multi-physics coupling results and traditional simulation results have large errors. In the electro-thermal-force coupled stress analysis, the stress is mainly distributed near the edge of the crack. But in the traditional stress analysis, the stress is evenly distributed, which is inconsistent with the actual theory. Therefore, the electro-thermal-force coupling analysis constructed under the dynamic model can better show the crack deposit, which has a better effect on the positioning and reduction of the solder layer defects.

It can be seen from Fig. 22 that as the crack length of the solder layer increases, the force of the coupled field increases, and the longer the crack, the more obvious the coupling effect of electro-thermal-force. When the crack reaches 40%, the entire stress is concentrated on the edge of the solder

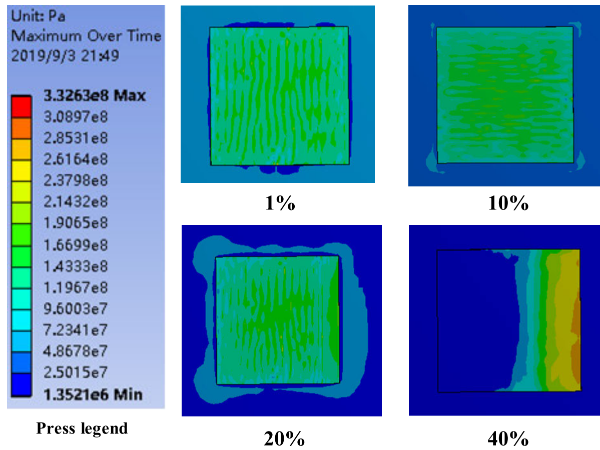

FIGURE 22. Analysis of coupled stresses with different crack lengths.

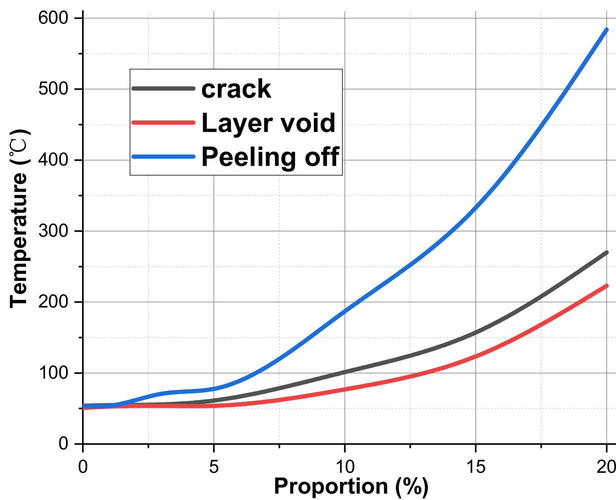

FIGURE 23. Chip temperature profile of different solder layer defects.

layer. Traditional stress analysis does not yield the final stress results.

It can be seen from Fig. 23 and Fig.24, when the proportion of voids and cracks in the solder layer is less than 15%, the effect of crack on the junction temperature of the chip is greater than that of the cavity. After the ratio is greater than 15%, the effect of the cavity on the junction temperature increases rapidly. The effect of the solder layer shedding on the junction temperature is exponentially distributed. The effect of the solder layer shedding on junction temperature is more serious than voids and cracks. At the same time, the solder layer peeling off will cause the chip temperature to concentrate on the falling area, resulting in device failure. When the defect area reaches 15% of the total area of the solder layer, the stress increase 150MPa because of the falling off of the solder layer, the stress increase 30MPa because of the void of the solder layer, and the stress increase caused by the solder layer crack is about 80MPa. When the solder layer defect is small, it is not enough to cause device failure. From the simulation results, it is known that the solder layer

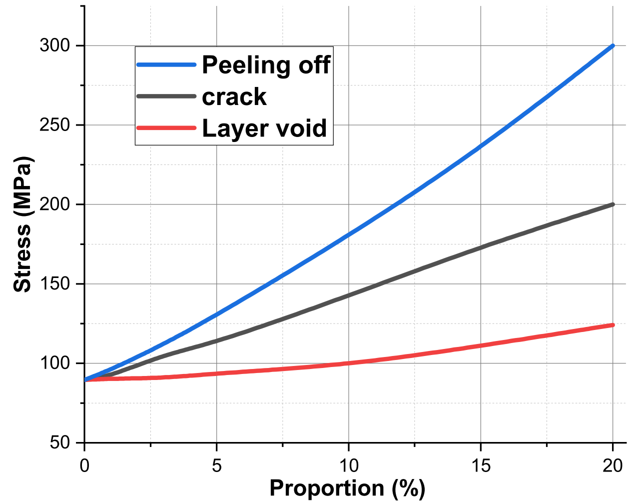

FIGURE 24. Curve of solder layer stress and chip temperature.

peeling has the greatest influence on the device, followed by the solder layer crack, and the least affected is the solder layer void.

VI. CONCLUSION

This paper creates an IGBT dynamic model, and improves the accuracy of power simulation by optimizing the dynamic model parameters, and constructs the IGBT electro-thermal-force multiphysics coupling model using the dynamic model. At the same time, the experimental results show that the dynamic model can greatly reduce power calculation error and improve simulation accuracy. Studying the finite element simulation results, among the three defects, the solder layer shedding has the greatest influence on temperature. The solder layer crack has a greater influence on the chip temperature than the void. After the solder layer defect exceeds a certain ratio, the effect on temperature is significantly increased. Under the same defect area, the solder layer shedding has the greatest influence on the chip stress, followed by the crack, and the least affected is the cavity. During the chip factory process, the voids are strictly controlled by the quality inspection. In this regard, the cracking and detachment of the solder layer should be taken seriously during the use of the IGBT.

REFERENCES

[1] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "*In situ* diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.

[2] L. Wang, J. Xu, G. Wang, and Z. Zhang, "Lifetime estimation of IGBT modules for MMC-HVDC application," *Microelectron. Rel.*, vol. 82, pp. 90–99, Mar. 2018.

[3] W. Zhihong, S. Xiezu, and Z. Yuan, "IGBT junction and coolant temperature estimation by thermal model," *Microelectron. Rel.*, vol. 87, pp. 168–182, Aug. 2018.

[4] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, "Overview of electric motor technologies used for more electric aircraft (MEA)," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3523–3531, Sep. 2012.

[5] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, ''Power capability investigation based on electrothermal models of press-pack IGBT three-level NPC and ANPC VSCs for multimegawatt wind turbines,'' *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3195–3206, Jul. 2012.

[6] G. Sonnenfeld, K. Goebel, and J. R. Celaya, ''An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors,'' in *Proc. IEEE Autotestcon*, Sep. 2008, pp. 208–215.

[7] W. Lai, M. Chen, L. Ran, S. Xu, H. Qin, O. Alatise, and P. A. Mawby, ''Study on the lifetime characteristics of power modules under power cycling conditions,'' *IET Power Electron.*, vol. 9, no. 5, pp. 1045–1052, Mar. 2015.

[8] X. Gong and J. A. Ferreira, ''Comparison and reduction of conducted EMI in SiC JFET and Si IGBT-based motor drives,'' *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1757–1767, Apr. 2014.

[9] V. Székely and M. Rencz, ''Thermal dynamics and the time constant domain,'' *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 23, no. 3, pp. 587–594, Sep. 2000.

[10] A. Bryant, N.-A. Parker-Allotey, D. Hamilton, I. Swan, P. A. Mawby, T. Ueta, T. Nishijima, and K. Hamada, ''A fast loss and temperature simulation method for power converters, Part I: Electrothermal modeling and validation,'' *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 248–257, Jan. 2012.

[11] T. K. Gachovska, B. Tian, L. Jerry, and A. Hudgins, ''A real-time thermal model for monitoring of power semiconductor devices,'' *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3361–3367, Jan. 2015.

[12] I. Swan, A. Bryant, P. A. Mawby, T. Ueta, T. Nishijima, and K. Hamada, ''A fast loss and temperature simulation method for power converters, Part II: 3-D thermal model of power module,'' *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 258–268, May 2011.

[13] R. Wu, H. Wang, K. B. Pedersen, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, ''A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations,'' *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3304–3314, Mar. 2015.

[14] Z. Wang, B. Tian, W. Qiao, and L. Qu, ''Real-time aging monitoring for IGBT modules using case temperature,'' *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1168–1178, Feb. 2016.

[15] W. Lai, M. Chen, L. Ran, S. Xu, N. Jiang, X. Wang, O. Alatise, and P. Mawby, ''Experimental investigation on the effects of narrow junction temperature cycles on die-attach solder layer in an IGBT module,'' *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1431–1441, Feb. 2017.

[16] B. Du, J. L. Hudgins, E. Santi, A. T. Bryant, P. R. Palmer, and H. A. Mantooth, ''Transient electrothermal simulation of power semiconductor devices,'' *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 237–248, Jan. 2010.

[17] U.-M. Choi, K. Ma, and F. Blaabjerg, ''Validation of lifetime prediction of IGBT modules based on linear damage accumulation by means of superimposed power cycling tests,'' *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3520–3529, Apr. 2018.

[18] H. Daou, M. Ameziani, and D. Lhotellier, ''Dynamic electric model for IGBT power module based on Q3D and Simplorer: 3D layout design, stray inductance estimation, experimental verifications,'' in *Proc. IEEE Elect. Syst. Conf.*, Nov. 2016, pp. 1–8.

[19] X. Wang, C. Zhu, H. Luo, Z. Lu, W. Li, X. He, J. Ma, G. Chen, Y. Tian, and E. Yang, ''IGBT junction temperature measurement via combined TSEPs with collector current impact elimination,'' in *Proc. IEEE Energy Convers. Cong. Exp. (ECCE)*, Sep. 2016, pp. 1–6.

[20] C. Qian, A. M. Gheitaghy, J. Fan, H. Tang, B. Sun, H. Ye, and G. Zhang, ''Thermal management on IGBT power electronic devices and modules,'' *IEEE Access*, vol. 6, pp. 12868–12884, 2018.

[21] M. Warwel, G. Wittler, M. Hirsch, and H.-C. Reuss, ''Real-time thermal monitoring of power semiconductors in power electronics using linear parameter-varying models for variable coolant flow situations,'' in *Proc. Workshop Control Power Electron.*, Jun. 2014, pp. 1–6.

[22] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. New York, NY, USA: Wiley, 1995.

[23] A. S. Bahman, K. Ma, and F. Blaabjerg, ''A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.

[24] K. Ma, U. M. Choi, and F. B. Gae, ''Prediction and validation of cumulative distribution function for power semiconductor devices with mission profiles in motor drive application,'' *IEEE Trans. Power Electron.*, to be published.

[25] Z. Wang, W. Qiao, B. Tian, and L. Qu, ''An effective heat propagation path-based online adaptive thermal model for IGBT modules,'' in *Proc. IEEE Appl. Power Elect. Conf. Expo.*, Mar. 2014, pp. 513–518.

[26] Z. Wang and W. Qiao, ''A physics-based improved cauer-type thermal equivalent circuit for IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6781–6786, 2016.

[27] K. Ma, N. He, M. Liserre, and F. Blaabjerg, ''Frequency-domain thermal modeling and characterization of power semiconductor devices,'' *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7183–7193, Dec. 2015.

[28] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen, and B. Rannestad, ''Reliability improvement of power converters by means of condition monitoring of IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7990–7997, Dec. 2016.

[29] J. Zhou, Y. He, J. Liu, W. Yuan, H. Ni, and Z. Peng, ''Improved IGBT dynamic model and electro-thermal-mechanical multi-field coupling failure analysis,'' in *Proc. Symp. Power Electron. Distrib. Gener. Conf.*, May 2019, pp. 827–832.

[30] C. Batard, N. Ginot, and J. Antonios, ''Lumped dynamic electrothermal model of IGBT module of inverters,'' *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 3, pp. 355–364, Feb. 2018.

JIANBO ZHOU received the B.Sc. degree from the Wuhan University of Science and Technology, in 2017. He is currently pursuing the M.Sc. degree with the Hefei University of Technology. His main research interests include power electronics reliability, as well as reliability evaluation of high power and high voltage power electronics.

BING LI received the M.Sc. and Ph.D. degrees from Hunan University, in 2006 and 2010, respectively. He is currently an Associate Professor with the Hefei University of Technology. His main research interests include WSN and RFID.

YIGANG HE received the M.Sc. degree from Hunan University, in 1992, and the Ph.D. degree from Xi'an Jiaotong University, in 1996. He is currently a Professor and the Dean of the School of Electrical Engineering and Automation, Hefei University of Technology. His research interests are in the areas of circuit theory and its applications, testing and fault diagnosis of analog and mixed-signal circuits, smart grid, radio frequency identification technology, and intelligent signal processing. He is the winner of the National Distinguished Young Scientists Foundation.

WEIBO YUAN received the B.Sc. degree from the Hefei University of Technology, in 2017, where he is currently pursuing the Ph.D. degree. His main research interests include electro-thermo-mechanical modeling and reliability of power semiconductor devices, high voltage and insulation thermo-mechanical modeling, and reliability of power semiconductor devices, as well as high voltage and insulation.

JIACHENG LIU received the B.E. degree from Ningxia University, in 2017. He is currently pursuing the M.Sc. degree with the Hefei University of Technology. His main research interests include power electronics reliability, and reliability evaluation of high power and high voltage power electronics.

HUADONG NI received the B.Sc. degree from Huangshan University, in 2016. He is currently pursuing the M.Sc. degree with the Hefei University of Technology. His main research interest includes power electronics reliability.