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Source/Drain Patterning FinFETs as Solution for Physical Area Scaling Toward 5-nm Node

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ABSTRACT A novel and feasible process scheme to downsize the source/drain (S/D) epitaxy of 5-nm node bulk fin-shaped field-effect transistors (FinFETs) were introduced by using fully-calibrated TCAD for the first time. The S/D epitaxy formed by selective epitaxial growth was diamond-shaped and occupied a large proportion of the device size irrespective of the active channel area. However, this problem was solved by patterning the low-k regions prior to S/D formation by preventing the lateral overgrowth of S/D epitaxy; the so-called S/D patterning (SDP). Its smaller S/D epitaxy decreased the average longitudinal channel stresses and drive currents for NFETs. However, the small diffusions of the boron dopants into the channel regions improved the short-channel effects and alleviated the drive current reduction for PFETs. Gate capacitances decreased greatly by reducing outer-fringing capacitances between the metal-gate stack and S/D regions. Through SPICE simulation based on the virtual source model, operation frequencies and dynamic powers of 15-stage ring oscillators were studied. SDP FinFETs have better circuit performances than the conventional and bottom oxide bulk FinFETs along with smaller active areas, promising for further area scaling through simple and reliable S/D process.

INDEX TERMS 5-nm node, source/drain patterning, FinFETs, longitudinal channel stress, ring oscillator, performance-power-area.

I. INTRODUCTION

Si fin-shaped field-effect transistors (FinFETs) have been scaled down to 10-nm node [1] by optimizing fin channels and layouts to increase the gate-to-channel controllability and device density, respectively. However, there are technical difficulties in scaling down of FinFETs. A thinner and taller fin is required to maintain good electrostatics below 10-nm node, but suffers from fin bending [2], smaller carrier mobility [3], and process difficulty [4]. A heavy punch-through-stopper (PTS) doping is also needed to reduce the sub-fin leakage of bulk FinFETs, but degrades the carrier mobility [5] and induces performance variations [6].

Meanwhile, a bottom oxide (BO) scheme is introduced to minimize the sub-fin leakage without PTS doping [7]. Bottom oxide below the source/drain (S/D) epi improves the short channel effects (SCEs) and decreases the gate capacitances (C_{gg}) due to the small S/D epi. However, some novel process scheme is still required to scale down the device area, limited in scaling by the minimum features of the contacted poly-pitch (CPP) of 42 nm and fin pitch (FP) of 21 nm by self-aligned quadruple patterning [8]. Large S/D epi formed by selective epitaxial growth (SEG) also constrains the scaling of FinFETs due to the risk of epi merging [9]. Furthermore, wrap-around contact (WAC), which reduces parasitic resistances (R_{sd}) effectively by increasing S/D contact area [10], requires more space between the S/D epi. Metal S/D structure has also been introduced to reduce R_{sd} greatly [11], but the large S/D epi still limits area scaling.

Thus, a simple and feasible process scheme downsizing S/D epi is proposed by using a fully-calibrated TCAD. DC/AC performances of all the bulk and proposed FinFETs were analyzed thoroughly in 5-nm technology node geometries.

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II. DEVICE STRUCTURE AND SIMULATION METHOD

All the bulk FinFETs were simulated by using Sentaurus TCAD [12]. Drift-diffusion transport model, Poisson equation and carrier continuity equations were calculated self-consistently. A density-gradient model was used to consider the quantum confinements at the fin channels. Mobility, generation-recombination and deformation potential models were equivalently used as in [7], [13].

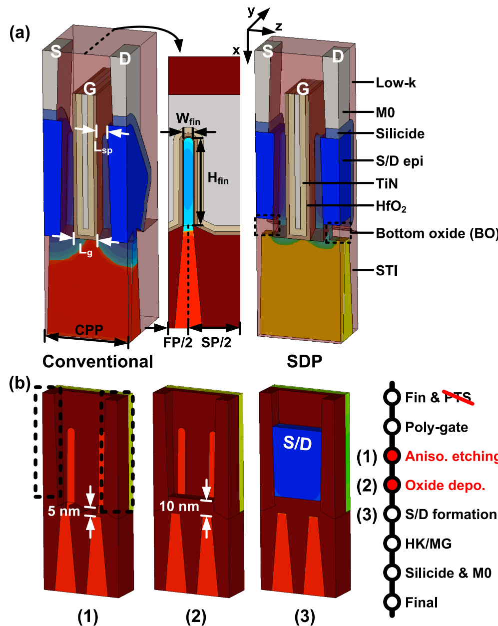

FIGURE 1. (a) 3-D schematic diagrams of conventional and source/drain patterning (SDP) FinFETs along with bottom oxide and (b) three key process steps for SDP FinFETs.

Fig. 1a shows the schematic diagrams of the conventional and S/D patterning (SDP) FinFETs along with the BO layer. Key geometrical parameters and material compositions are also denoted. Conventional and BO FinFETs have the diamond-shaped S/D epi with over-etching depth of 5 nm [7], whereas the proposed SDP FinFETs have a rectangular S/D epi occupying a smaller device area. All the FinFETs adopted WAC, and contact resistivity at the NiSi interface was $1\times10^{-9}\Omega\cdot\text{cm}^2$ [14]. Fig. 1b shows three key process steps of SDP FinFETs. Due to the presence of BO, PTS doping is not performed for both the BO and SDP FinFETs, whereas conventional FinFETs have PTS doping at 2×10^{18} cm^{-3} to prevent the sub-fin leakage [13]. The SDP scheme is patterning low-k regions under the anisotropic etching prior to the BO deposition and S/D formation to prevent lateral overgrowth of S/D epi. There is only one additional mask required to pattern low-k regions, and all other process steps are compatible to the current CMOS technology.

Table 1 shows the geometrical parameters and values of all the FinFETs. The CPP and FP for each technology nodes are referred from [1], [8] and [9]. Gate length (L_g) and spacer length (L_{sp}) were scaled down to 12 and 5 nm in the 5-nm node, respectively [15]. Fin width (W_{fin}) and height (H_{fin}) were the same as 5 and 46 nm, respectively, regardless of the device structure in the 5-nm node. W_{fin} values were chosen to minimize the RC delay of both the P- and NFETs for each technology nodes. The H_{fin} was fixed to 46 nm because it varied from the drain currents (I_{ds}) and C_{gg} simultaneously. Therefore, not affecting the RC delay of the devices [13]. The separation length (SP) was slightly scaled down from 58 to 56 nm to prevent the S/D epi merging between the P- and NFETs in the 5-nm node. However, SDP FinFETs can decrease the SP effectively down to 29 nm. The S/D epi was formed by crystallographic deposition with different growth rates in <100>, <110> and <111> crystal directions each [7]. Equivalent oxide thickness was fixed to 1.0 nm, and the dielectric constant of low-k spacer was 5.0.

TABLE 1. Geometrical parameters of the bulk FinFETs in three different technology nodes.

Geometrical Parameters		Conventional 10-nm	Conventional 7-nm	Conventional 5-nm	BO 5-nm	SDP 5-nm
CPP	Contacted poly pitch	54	48	42	42	42
FP	Fin pitch	34	26	21	21	21
SP	Separation length	58	58	56	56	29
L_g	Gate length	18	15	12	12	12
L_{sp}	Spacer length	7	6	5	5	5
L_{sd}	S/D length	22	21	20	20	20
W_{fin}	Fin width	7	6	5	5	5
H_{fin}	Fin height	46	46	46	46	46

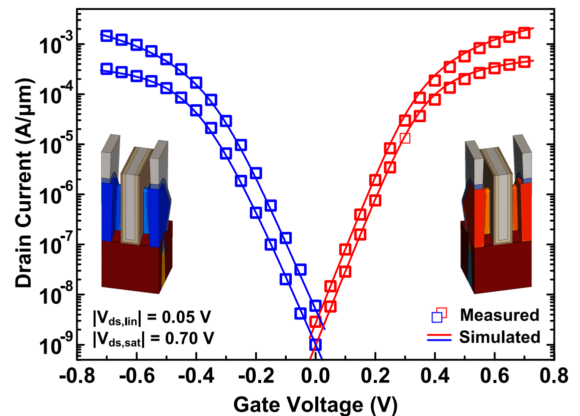

FIGURE 2. TCAD simulations (lines) calibrated to the 10-nm node FinFETs (symbol) [1].

Fig. 2 shows the TCAD results calibrated to the Intel's 10-nm node FinFETs [1]. Subthreshold swing (SS) and drain-induced barrier lowering (DIBL) were fitted first by changing the S/D doping profiles. Ballistic coefficient and surface roughness scattering factors were tuned to fit the I_{ds} in the linear regime. Then, the saturation velocity was tuned to fit the I_{ds} in the saturation regime.

The threshold voltage (V_{th}) was extracted by using the constant current method at $10^{-7}\times W_{eff}/L_g$ where W_{eff} is the

effective width as $N_{fin} \times (W_{fin} + 2 \times (H_{fin} - T_{bo}))$, N_{fin} is the number of fins, and T_{bo} is the BO thickness above the bottom fin (5 nm) for BO and SDP devices. SS was extracted below the V_{th} in the saturation regime, and DIBL was extracted from the V_{th} difference at the drain voltages (V_{ds}) of 0.05 and 0.7 V.

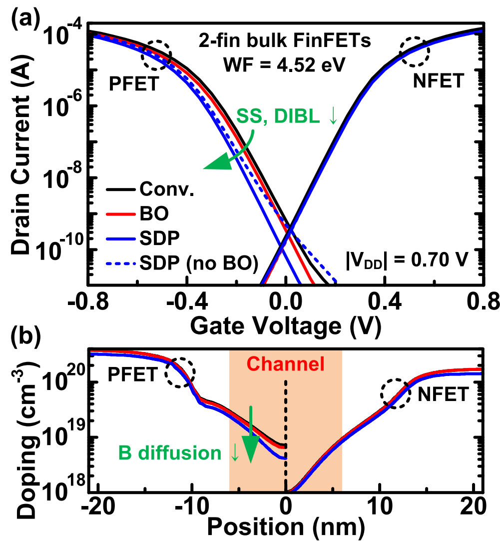

FIGURE 3. (a) Transfer curves of conventional, BO, and SDP FinFETs and (b) their S/D doping profiles at the middle of fins.

III. RESULTS AND DISCUSSION

Fig. 3a shows the transfer characteristics of three different 2-fin bulk FinFETs at the operation voltage (V_{DD}) of 0.7 V with the same work function of 4.52 eV. As the device advanced to BO and SDP, both the SS and DIBL decreased, and the V_{th} increased for PFETs, whereas similar SCEs are shown for NFETs. This effect is explained by S/D doping profiles (Fig. 3b). The doping profiles of the NFETs were not significantly changed. However, smaller amounts of boron dopants diffuse into the active channel regions for the p-type SDP FinFETs, which improved the SCEs. SDP FinFETs without BO are also included in Fig. 3a, showing that the PFETs suffer from the punch-through effect at the bottom fin. Greater PTS doping is required to minimize the effect, but the performance variations increase by random dopant fluctuation (RDF) [7].

As the device advanced to BO or SDP, longitudinal channel stresses (S_{ZZ}) near the S/D epi increased (Fig. 4a). The increase of compressive stress retards boron dopants diffusing into the channels [16]. Moreover, the SDP FinFETs had the shrunk S/D epi containing smaller amounts of boron dopants, thus much abrupt S/D doping profiles were obtained. However, SDP FinFETs without BO had smaller S_{ZZ} near the S/D epi at the bottom, thus increasing boron diffusions into the bottom fin and sub-fin leakage currents. On the other hand, phosphorus dopants for NFETs were not affected by the S_{ZZ} near the S/D epi [16]. Therefore, the same S/D doping profiles were obtained (Fig. 3b). Thus, all the NFETs have similar SCEs irrespective of the device structure. Fig. 4c compares

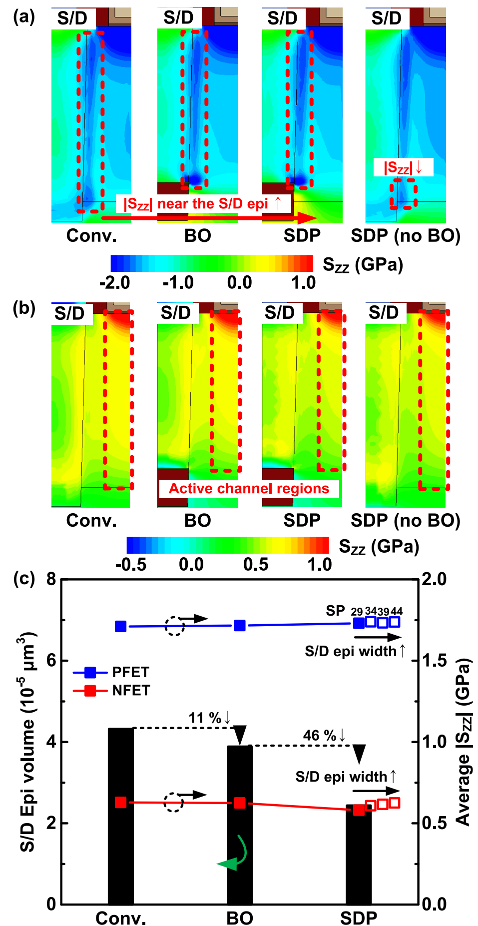

FIGURE 4. 2-D stress profiles of the (a) PFETs and (b) NFETs and (c) S/D epi volume (left) and average longitudinal channel stresses ($|S_{ZZ}|$) (right) of all the FinFETs. $|S_{ZZ}|$ of the SDP FinFETs with different S/D epi widths are also specified.

the S/D epi size and the $|S_{ZZ}|$ obtained by averaging the active channel regions (= average $|S_{ZZ}|$) indicated in Fig. 4b. BO scheme prevented the SEG above the PTS region, which downsized the S/D epi by 11 %. On the other hand, the SDP scheme shrunk it further by 46 %. The average S_{ZZ} of the SDP NFETs decreased by 7.5 %, whereas the average S_{ZZ} of the SDP PFETs were almost constant. It was studied that the shorter S/D length under the same L_g and L_{sp} reduced the $|S_{ZZ}|$ significantly [11], [17]. However, the S/D epi width affected the $|S_{ZZ}|$ of P- and NFETs differently (Fig. 4c); larger S/D epi width increased the $|S_{ZZ}|$ for NFETs, but does not affect the $|S_{ZZ}|$ for PFETs.

Effective currents (I_{eff}) of all the FinFETs are shown in Fig. 5. I_{eff} are calculated by using [18] and used for the DC performance metrics. Off-state currents (I_{off}) were fixed to 0.1 and 10 nA for low-power (LP) and high-performance (HP) applications, respectively, by shifting the transfer curves in Fig. 3a. The I_{eff} of PFETs for LP application increased as the device advanced to BO and SDP, whereas those of NFETs decreased. PFETs decrease the SS and DIBL as the SDP scheme is adopted by decreasing boron diffusion into the channel (Fig. 3b), and it is

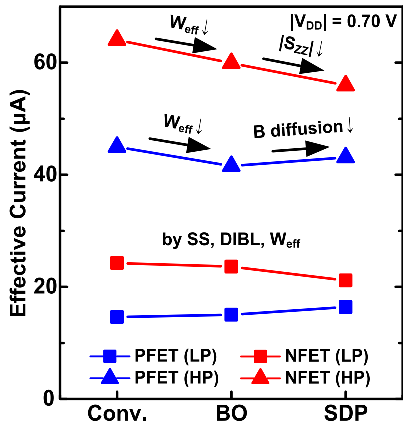

FIGURE 5. Effective currents (I_{eff}) of all the FinFETs for LP (I_{off} = 0.1 nA) and HP (I_{off} = 10 nA) applications.

reflected to the I_{eff} increase. On the other hand, the SCEs of NFETs were almost constant. Instead, the presence of BO and SDP decreased the W_{eff} and average $|S_{ZZ}|$, respectively, and affected the I_{eff} reduction. The I_{eff} of PFETs were also degraded by smaller W_{eff} for HP application, but slightly by the improved SCEs. In summary, the SDP structure does not help to increase the DC performances.

DC performance variations of all the FinFETs were analyzed in terms of RDF and work-function variation (WFV) through statistical impedance field method. The number of randomized devices was 10,000 for RDF and WFV each. All the dopants of P- and NFETs were randomized for the RDF, whereas the WF was randomized as a number of 5-nm-size grains having the WF values of 4.6 and 4.4 eV with probabilities of 60 and 40 %, respectively [7], [19].

TABLE 2. DC performance variations of 5-nm node conventional, BO, and SDP FinFETs by RDF and WFV.

SP application (I_{off} = 1 nA)		PFETs			NFETs		
		Conv.	BO	SDP	Conv.	BO	SDP
σV_{th} (mV)	RDF	24.2	24.4	19.8	14.4	14.1	15.3
	WFV	12.8	13.3	12.7	11.1	11.5	11.4
σI_{on} (%)	RDF	6.16	6.37	5.47	4.78	4.82	5.00
	WFV	3.83	3.90	3.64	3.37	3.35	3.32
σI_{off} (nA)	RDF	2.75	0.893	0.704	1.30	0.795	1.48
	WFV	0.823	0.428	0.410	0.332	0.357	0.333

Table 2 shows the DC performance variations of all the 5-nm node FinFETs for standard performance application (I_{off} = 1 nA). On-state current (I_{on}) variations were calculated as the standard deviations divided by the averages. Generally, RDF induces greater DC performance variations than does WFV. As the technology node is scaled down to 5 nm node, shorter L_{sp} increases the number of S/D dopants diffusing into the channels and thus the RDF-induced variations become larger [20]. In the meantime, the SDP PFETs alleviate the RDF-induced variations by decreasing boron diffusions into the channels (Fig. 3b). WFV induces similar DC performance variations of all the devices. The conventional PFETs have larger I_{off} variations by RDF or WFV because some devices lose the controllability at the bottom fin where the sub-fin leakage current flows.

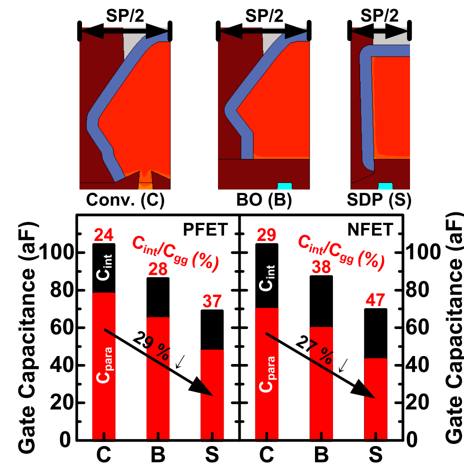

FIGURE 6. S/D epi size (top) and gate capacitances (C_{gg}) and parasitic capacitances (C_{para}) (bottom) of all the FinFETs.

However, SDP FinFETs show the outstanding capacitive performances (Fig. 6). C_{gg} were extracted at the gate voltages (V_{gs}) and V_{ds} of V_{DD}, whereas parasitic capacitances (C_{para}) were extracted at the off state. The BO and SDP schemes effectively reduce the C_{gg} and C_{para} due to the shrunk S/D epi. PFETs have additional C_{para} decrease due to the decrease of doping concentrations at the S/D extensions [21]. Especially, SDP FinFETs have the ratio of intrinsic capacitance (C_{int}) out of C_{gg} by 37 and 47 % for P- and NFETs, respectively.

Fig. 7 summarizes the CMOS inverter area of all the FinFETs. The CMOS inverter area was calculated by adding the active areas of P- and NFETs as 2×(SP+FP)×CPP. Conventional and BO FinFETs have the same CMOS inverter area in the 5-nm node, whereas the SDP FinFETs reduce the inverter area by 43% through greatly scaling down the SP.

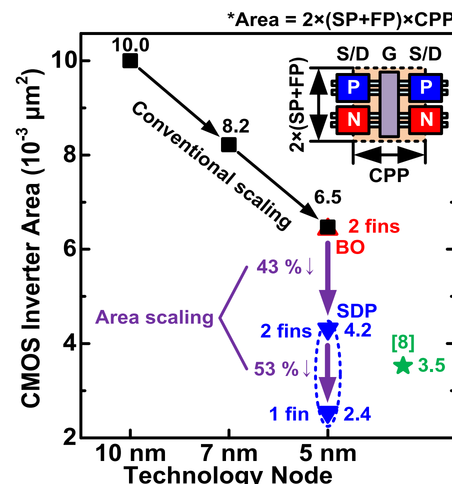

FIGURE 7. CMOS Inverter area of all the FinFETs. The area of complementary FETs was also included for comparison [8].

As a single fin was used, the inverter area decreased greatly by 53 % compared to 2-fin SDP FinFETs. CMOS inverter area of complementary FETs (CFETs) is also shown for comparison [8]. Among all, the 1-fin SDP FinFETs occupy the smallest inverter area.

TABLE 3. Virtual source parameters of the bulk FinFETs in 5-nm technology node.

Parameters	Conventional		BO		SDP	
	P	N	P	N	P	N
C_{inv} (μF/cm^2)	3.72	3.63	3.94	3.89	3.07	3.09
SS (mV/dec)	79.9	71.3	79.2	70.7	75.0	70.8
DIBL (mV/V)	90.5	67.2	84.8	62.3	75.0	65.0
$W_{eff} \cdot R_s$ (Ω·μm)	150	102	150	102	151	104
μ (cm^2/(V·s))	42.1	63.3	40.8	55.8	50.9	65.0
v_{sat} (10^7 cm/s)	0.71	0.71	0.67	0.67	0.78	0.77

Virtual source modeling was performed to analyze the intrinsic device performances quantitatively [22]. Virtual source parameters of all the FinFETs in the 5-nm technology node are summarized in Table 3. Gate-to-channel inversion capacitances per unit area (C_{inv}) were extracted by using linear extrapolation of Q-V curves [23]. Smoothness parameters (α, β) of virtual source modeling were fixed at 2.7 and 2.3, respectively, for all the devices to compare the physical parameters accurately. SS, DIBL, source-side resistance ($R_s = R_{sd}/2$), carrier mobility (μ) and saturation velocity (v_{sat}) were used as fitting parameters. Virtual source modeling accurately describes the transfer curves of all the FinFETs at the $|V_{ds}|$ of 0.05, 0.35, and 0.70 V (not shown). Both μ and v_{sat} increased greatly for SDP FinFETs due to the C_{inv} decrease by small diffusions of S/D dopants into the channels.

Using the virtual source parameters, 15-stage ring oscillators (fan-out = 3) have been simulated using HSPICE for standard performance application (I_{off} = 1 nA) (Fig. 8). Interconnect resistance and capacitance per wire length are from [7], [9], and wire length was simply assumed as 25×CPP+3.33×CH, where the CH is a cell height as 2×(SP+FP) [8]. Conventional FinFETs in three different technology nodes have similar circuit performances, but the device area is shrunk by decreasing CPP and FP. Under the same N_{fin} of 2, BO FinFETs show similar performances as 5-nm node conventional FinFETs at small V_{DD}. However, their small W_{eff} decreases the current drivability. SDP FinFETs not only take smaller area, but also outperform conventional and BO FinFETs in spite of their small W_{eff} because all the capacitive elements in the front-end and interconnect decrease critically. SDP FinFETs (N_{fin} = 1) have similar circuit performances as conventional and BO FinFETs, but the device area is scaled down aggressively.

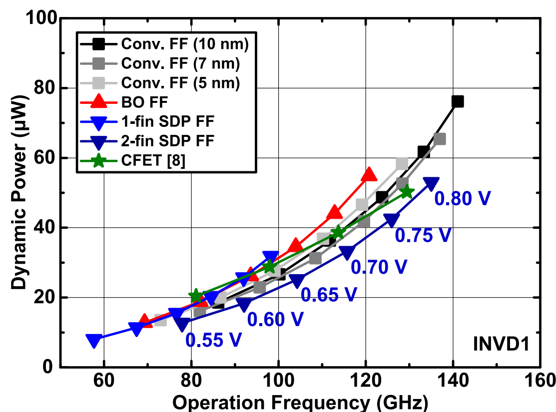

FIGURE 8. Dynamic power and frequency of 15-stage ring oscillators (fan-out = 3) for all the FinFETs at V_{DD} from 0.55 to 0.80 V. CFETs (L_g = 12 nm, L_{sp} = 7 nm, L_{ov} 10 %) are also included for comparison at V_{DD} from 0.65 to 0.80 V [8].

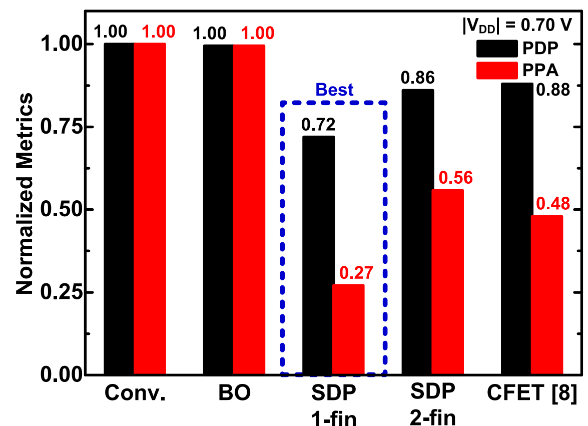

FIGURE 9. Power-delay product (PDP) and performance-power-area (PPA = PDP × inverter area) of all the FinFETs at the V_{DD} of 0.70 V. 1-fin SDP FinFETs have the smallest PDP and PPA among all the FinFETs.

Power-delay product (PDP) and performance-power-area (PPA = PDP × inverter area) normalized by 5-nm node conventional FinFETs at the V_{DD} of 0.70 V are shown in Fig. 9. PDP was calculated by the dynamic power divided by the operation frequency. Conventional and BO FinFETs have almost the same performance, but the absence of PTS for BO scheme is immune to RDF [7]. CFETs have superior PPA than 2-fin SDP FinFETs, but the 1-fin SDP FinFETs outperform the CFETs and all the FinFETs by critical device scaling. Thus, the SDP technique is capable of extending Si-FinFETs toward sub-5-nm node.

IV. CONCLUSION

5-nm node SDP FinFETs were presented and analyzed by using fully-calibrated TCAD. The patterned low-k regions resized the S/D epi under the SEG so as to enable the SP scaling. The shrunk S/D epi along with high $|S_{ZZ}|$ near the S/D epi retarded the diffusion of boron dopants into the channels, improving the SCEs for PFETs. In addition, this shrunk S/D epi decreases the C_{para} and C_{gg} greatly, thus improving circuit performances of 15-stage ring oscillators. Compared to all the FinFETs and CFETs, SDP FinFETs are promising to attain smaller PDP, smaller device area and scalability down to the future technology nodes through feasible and CMOS compatible process.

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