

Received November 3, 2019, accepted November 19, 2019, date of publication November 26, 2019, date of current version December 10, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2956076

# A Simple and Novel Precharging Control Strategy for Modular Multilevel Converter

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This work was supported by the National Natural Science Foundation of China, under Project 51777116.

**ABSTRACT** Modular multilevel converter (MMC) has been widely concerned due to its inherent excellent performance in recent years. However, in practical engineering, one of the technical challenges of MMC operation control is how to complete the submodule (SM) capacitors precharging safely and effectively, and reduce the impact of overcurrent phenomenon on the converter during the start -up process. In this paper, a simple and novel precharging control strategy is proposed. It can precharging all SMs of the converter at the same time, without the need for capacitor voltage balance algorithm, extra measurements and additional power supplies. It takes advantage of the symmetry of the grid voltage and the structural characteristics of MMC to form boost circuits between the arms by specific switching operations. Furthermore, the proposed method is not limited by the SM topology. The most commonly used SM topologies can also be converted into boost circuits and have the similar precharging process. By selecting appropriate control parameters, the precharging speed and efficiency of the converter can be improved. The effectiveness of the proposed control strategy is verified by simulations and experiments.

**INDEX TERMS** Modular multilevel converter (MMC), boost circuit, precharging control strategy, startup method.

#### I. INTRODUCTION

Modular multilevel converters have attracted increasing attention because of its excellent characteristics, including superior harmonic performance, modularity and scalability, low switching frequency and high voltage waveform quality [1]–[3]. With these excellent performances, it has gradually become the most popular converter topologies in many fields, such as high-voltage dc transmission [4], large-capacity DC-DC converter [5], energy storage systems [6] and energy routers [7].

At present, the literature relating to MMC mainly focuses on modulation methods, steady-state analysis, circulation suppression, fault-tolerant management, etc., [8]–[12]. Nevertheless, there is still an important but often overlooked technical challenge of MMC, which is how to precharge the SM capacitors to the nominal voltage safely and stably before normal operation. Although different start-up control strategies of MMC have been proposed in previous literature, these strategies either have great demands on real-time PLL

The associate editor coordinating the review of this manuscript and approving it for publication was Zhixiang  $\text{Zou}^{\textcircled{\text{D}}}$ .

control and capacitors voltage balancing algorithm, or require auxiliary power supplies [15]–[24]. It is worth noting that, power electronics in MMC are vulnerable to damage during start-up and if the complexity of the precharging control algorithm is relatively high, it will undoubtedly increase the operational risk of the converter. Therefore, it is of great significance to study the start-up control of the converter.

The existing precharging control methods, developed in the references [13]–[25], can be roughly divided into three categories:

1) Precharging from auxiliary power supplies: methods in this category include using an auxiliary dc power supply to charge the SM capacitors one by one [13], or using a boost circuit composed of an external low-voltage dc power supply to complete the precharging process [14]. The former precharging method is quite simple, but the operation is more complicated and the precharging process takes too long. The latter method is theoretically able to precharging SM capacitor to the nominal value in various applications. However, in high-voltage applications, the insulation requirements of dc source and blocking diode are more stringent, which also increases the cost of the equipment. After completing the precharging process with the above two methods, the power equipment needs to be bypassed from the dc side, which not only increases the charging time but also reduces the utilization rate of the equipment.

2) Precharging from the connected power grid: This kind of precharging method is characterized by the connection to the active power grid. The differences between these methods depend on the charging side of MMC (ac/dc side), or the type of SM topology. In order to limit impulse current in the precharging process on the dc side, the method of adding current limiting resistors in arms and blocking part of SMs is adopted in [15]-[17]. And [15] proposed charging methods with different SMs and charging sides to improve the applicability of charging strategies to different application scenarios. However, the core idea in [15]–[17] is still based on voltage balancing algorithm and blocking part of the arm SMs, in which the charging current waveform of RC circuit is exponentially attenuated, resulting in slow charging speed. Other literature has proposed precharging schemes for their respective SM types, such as CDSM [18], FCSM [19], [20] and SM with DC fault blocking capability [21]. However, they have a narrow range of application and are not applicable to common SM topologies. Generally, the dc side charging process of MMC has been deeply studied, so other papers focus on the ac side starting method.

3) Precharging with complicated control strategies from ac power grid: The method of using constant dc voltage control to complete the precharging process has been proposed in [22], [23], just the application scenarios are slightly different. This control method is improved through the steadystate control strategy by modifying the dc voltage reference. Theoretically, this way can complete the startup of MMC, but the charging process will always face the problem of over-modulation, which is a risk for the converter itself. The closed-loop control startup strategy has been proposed in [24], which can realize the constant charging current during startup, but requires additional PI controller and charging current controller, with high control complexity. In [25], small signal modeling and analysis of start-up process of MMC are proposed, but capacitor voltage feedforward control and average capacitor voltage control are required, so the controller is rather complex. Consequently, these methods require high accuracy of capacitor voltage balance algorithm and controller, and would show their disadvantages when facing the large scale of SMs in the converter in practical applications.

This paper proposes a simple and novel precharging control strategy for MMC in ac side, which is very suitable for MMC startup with a large number of SMs in high voltage applications. It takes advantage of the symmetry of the grid voltage and the structural characteristics of MMC to form boost circuits between the arms by specific switching operations. By analyzing the precharging process between two phase arms, the triggering signal of each arm SM is configured and two sub-modes in the controllable charging process are given. Through the above analysis, the effects of



FIGURE 1. Schematic diagram of MMC.



FIGURE 2. Schematic diagram of different SM topologies: (a) half-bridge SM, (b) full-bridge SM, (c) neutral-point-clamped SM, (d) flying-capacitor SM, and (e) clamp-double SM.

different parameters on the charging process are derived from graphic interpretation. In addition, the precharging process of several other SMs is also analyzed and summarized with the proposed strategy. The effectiveness of the proposed control strategy is verified by simulations and experiments.

#### II. PRECHARGING PROCESS OF MMC

The general schematic diagram of MMC is shown in Fig. 1, in which there are six arms, each arm is composed of N SMs and an inductor in series. Different types of SM can constitute different types of MMC, five common SM topologies are shown in Fig. 2, including half-bridge SM (HBSM), full-bridge SM (FBSM), neutral-point-clamped SM (NPCSM), flying-capacitor SM (FCSM) and clampdouble SM (CDSM). The detailed operation of these SMs has been described in the references [26]–[28] and are not repeated here.

The working modes and the direction of arm current determine the current flow path in the SM. Three working



FIGURE 3. Working modes of HBSM.

modes of HBSM are shown in Fig. 3. Although different SMs have their own modes of operation and means of control, they can meet the requirements of the charging process by simplifying the charging circuit.

In practical engineering, the current limiting resistors are always needed to prevent inrush current, and the precharging process of the converter from the ac side can be divided into two stages [18]:

1) Uncontrollable Precharging (Stage 1): At the beginning of this stage, the voltage of SM capacitor is about zero, so it is impossible to provide energy to control the switches. The grid current flows through the anti-parallel diodes to form an uncontrolled rectifier circuit and the SM capacitors in the circuit are charged. At the end of this stage, the sum of the capacitor voltages is equal to the grid line voltage, and the capacitor voltage can be expressed as  $U_{c_stage1}$ .

2) Controllable Precharging (Stage 2): The capacitor voltage at the end of Stage 1 is enough to drive the control circuit. By orderly switching of SMs, the capacitors can be charged to the rated voltage  $U_{c_stage2}$ .

In recent years, several new precharging control strategies use Bypass Mode and Block Mode. Since the ac voltage in Stage 2 cannot continue charging all the SM capacitors at the same time, a part of the SMs are put into Bypass Mode by means of dynamic grouping, while the rest of the SMs continue to be charged. Such as [15], this strategy requires real-time grouping and sorting control of SMs, and the computational load will also increase when the number of SMs is larger. These conventional ac side precharging control strategies ignore the voltage-pump effect of the arm inductors. This paper will take this as the starting point and propose the boost equivalent model and control strategy without massive computation to realize the simultaneous charging for all SMs in the same arm.

## III. PROPOSED PRECHARGING CONTROL STRATEGY

# A. ANALYSIS OF THE PROPOSED STRATEGY

The idea of the proposed charging control strategy is that the converter arm circuit can be intentionally transformed into a boost circuit by using the inherent circuit characteristics of



FIGURE 4. Charging circuit of HBSMs in AB-phase: (a) inductor-charging mode and (b) capacitor-charging mode.

the SMs and arm inductors in series. The arm inductors are used as the medium for energy transfer, so that the voltage of the capacitor in SMs can be charged rapidly to the rated value. Most of the SM topologies in MMC can be transformed into boost circuits, including the SM topologies shown in Fig. 2. Taking HBSM as an example to explain the precharging principle of the proposed method:

As is known to all, the three-phase grid voltage is symmetrical with each other, so the charging process of each phase is similar. Assuming that the B-phase voltage is the maximum, taking the up-arm of phase A as an example, the following interpretation is about the precharging control of HBSM with Fig. 4.

In HBSM, the discharge circuit can be formed when  $T_1$ is turned on, which is undesirable in charging mode, so  $T_1$ of all HBSMs are always turned off in Stage 2. Then,  $T_2$  can be triggered by periodic signal. When  $T_2$  of all HBSMs are ON, there are only inductors and current limiting resistors in the circuit, thus the arm current increases rapidly, and the magnetic field energy in the arm inductor accumulates continuously. When  $T_2$  of all HBSMs are OFF, since the inductive current cannot be mutated, the SM capacitors are forced into a series circuit. The arm inductor converts the stored magnetic field energy and some of the energy provided by the ac power grid into the electric field energy in the SM capacitors and promotes the voltage of SM capacitors to continue rising. The key of the charging process is how to determine the pulse trigger of  $T_2$ , which also determines the speed of voltage rise of capacitor in SMs. According to the above analysis and Fig. 4, there are two sub-modes of control for all SMs of MMC in Stage 2:

1) Inductor-charging mode (Mode 1): In this mode, capacitors in all SMs are bypassed, shown in Fig. 4(a). Only inductors and current limiting resistors are connected in series in the circuit. The inductors obtain energy through the arm current. Because of the existence of current limiting resistors, there is an upper limit for the increase of current which will be analyzed below.

2) Capacitor-charging mode (Mode 2): Capacitors in the same arm are inserted and connected in series with inductors and current limiting resistors in this mode, shown in Fig. 4(b). And the sum of capacitor voltages is larger than the grid voltage, the current will gradually decrease. The current flowing into the capacitors makes the voltage value rise. If this state lasts for a period of time, the current in the circuit will drop to zero. Since the SM capacitor cannot discharge, the circuit will not generate any current until the next inductor-charging mode.

The design of current limiting resistance has been studied in [18]. The formula is given here

$$R_0 = \sqrt{\frac{2U_L^2}{3I_{ch_{max}}^2} - (X_{ch})^2 - R_a}$$
(1)

where  $U_L$  is AC grid line voltage,  $I_{ch_{max}}$  is the maximum phase current of the charging process,  $X_{ch}$  is minimum reactance of the charging circuit, and  $R_a$  is arm equivalent resistance.

The reactance value of the charging circuit reaches the minimum value in Mode 1, which can be given by

$$X_{ch} = \omega L_0 \tag{2}$$

where  $L_0$  is arm inductance and  $\omega$  is the AC grid angular frequency. To protect the components in MMC from damage, by setting the safety coefficient  $k_1$ , and the maximum charging current is set as

$$I_{ch_{max}} = \frac{I_{rated_{m}}}{k_1} = \frac{\sqrt{2S_N}}{\sqrt{3}k_1U_L}$$
(3)

where  $I_{rated_m}$  is peak value of rated line current. Therefore, based on the above analysis, the current limiting resistance can be calculated.

#### **B. BOOST EQUIVALENT CIRCUIT**

From Fig. 4, arm voltage of B-phase is negative and the current in the arm flows to the positive bus  $(Line_p)$  through the antiparallel diode, ignoring the conduction voltage drop of the diodes and arm equivalent resistance, the positive bus voltage is given by

$$u_{Line\_p} = u_{sb} - R_0 i_{pb} - L_0 \frac{di_{pb}}{dt}$$
(4)

where  $u_{Line_p}$  represents the voltage of the positive bus,  $R_0$  represents the current limiting resistance and  $L_0$  represents the arm inductance. From Fig. 4, turning on or off IGBTs in B-phase will not affect the current circuit. In order to simplify the control strategy, the control of IGBTs in B-phase can be

the same as that in A-phase. Based on (4), the corresponding arm voltage of phase A can be given by

$$u_{a\_up} = u_{Line\_p} - u_{sa} \tag{5}$$

When  $T_2$  of all SMs in the upper arm of phase A are ON, the arm voltage can be given according to the equivalent circuit

$$u_{a\_up} = L_0 \frac{di_{pa}}{dt} + R_0 i_{pa} \tag{6}$$

The charging circuit in Mode 1 is a first-order circuit. Assume  $t_1$  is the initial moment of Mode 1, the phase angle of phase A voltage at  $t_1$  is  $\varphi_{ua1}$  and the initial current at  $t_1$  is  $I_{a1}$ . Then the analytical formula of the charging current can be obtained by

$$i_{a1}(t) = \begin{cases} \left[ I_{a1} - \sqrt{\frac{1}{6}} \frac{U_L}{|Z_1|} \cos(\varphi_{ua1} - \varphi_{z1}) \right] e^{-\frac{t-t_1}{\tau}} \\ + \sqrt{\frac{1}{6}} \frac{U_L}{|Z_1|} \cos[\omega(t-t_1) + \varphi_{ua1} - \varphi_{z1}] \end{cases}$$
(7)

where

$$|Z_1| = \sqrt{R_0^2 + (\omega L_0/2)^2}$$
(8)

$$\tau = \frac{L_0}{2R_0} \tag{9}$$

$$\varphi_{z1} = \tan^{-1} \left( \frac{\omega L_0}{2R_0} \right) \tag{10}$$

According to circuit analysis, the transition process of the first order circuit is exponential. In engineering, it is generally believed that the transition process ends when the error is less than 5%. That is to say, the transient decay time from  $3\tau$  to  $5\tau$  can be regarded as the end of the transient process. In this paper,  $5\tau$  is taken as the end time, so the effective charging time in Mode 1 is defined as

$$T_{eff} = 5\tau \tag{11}$$

And when  $T_2$  of all SMs in the upper arm of phase A are OFF at  $t_2$ . It can be determined that

$$I_{a1}(t_2) = I_{a2} \tag{12}$$

Then, the arm voltage can be given by

$$u_{a\_up} - \sum_{i=1}^{N} u_{sm\_i} = L_0 \frac{di_{pa}}{dt} + R_0 i_{ap}$$
(13)

The charging circuit in Mode 2 is a second-order circuit. Assume the phase angle of the line-to-line voltage at the initial moment of Mode 2 is  $\varphi_{uab2}$  and the analytical formula of the charging current can be obtained by

$$i_{a2}(t) = A_1 e^{-r_1(t-t_2)} + A_2 e^{-r_2(t-t_2)} + A_3 e^{-r_3(t-t_2)} + A_4 e^{-r_4(t-t_2)}$$
(14)

where

$$\begin{cases} r_{1,2} = \frac{1}{2} \left( -\frac{R_0}{L_0} \pm \sqrt{\left(\frac{R_0}{L_0}\right)^2 - \frac{4}{L_0C}} \right) & (15) \\ r_{3,4} = \pm j\omega \end{cases}$$

$$A_{1} = \frac{\sqrt{2r_{1}U_{L}\left[r_{1}\cos(\varphi_{uab2}) - \omega\sin(\varphi_{uab2})\right]}}{L_{0}(r_{1} - r_{2})(r_{1}^{2} + \omega^{2})} + \frac{r_{1}I_{a2}L_{0} - \sum_{i=1}^{N}u_{Ci}(t_{2})}{(r_{1} - r_{2})L_{0}}$$
(16)

$$A_{2} = -\frac{\sqrt{2}r_{2}U_{L}\left[r_{2}\cos(\varphi_{uab2}) - \omega\sin(\varphi_{uab2})\right]}{L_{0}(r_{1} - r_{2})(r_{1}^{2} + \omega^{2})} - \frac{r_{2}I_{a2}L_{0} - \sum_{i=1}^{N}u_{Ci}(t_{2})}{(r_{i} - r_{2})L_{0}}$$
(17)

$$A_{3} = \frac{\sqrt{2}U_{L} [r_{3} \cos(\varphi_{uab2}) - \omega \sin(\varphi_{uab2})]}{2L_{2} (r_{2} - r_{2}) (r_{2} - r_{2})}$$
(18)

$$A_4 = \frac{\sqrt{2}U_L \left[ r_4 \cos(\varphi_{uab2}) - \omega \sin(\varphi_{uab2}) \right]}{2L_0 \left( r_4 - r_1 \right) \left( r_4 - r_2 \right)}$$
(19)

During the charging process, the inductive pump is used to transfer power from the AC grid to the capacitors, and the variation of capacitor voltage can be further obtained by

$$\Delta u_{c} = \int_{t_{2}}^{t_{1}+T_{c}} C_{sm} i_{2}(t) dt$$
(20)

where  $T_c$  is carrier period. The initial current of Mode 2 in each switching period can be denoted as  $I_{a2}(k)$ . As the current waveform in the charging circuit of Mode 1 do not change with the charging process, the average value of  $I_{a2}$  within a grid cycle cannot be changed, so

$$\langle I_{a2} \rangle = \frac{1}{N} \sum_{k=1}^{N} I_{a2}(k)$$
 (21)

$$N = \frac{f_{ac}}{f_c} \tag{22}$$

where  $f_{ac}$  is the grid frequency and  $f_c$  is the carrier frequency. It is can be derived from (20) and (21) that the average value of the rise rate of capacitor voltage would be an almost constant. Therefore, this charging method can achieve an approximate linear speed to charge all SMs of the converter, which is capable of charging rapidly. Fig. 5 containing the calculation waveform and the simulation waveform can be obtained with the system parameters of Nan'ao project, which is shown in TABLE 1.

Where, the envelope waveform is the maximum charging current limited by current limiting resistance, which can be expressed as

$$i_{ch_{max}} = I_{ch_{max}} \cos(\omega t - \varphi_{z1})$$
(23)

When calculating the waveform of the transient process in Mode 2, the internal parameters of power electronic devices, such as cut-off voltage and internal resistance of IGBTs, are ignored, resulting in an error of 1.42%. The waveform calculated here is just to analyze the influencing factors of precharging control, so this small error can be ignored. It can be seen from the above analysis and Fig. 5 that the charging



**FIGURE 5.** Controllable charge transient waveform: (a) charging current and (b) capacitor voltage.

TABLE 1. Simulation parameters of MMC.

Simulation parameter	Value
Nominal capacity	100 MVA
AC line voltage	166 kV
DC line voltage	$\pm 160 \text{ kV}$
AC grid frequency	50 Hz
Number of SMs per arm	200
Nominal SM voltage	1.6 kV
Capacitance of SM capacitor	2.5 mF
Arm inductance	180 mH
Current limiting resistance	1.1 kΩ
Switching devices	IGBT (3300 V / 1000 A)

speed of capacitor is related to hardware parameters and control parameters. As is known to all that the design of main circuit parameters of MMC depends on its steady-state operation characteristics and other practical factors. In order not to affect its normal operation, the parameter design of charging process should not change the parameters of main circuit. Hence, the remaining adjustable parameters are carrier frequency and duty ratio in controller.

By using the simulation parameters in TABLE 1, the relationship between the rise time of capacitor voltage in Stage 2 and carrier frequency and duty ratio is verified by simulation as shown in Fig. 6. It can be found that, for a certain duty ratio, when the carrier frequency increases, the charging speed will increase correspondingly. However, when the carrier frequency is higher than 1000 Hz, the effect of increasing frequency on improving charging speed decreases obviously. Fully considering the electrical parameters, charging efficiency and safety redundancy of power electronic devices, 800 Hz carrier frequency is appropriate. On the other hand, it is also can be found that under the same carrier frequency, too large or too small duty ratio will inhibit the charging efficiency. That is because when the duty ratio is too small, the time of Mode 1 is relatively short, and the energy obtained by the inductor is less, the energy converted into the capacitor per unit switching period will be correspondingly reduced. When the duty ratio is too large, the time of Mode 2 is relatively short. Although the inductors gain a lot of energy,



FIGURE 6. The rise-time of capacitors voltage in Stage 2 with different duty ratios and carrier frequencies.



FIGURE 7. The rise-time of capacitors voltage in Stage 2 with different initial phase of carrier.

there is not enough time to transfer it into the capacitors, so the rise speed of capacitor voltage will also decrease. This trend is also shown in the simulation waveform in Section IV. Since the charging circuit is a first-order circuit in Mode 1, the decay time of its free component is fixed. According to (11), when the carrier frequency is 800 Hz, its duty ratio can be calculated as

$$d = T_{eff} f_{carry} = 0.384 \approx 0.4 \tag{24}$$

In the above analysis, it can also be found that  $\varphi_{u1}$  may also be another factor affecting the charging speed. But carrier frequency is generally much larger than the grid frequency, so the impact is small. Fig. 7 shows the controllable charging stage time at different carrier initial phase with d = 0.4 and fc = 800 Hz. As can be seen from this figure, with the change of carrier initial phase, the fluctuation of controllable charging time is very small, and the maximum deviation is no more than 0.6%. Therefore, from the perspective of engineering, this deviation can be ignored.

Due to the topological structure characteristics of MMC and the symmetrical relationship between three-phase voltages of the power grid (time symmetry of three-phase voltage), the precharging control method of other arms are similar, except that they lag each other in time. So the charging process of the converter is phase-by-phase in accordance with the order of the voltage of the power grid. The charging current of the upper and lower arms of the same phase is opposite, so their charging process is also symmetrical. The precharging sequence of capacitors in the six arms of the converter, carrier and pulse trigger waveforms are shown in Fig. 8.

Taking A-phase capacitors as an example, when phase A is the minimum voltage in the three-phase power grid, the upper arm voltage of phase A is positive, and the boost circuit formed by the arm inductors charges these capacitors.



FIGURE 8. The precharging sequence of six arms.

When phase A is the maximum voltage, the upper arm voltage of phase A is negative and the arm current flows only through the diodes, not capacitors, so the capacitor voltage remains unchanged. The charging process of the lower arm is the same as that of the upper arm, but the charging time is exactly the opposite. After a grid cycle, the capacitors of the six arms of the converter all get the same precharging time, so their voltage variations are almost the same in one cycle. And for all SMs in the same arm, we know that the ideal simultaneous switching does not exist in engineering practice. But the effect of the switching delay can be ignored when the error time is within the allowable range. According to IGBT's inherent switch delay and drive signal delay, the maximum delay time between each SM can be considered no more than 5 us, while the carrier period corresponding to 800 Hz is 1.25 ms. Therefore, it can be assumed that switching delay of the SMs in practical project will not affect the precharging process.

In general, the rated arm inductor voltage and insulation level are designed to withstand short circuit faults. That means that the arm inductor in series should to be able to withstand dc rated voltage or ac line voltage. In practical engineering, the rated voltage of inductor is generally taken as the line voltage of ac power grid to meet the requirement of fault tolerance. The proposed charging strategy ensures that the inductor voltage stays within the safe voltage range during the start-up process. Hence, this charging method is no harm to the inductor itself, which is also verified in the simulation. According to [29], to reduce the voltage mutation on arm inductors further, small delay signals can be added in turn to the trigger unit to drive  $T_2$  of different SMs, which is also considered and verified in the simulation results in Section IV.

On the other hand, considering the inconsistency of threephase voltage amplitudes and SM capacitances in practical projects, the charging speed of each unit will not be completely consistent, so it is necessary to check whether the charging unit has completed charging. In detail, when M SMs in the same arm have completed charging, the M SMs are always kept in Mode 1, while other SMs can still be charged in the specified Mode 2. When the entire arm has been charged, all SMs in the arm will be in Block Mode. The anti-parallel diode can continue to provide charging current to the arms of other phases, so the arms will not affect each other during the controllable charging process. In addition, the real-time detection of capacitor voltage in the controller is always used to ensure that capacitor voltage is within the specified range to avoid damage to electrical components.

Due to the symmetry of the converter topology and the grid voltage, the charging current will naturally change direction, so the phase of the grid voltage is not taken into consideration. In other words, the PLL control is not required. Since there is no discharge loop (since  $T_1$  is always switched off during the whole precharging process), the controller does not need to design dead zone time separately, which improves the safety of the converter during charging. Therefore, compared with the precharging strategy in this paper greatly simplifies the controller design.

#### C. APPLICABLE TO DIFFERENT SM TOPOLOGIES

The proposed precharging strategy is also applicable to other common SM topologies, including some topologies shown in Fig. 2. The precharging control of other SMs is similar to that of the HBSM. Some IGBTs are blocked to prevent the capacitor from discharging, and the other IGBTs are switched on and off periodically to make the converter's arm form boost circuit. This method still uses the pumping effect of the arm inductors to continue charging the capacitors. The difference between their precharging control mode and that of HBSM lies in the need to turn on some IGBTs to realize the capacitor bypass. It is still assumed that the voltage of phase B is the maximum value to analyze the precharging process of the arm capacitors on phase A.

Due to the limitation of the length of the article, taking CDSM as an example with Fig. 9. In Fig. 9, two capacitors can be charged in series to realize the precharging. In this way, all capacitors in the converter can be charged simultaneously. In the precharging state shown in Fig. 9, the current of the upper arm of phase B is negative, and all the capacitors in this arm need to be bypassed, but the CDSM cannot bypass the capacitor only by antiparallel diodes. Therefore,  $T_5$  in the serial pathway should be always turned on to form an inductive charging circuit in this arm. Switches  $T_1$  and  $T_4$  that can form discharge paths are always turned off. In the SMs of upper arm of phase A, when  $T_2$  and  $T_3$  are turned on, the two capacitors are bypassed, the current in the circuit increases rapidly, and the arm inductor stores energy.

When  $T_2$  and  $T_3$  are turned off, both capacitors of CDSM are connected in series in the circuit, the inductor transfers energy to the capacitors, and the capacitors voltage increase gradually. The trigger signal can be applied to the gates of  $T_2$ and  $T_3$  of all the CDSMs in the converter. When  $C_1$  completes charging first,  $T_2$  is kept in Mode 1. On the contrary, when  $C_2$ completes charging,  $T_3$  is kept in Mode 1. When the entire arm is charged, the arm will enter the Block state. In this way, the fast start-up of CD-MMC can be realized. Similar to the CDSM precharging process, most other topologies

![](_page_6_Figure_8.jpeg)

**FIGURE 9.** Charging circuit of CDSMs in AB-phase: (a) inductor-charging mode and (b) capacitor-charging mode.

![](_page_6_Figure_10.jpeg)

FIGURE 10. Boost equivalent charging circuit: (a) inductor-charging mode and (b) capacitor-charging mode.

TABLE 2. Control methods of different SMs.

Type of SM	Normally ON	Normally OFF	Mode 1 Trigger Enable	Mode 2 Trigger Enable
HBSM		$T_1$	$T_2$	—
FBSM	$T_4$	$T_1 T_3$	$T_2$	—
FCSM	$(T_4)$	$T_1 T_2$	$T_3 T_4$	—
NPCSM		$T_1 T_2$	$T_3 T_4$	—
TMSM		$T_1 T_3 T_4$	$T_2$	—
CDSM	$T_5$	$T_1 T_4$	$T_2 T_3$	_
HDSM	$T_5$	$T_1 T_4$	$T_2 T_3$	—
CCSM	$T_{5}, T_{6}$	$T_1 T_4$	$T_2 T_3$	—
CCDSM	$T_5$	$T_1 T_4 T_6$	$T_2 T_3$	—

in [26] can be controlled to start-up the converter. Different SM topologies can form similar equivalent charging circuits which shown in Fig. 10 through the control method shown in TABLE 2. And the control parameters of different SM topologies also can be selected by the similar analysis method as above. Finally, the control block diagram of proposed precharging strategy can be obtained, as shown in Fig. 11.

#### **IV. SIMULATION RESULTS**

# A. PRECHARGING SIMULATION FOR

### **DIFFERENT TYPE OF SMs**

Simulation studies have been performed by using MATLAB/Simulink to verify the proposed precharging

![](_page_7_Figure_2.jpeg)

FIGURE 11. Control block diagram of proposed precharging control strategy.

control strategy. Both of the HBSM and the CDSM have been studied. The simulation parameters are taken from the Nan'ao project, as shown in TABLE 1. The safety coefficient  $k_1$  was set as 3, the maximum of charging current  $I_{ch\_max}$  is about 0.12 kA and the current limiting resistance is 1.1 k $\Omega$ . The trigger delay time of different groups was set as 5 us and the capacitance error of 10% were also considered in the simulation. Fig. 12 shows the simulation result of HBSM precharging with d = 0.4 and  $f_c = 800$  Hz. Ten voltages of capacitors in six arms of the converter are shown in Fig. 12(a) and (b), respectively.

In order to facilitate the explanation, ten capacitor voltages in the A phase upper arm were selected, including the voltage waveform with the largest error of capacitance value, and all other capacitor voltage waveforms were in the middle of these two envelope lines, with the same variation rule. The controllable precharging starts at t = 1.5 s, and at the moment, the average voltage of SM capacitors is  $U_{c_stage1} = 1.17$  kV. Due to the capacitance error, the voltage of the SMs capacitor in upper-arm of phase A will be different. Since all the SMs are charged simultaneously in the controllable precharging stage, their charging waveform is similar, which is reflected in the fact that different capacitor charging waveforms rise in parallel.

It also can be seen from the enlarged figure in Fig. 12(a) that the SM capacitors are stopped charging after charging to the rated value  $U_{c_{stage2}} = 1.6$  kV, and this voltage value of capacitors remains stable. Depending on the symmetrical structure of MMC and the anti-parallel diodes

in SMs, the charging process of six arm SM capacitors is similar but independent. As can be seen from the enlarged figure in Fig. 12(b), even if the charging speed of each arm is slightly different, it will not affect the final charging completion. After a period of approximately linear charging process, the voltages of all SM capacitors in the converter are closed to the rated value. Since the capacitor voltage varies almost linearly, the charging speed is faster than the exponential attenuation waveform shown in Fig. 13 proposed in [15]. And then in Fig. 12(c) and (d), the current of upper-arm of phase A and the three-phase current of the converter are shown, respectively. Depends on the current limiting resistors, the maximum charging current of phase A in the Stage 2 is about 0.12 kA. As can be seen from the enlarged figure, the charging current of the three phases remains stable and relatively symmetrical. At the controllable charging end, since the SMs of the A-phase lower arm are charged, the A-phase current is only composed of the upper arm charging current. Therefore, the amplitude of arm current waveform increases, which is consistent with the phase current. Therefore, in the whole process of controllable charging, the charging current is always lower than the Ich\_max, so the charging process has good stability without overcurrent.

Fig. 14 shows the arm inductor voltage waveform. As can be seen from the figure, at the moment when the converter is connected to the ac grid at 0.2s, an impulse voltage is generated on the inductor, which is inevitable. Because there is no current in the loop at this moment, the voltage of current limiting resistor is nearly zero, and all SM capacitor voltage are also almost zero, so only the arm inductors bear this ac voltage. Generally, considering the short-circuit fault, the arm inductor rated voltage and insulation level are designed to withstand the rated line voltage, so the transient voltage on the arm inductor during the starting process should not exceed this rated voltage. From Fig. 14, the voltage on the arm inductor is always lower than the ac line voltage (shown by the orange line), which is in line with the safety voltage. In addition, due to the slight delay of the sub-module trigger signal, the voltage of the inductor rises as a ramp, which can be seen in the right enlarged image of Fig. 14. It also greatly reduces the voltage change rate on the arm inductors. In addition, arm inductors are usually placed far away from the control circuit and drive circuit, and the charge process is very short compared to the long-time of rated operation, so EMI issues during start-up can be ignored.

Fig. 15 shows the result of CDSM precharging with d = 0.4 and  $f_c = 800$  Hz. The average voltage of capacitors in six arm of the converter, the voltage of two capacitors in the same SM, the upper-arm current of phase A and the three-phase current of the converter are shown in Fig. 15(a), (b), (c), and (d), respectively. The precharging of Stage 2 starts at t = 1.5 s with the average voltage of SM capacitors is  $U_{c_stage1} = 782$  V. Similarly, considering the error of capacitance value, the waveform of capacitor charging voltage rise with different capacitance is not completely consistent, as shown in Fig. 15(a) and (b).

![](_page_8_Figure_2.jpeg)

FIGURE 12. Simulation result of precharging HBSM: (a) capacitor voltage in upper-arm of phase A, (b) average capacitor voltages in six arms, (c) upper-arm current of phase A, and (d) three-phase current.

![](_page_8_Figure_4.jpeg)

FIGURE 13. Simulation result of charging method proposed in Ref. [15]: (a) capacitor voltage in upper-arm of phase A and (b) three-phase current.

![](_page_8_Figure_6.jpeg)

FIGURE 14. Waveform of arm inductor voltage.

Through the proposed control method, all capacitors can be charged without exceeding the rated voltage. Since the hardware parameters and control parameters are the same as the HBSM, the maximum value of charging three-phase current is not much different and the current amplitude is about 0.12 kA. The  $U_{c\_stage1}$  in CDSM is about two thirds of that in HBSM, so the charging time of CDSM is a little longer. But this does not affect the stability of the charging process, the voltage value of the CDSM capacitor rises approximately linear, the maximum charging current remains unchanged, and the trend of various waveforms is basically the same as that of HBSM waveforms. It shows that the proposed charging control strategy has good applicability to different SM topologies.

#### B. PRECHARGING SIMULATION OF HBSM WITH DIFFERENT CONTROL PARAMETERS

According to the above analysis, the change of control parameters will affect the charging speed. Here is the simulation waveform of MMC when the control parameters change. Simulation studies have been performed by using MATLAB/Simulink with different control parameters.

![](_page_8_Figure_12.jpeg)

**FIGURE 15.** Simulation result of precharging CDSM: (a) average capacitor voltages in six arms, (b) two capacitor voltages in the same SM, (c) upper-arm current of phase A, and (d) three-phase current.

And the hardware parameters in TABLE 1 are still used. According to the curve shown in Fig. 6, when the carrier frequency is fixed, the duty ratios can have a great impact on the charging process only when the value is at two extremes. Fig. 16 is shown the precharging process of HBSM with different duty ratios and the carrier frequency is  $f_c = 800$  Hz. By comparing the waveforms in Fig. 16, it is easy to be found that too large or too small duty ratio will reduce the controllable charging speed when carrier frequency is fixed;

![](_page_9_Figure_1.jpeg)

**FIGURE 16.** Simulation result of precharging HBSM with different duty ratios and fixed carrier frequency.

![](_page_9_Figure_3.jpeg)

FIGURE 17. Simulation result of precharging HBSM with fixed duty ratio and different carrier frequencies.

and when the duty ratio is set as the median value, the change has little impact on the charging speed, which is corresponds to the previous analysis.

Fig. 17 is shown the precharging process of HBSM with different carrier frequencies and the duty ratio is constant d = 0.4. By comparing the three waveforms in Fig. 17, it can be seen that when the duty is fixed, the reduction of carrier frequency will reduce the charging speed of the capacitor. The reason for this also can be found in enlarged diagrams in Fig. 17. We know that the decrease of carrier frequency makes the boost circuit triggered less times per gird cycle, and then, the rise of capacitor voltage decreases, finally causing the charging speed to drop. Based on Fig. 6, we know that within a certain range, the increase of carrier frequency can improve the precharging speed. But the increase of speed is gradually decreasing with the increase of frequency, and the larger carrier frequency will also burden the power electronic devices. Therefore, carrier frequency selection needs to refer

![](_page_9_Picture_8.jpeg)

FIGURE 18. Photograph of the laboratory prototype.

TABLE 3. Experiment parameters of MMC.

Experiment parameter	Value
AC line voltage	150 V
AC grid frequency	50 Hz
Number of SMs per arm	4
Nominal SM voltage	90 V
Capacitance of SM capacitor	2 mF
Arm inductance	2.5 mH
Current limiting resistance	30 Ω

to the safety switching frequency of power electronic devices. The safe switching frequency of IGBTs can usually reach several kilohertz, so the 800 Hz selected in this paper is safe and reasonable.

#### **V. EXPERIMENTAL RESULTS**

In order to verify the validity of the proposed precharging methods, a three-phase MMC prototype with four SMs per arm has been built, as shown in Fig. 18. TABLE 3 lists the circuit parameters for the experiments.

Fig. 19 shows the experimental result of HBSM precharging with d = 0.4 and  $f_c = 800$  Hz. The voltage of capacitors in lower arm of three-phase and the A-phase lower arm current of the converter are shown in Fig. 19(a), and the three-phase current of the converter is shown in Fig. 19(b). The precharging of Stage 2 starts at  $t_1$ , and at the moment, the voltage of HBSM capacitor is  $U_{c \text{ stage1}} =$ 52.8 V. As can be seen from the enlarged figure on the left in Fig. 19(a), the charging process of the three capacitor voltages differs from each other by 120 degrees, which is consistent with the above analysis and simulation results. Due to the inherent error of the capacitor value, the capacitor with a smaller capacitance has a faster voltage rise rate during the controllable charging process, so there is a slight voltage deviation at the end of the Stage 2. Through the proposed control method, all the capacitors can be charged to the rated value  $U_{c_{stage2}} = 90$  V at  $t_2$  which is shown in the enlarge figure on the right in Fig. 19(a). The maximum of A-phase lower arm charging current is about 3.76 A which is less than  $I_{ch_{max}} = 4$  A, without the overcurrent phenomenon.

![](_page_10_Figure_2.jpeg)

FIGURE 19. Experimental result of precharging HBSM: (a) three upper-arm capacitor voltages and (b) three-phase current.

From Fig.19(b) and the enlarged figures, the three-phase current has good symmetry, and the waveform is also the same as the simulation verification, which indicates that the proposed control strategy is reasonable and feasible.

Fig. 20 shows the experimental result of HBSM precharging with different duty ratios or carrier frequencies. In Fig. 20(a) and (b),  $u_{c_{aup}}$  is charged from 52.8 V to 90 V during Stage 2. The maximum value of three-phase charging current in Fig. 20(a) is about 3.1 A, and in Fig. 20(b) is about 4 A. By comparing Fig. 19 and Fig. 20, it shows that, the trend of waveform change is the same as that in simulation verification with the change of control parameters. Based on the fact that the converter can be stably precharged to the rated value under different control parameters, the correctness of the theoretical analysis and the effectiveness of the proposed method is verified. It is worth mentioning that the ac power supply used in the experiment is the actual threephase power grid voltage, and its voltage waveform is not completely ideal symmetric. However, from the experimental waveforms, we found that it does not affect the charging process and results, which also indicates the applicability of the proposed charging strategy.

![](_page_10_Figure_6.jpeg)

**FIGURE 20.** Experimental result of precharging HBSM with different duty ratios and carrier frequencies: (a) three upper-arm capacitor voltages and three-phase current when d = 0.2 and  $f_c = 800$ Hz, (b) three upper-arm capacitor voltages and three-phase current when d = 0.5 and  $f_c = 500$ Hz.

#### **VI. CONCLUSION**

In this paper, a simple and novel precharging control strategy is proposed for MMC. It takes advantage of the symmetry of the ac grid voltage and the structural characteristics of MMC to form boost circuits between the arms by specific switching operations. The proposed strategy has the advantage of charging the capacitors without the need for complex controller, capacitor voltage sorting balance algorithm, and auxiliary charging equipment. In the description of the proposed control strategy, the charging process is divided into two sub-modes and the boost equivalent circuit diagram of ac side precharging is obtained. Then the proposed strategy is analyzed theoretically, and the approximate linear charging capability of the control strategy which can improve the charging speed of MMC is derived. The idea of this method is applied to other SM topologies, which have similar quick charging effect, and the control methods of different SMs are summarized. Based on the formula derivation and simulation waveform, the influence of control parameters on the proposed precharging strategy is analyzed and the appropriate control parameters of boost equivalent charging

circuit are derived. The same startup effect is obtained in the physical experiment platform. Through simulation and experiment, the effectiveness of the proposed precharging control strategy and the influence of control parameters on the charging process are verified.

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![](_page_11_Picture_34.jpeg)

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![](_page_11_Picture_36.jpeg)

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![](_page_12_Picture_2.jpeg)

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![](_page_12_Picture_4.jpeg)

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