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RF Energy Scavenging With a Wide-Range Input Power Level

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ABSTRACT Energy scavenging is a promising technique for micro-devices such as wireless sensor networks (WSNs). Radio frequency (RF) is considered a sustainable source that can be utilized and harvested due to its important features. The essential goal of this study was designing and investigating a wide input power range through a theoretical and simulation work for the 900 MHz frequency band with acceptable efficiency. In this work, we investigated both the low input power and the high input power range circuits; the two circuits were combined to achieve the goal of the wide input power range. L impedance matching elements were used to perform the desired matching between the power source and the circuit to reduce the reflected power resulted in enhanced RF-DC conversion efficiency. 60 % was the peak efficiency for the proposed design at 0 dBm with the output voltage of 16.56 V, and a generated current of 1.39 mA for the load of 12KΩ.

INDEX TERMS Conversion efficiency, input power level, rectifier topology, RF energy scavenging.

I. INTRODUCTION

The unique features of wireless sensor networks (WSNs) have made it an interesting research area for scientists all around the world. WSNs are utilized in diverse areas such as health, environment, and industrial monitoring. Mostly, batteries are the basic power source for wireless sensors [1], [2]. The performance efficiency of WSNs depends on the battery lifetime, therefore the lifetime should be within several months or years. Battery replacement can become complicated in sensor networks consisting of thousands of nodes [3], however, energy harvesting techniques have been growing rapidly. Some sources of renewable energy include solar radiation, wind, heat, vibration, etc [4]–[8]. Energy scavenging can provide a continuous power to feed WSNs for autonomous sensors [2]–[11]. Radio frequency (RF) wave is one of the renewable sources that is broadcasted for 24 hours per day through different sources such as routers, radar systems, radio transmission towers, and mobile base stations [12]. That is why RF energy harvesting is considered a viable solution. RF energy scavenging system can be integrated with appropriate and lightweight equipment for daily use. Therefore RF energy scavenging can be utilized to overcome defects of the traditional sources. The main function of RF scavenging is harvesting the surrounding electromagnetic energy and converting it into useful DC power. The RF energy harvesting system depends on the RF receiver that includes six stages as shown in Fig.1.

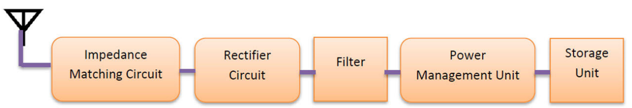

FIGURE 1. RF energy harvesting system.

The receiver is composed of a receiving antenna, an impedance matching circuit, a rectifier circuit, a filter, a power management unit, and a storage unit. The receiving antenna is the first part which is the interface between the radiated electromagnetic waves in the medium and the other parts of the receiver. The antenna works to capture RF waves and convert them into electrical signals. Since the extracted electrical signals are alternating, the rectifier is needed to rectify the generated signals.

Different topologies have been designed since the basic element for these topologies is the diode or the transistor. To achieve the maximum transferred power, the impedance matching circuit is used. The impedance of both the receiving antenna and the rectifier are different and not matched, therefore neglecting the impedance matching results in a high

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power loss. Hence, the mismatching between the receiving antenna and the rectifier degrades the RF-DC energy conversion efficiency.

RF Energy harvesting system faces many challenges; some of them are related to the receiving antenna. Other challenges are mainly due to lapses in impedance matching and rectifier design such as the conversion efficiency of the rectifier, the number of rectifier stages, and the rectifier topology [13]. Many researchers have studied and proposed solutions to combat conversion inefficiencies. For example, a rectifier design was presented by Skaik [14] to harvest RF power for a quad-band at input power levels of −10, 0, and +10 dBm. A Latour voltage doubler was designed by Mabrouki *et al.* [15] for low input power levels in a range of -30 dBm to -10 dBm at 10KΩ resistor load (R_L) and 850MHz resonance frequency. Yunus [16] proposed a Dickson voltage multiplier and L-matching circuit for utilizing GSM 900 MHz signals at different input power levels below +10 dBm. Rajawat *et al.* [17] presented a Karthaus-Fischer voltage multiplier as a rectifier for the band of GSM 2.45 GHz at a range extended from 0 to 24 dBm input power. A far-field RF energy harvesting technique was offered by Baranov *et al.* [18] for powering wireless gas sensor nodes at 900 MHz with input power levels varied between −20 dBm and 10 dBm. At the same trend, Mouapi *et al.* [1] suggested a technique for autonomous WSNs design powered by RF at the ISM band 2.45GHz for multiple input power levels. Finally at a limited input power range of -18 dBm to -10 dBm a differential cross-coupled rectifier was presented by Ouda *et al*. [19] for enabling wireless powering across different distances, at a signal frequency of 1GHz.

Based on the mentioned literature, it is clear that most of the designs focused on utilizing wide-bands whereas input power levels were resolved as a dependent parameter. Some of these designs considered a limited range of input power levels. Actually, there are many reasons for varying the input power level, mostly they are based on the receiving antenna characteristics, another reason is the distance between the transmitting source and the RF receiver. However, the input power level is an important point that should be taken into account. The variation of the input power level causes a dynamic impedance at the rectifier input that indicates more power loss by the current designs.

In this work, we introduce and investigate a wide input power range with a simple design and an interesting RF-DC conversion efficiency. Both the low and the high input power circuits were studied then they were combined to achieve the wide input power range. The rest of this paper is divided as follows: the system theory is explained in the second section, the third section introduces the circuit design for the low input power range circuit design, the high input power range circuit design, and the wide input power range circuit design. Simulation results and discussion are presented in the fourth section. Finally, the conclusion of this study is provided in the fifth section.

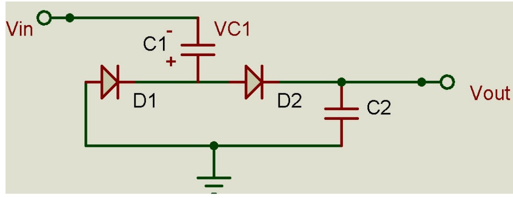


FIGURE 2. A typical single-stage voltage multiplier circuit.

II. THEORY

The received RF power level is manipulated by some parameters, these parameters are governed by the Friis equation as follow [16]:

$$P_r = P_t G_r G_t (\lambda/4\pi R)^2 \quad (1)$$

where P_r is received power, P_t is transmitted power, G_r is receiving antenna gain, G_t is transmitting antenna gain, λ is wavelength, and R is the distance between the source and receiver. Through the mentioned equation, it is clear that the transmission antenna, the receiving antenna, and the distance between the two antennas manipulate the received input power level. A typical single-stage voltage multiplier is shown in Fig.2. Usually, this multiplier is connected to an antenna through a matching element. There is no power supply or DC bias for this circuit just only the energy of the applied RF signal at the input.

First, it is supposed that both C_1 and C_2 of the voltage multiplier are initially discharged and a single-tone signal (V_{in}) is applied to the input which has an amplitude (V_m) and an angular frequency (ω). V_m depends on the received input power. The ripple at the output voltage is neglected. During the negative half-cycle of the input, D_1 is forward-biased at $\Delta\tau_1 = t_2 - t_1$, while D_2 is off then when the input changed into the positive half-cycle, D_2 is switched on at $\Delta\tau_2 = t_4 - t_3$, while D_1 is reverse biased. Besides, there is an interval between turn-on times of diodes which both diodes are reverse biased within that interval. Fig. 3 shows one cycle operation for the rectifier since the moments of t_1, t_2, t_3, t_4, and T are considered from the origin of the coordinates.

From Kirchhoff voltage law, D_1 turns on at t_1 when $V_{in} \leq -(V_{th} + V_{C1})$. V_{th} and V_{C1} are the diode threshold voltage and the voltage across C_1 respectively, then C_1 is charged until the input reaches t_2. It is noticed that C_1 is charged quickly, therefore, the C_1 voltage can easily follow the input voltage since this capacitor has a small capacitance. Hence V_{C1} increases to be about $(V_m - V_{th})$ at t_2 which is close to T/4 (where T is the input signal period time). When the input reaches t_2, D_1 is reversely biased, but D_1 and D_2 are still off until t_3. D_2 turns on when $V_{in} \geq V_{th} - V_{C1} + V_{out}$ between t_3 and t_4. D_2 is reverse-biased at moment t_4 and both diodes will be off until the cycle ends. The variation level of the output voltage is smaller than the input rate therefore when the circuit is analyzed at the input rectifier frequency, it can be assumed that V_{out} is AC ground and the effect of C_2 value on the impedance of the input can be neglected. For this analysis [20]–[23], the diodes are assumed to be the

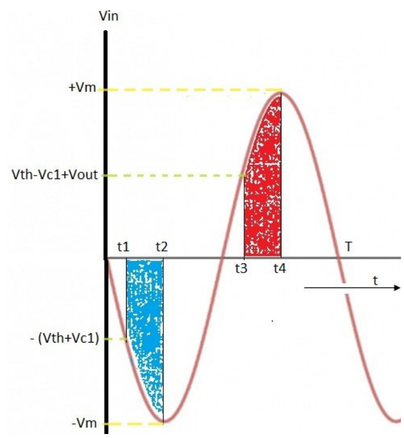


FIGURE 3. One cycle operation of the voltage multiplier.

same for obtaining the necessary formulas. There are two expected operation cases in each cycle: the first case is that both of the diodes are reversely biased whereas the second case is that one of the diodes is forward biased while the other diode is reverse-biased. Therefore in each cycle, the rectifier input impedance significantly is changed based on the diodes switching between the two cases. Thus the equivalent input impedance of the input of the rectifier will be a function of the impedances of these two cases, as in (2).

$$Z_{in} = f(Z_{in,ON}, Z_{in,OFF}) \tag{2}$$

where $Z_{in,OFF}$ is the average input impedance of the rectifier at the first case, $Z_{in,ON}$ is the average input impedance when both diodes are turned off. Hence, these two impedances can be calculated as follow:

$$Z_{in,OFF} = \frac{Z_{D,OFF}^2}{2Z_{D,OFF}} + \frac{1}{JC_1\omega} = \frac{Z_{D,OFF}}{2} + \frac{1}{JC_1\omega} \tag{3}$$

$$Z_{in,ON} = \frac{Z_{D,OFF} \times Z_{D,ON}}{Z_{D,OFF} + Z_{D,ON}} + \frac{1}{JC_1\omega} \tag{4}$$

where $Z_{D,OFF}$, $Z_{D,ON}$ are the average impedances of the diodes in both cases, respectively. The rectifier input impedance is estimated due to the power analysis as follow:

$$P_{in} = \frac{1}{T}\int_0^T \frac{V_{in}^2}{Z_{in}}dt \tag{5}$$

Due to Fig.3, the integral of (5) can be represented as

$$P_{in} \approx \frac{2}{T}\left(\int_0^{t_1} \frac{V_{in}^2}{Z_{in,OFF}}dt + \int_{t_1}^{T/4} \frac{V_{in}^2}{Z_{in,ON}}dt + \int_{T/4}^{T/2} \frac{V_{in}^2}{Z_{in,OFF}}dt\right) \tag{6}$$

The time t_2 in Fig. 3 is approximated by T/4 and used in the integral, on the other hand, $V_{in} = V_m \sin(\omega t)$ is substituted in (6) to get (7) as the follow:

$$P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4} + t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right] + \frac{1}{Z_{in,ON}}\left[\frac{T}{4} - t_1 + \frac{1}{2\omega}sin(2\omega t_1)\right]\right] \tag{7}$$

By considering (5, 7), when the input is the same as V_{in}, the rectifier impedance will be:

$$Z_{in} \approx \frac{T}{2} \times \left[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4} + t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right] + \frac{1}{Z_{in,ON}}\left[(\frac{T}{4} - t_1 + \frac{1}{2\omega}sin(2\omega t_1)\right]\right]^{-1} \tag{8}$$

Based on Fig. 3, t_1 is changed from t_1 to about T/4 and its value in each cycle can be expressed as

$$t_1 = \frac{1}{\omega}sin^{-1}\left[\frac{V_{th} + \frac{V_{out}}{2}}{V_m}\right] \tag{9}$$

Since V_{C1} is replaced by $\frac{V_{out}}{2}$

$$V_{out} = 2(V_m - V_{th}) \tag{10}$$

By substituting $\omega = 2\frac{\pi}{T}$, the voltage multiplier input impedance can be calculated as a function of the output voltage (V_{out}) and V_m through (8, 9) as shown in (11).

$$Z_{in} \approx 2\left[\left(\frac{1}{Z_{in,OFF}} + \frac{1}{Z_{in,ON}}\right) + \frac{1}{\pi}\left(\frac{1}{Z_{in,OFF}} - \frac{1}{Z_{in,ON}}\right) * \left[2sin^{-1}\left(\frac{2V_{th} + V_{out}}{2V_m}\right) - sin\left(2sin^{-1}\left(\frac{2V_{th} + V_{out}}{2V_m}\right)\right)\right]\right]^{-1} \tag{11}$$

The full analysis for the voltage multiplier input impedance is mentioned in the appendix. The amplitude voltage of the power source has an internal resistance of 50Ω can be calculated as follow:

$$V_m = 10^{\frac{P(dBm)-10}{20}} \tag{12}$$

In Fig. 2, the average value of the applied voltage is - $\frac{4V_m}{\pi}$ in the off region when the maximum applied voltage is $2V_m$ over the rectifier diodes. For the ON region, the applied voltage across the diodes will be near to the threshold voltage (V_{th}).

III. CIRCUIT DESIGN

For designing the rectifier for RF energy harvesting, the most important issue is that choosing a suitable diode. The rectifier requires diodes to have low forward voltage, fast switching at high frequencies, the ability to operate at low input power level, low junction capacitance, low saturation current, and optimum input impedance. Obtaining an ideal diode to meet these requirements is not an easy process. However, choosing the most suitable one for a wide input power range is necessary. HSMS-2852 and HSMS-2862 Schottky diodes which belong to HSMS-285x, HSMS-286x series respectively mostly match the requirements of the proposed design. By referring to the diodes datasheets [20], [21] there are some important specifications that are provided in Table 1.

Where V_J is junction voltage, C_{JO} is junction capacitance at zero bias, I_s is saturation current, I_b is externally applied bias current, n is ideality factor, R_s is series resistance, and m is grading coefficient. Besides, the Schottky diode's equivalent circuit is mentioned in the datasheet to describe the

TABLE 1. **HSMS-2852 and HSMS-2862 Schottky diodes specifications.**

Parameter Units	HSMS-2852	HSMS-2862
V_J (V)	0.35	0.65
C_{JO} (pF)	0.18	0.18
EG (eV)	0.69	0.69
I_s (A)	3 E-6	5 E-8
n	1.06	1.08
R_s (Ω)	25	6
m	0.5	0.5
L_P (nH)	2	2
C_P (pF)	0.08	0.08

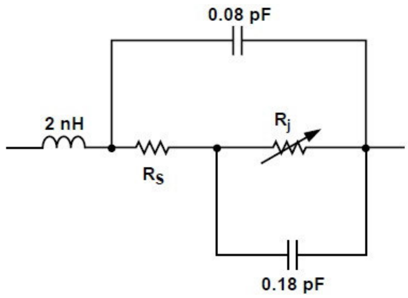


FIGURE 4. **The equivalent circuit of HSMS-2852 and HSMS-2862 Schottky diodes [20], [21].**

diode performance as depicted in Fig. 4. Agilent Avago Technology provides many types of diode packages. For reducing the circuit size, HSMS-2852, HSMS-2862 Schottky diode packages were used since the single package includes two diodes that are connected in series i.e a single HSMS-2852 package equal two packages of HSMS-2850.

To design an accurate model, the package parasitic elements were taken into consideration; the parasitic elements were represented by L_P and C_P. Equation (11) is used to calculate the rectifier input impedance at any applied input power level, therefore $Z_{in,ON}$ and $Z_{in,OFF}$ must be calculated, but that requires calculating both R_J, I_b, C_J, z_d, and Z_D since R_J, I_b, C_J, z_d, and Z_D are the diode junction resistance, externally applied bias current, junction capacitance, the diodes' average impedances, and the diodes' average impedances including the parasitic elements in the two cases (ON, and OFF regions) respectively.

$$R_J = \frac{8.33 \times 10^{-5} nT}{I_b + I_s} \tag{13}$$

where T = temperature °K.

$$I_b = I_s\left(e^{\frac{V_a}{nV_T}} - 1\right) \tag{14}$$

where V_T, V_a are the thermal voltage and the applied voltage to the diode respectively.

$$C_J = \frac{C_{JO}}{\left(1 - \frac{V_a}{V_J}\right)^m} \tag{15}$$

$$z_d = R_s + \frac{R_J}{1 + j\omega R_J C_J} \tag{16}$$

$$Z_D = \frac{z_d}{1 + j\omega z_d C_p} + j\omega L_p \tag{17}$$

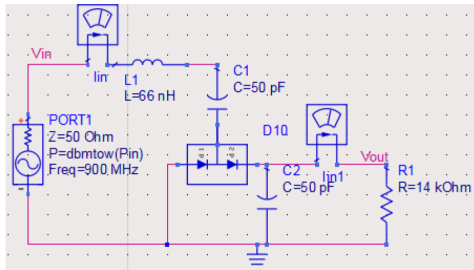


FIGURE 5. **A single-stage of Dickson rectifier with L matching for the low input power range.**

Advanced Design System (ADS) 2017 simulation program - Harmonic Balance simulation controller (HB) was used for simulation processes in this work. The power source with 50Ω internal impedance was used instead of the receiving antenna. All simulation processes were adjusted at the 900 MHz frequency band.

A. THE LOW INPUT POWER RANGE CIRCUIT DESIGN

For the low input power range (-50 dBm to 0 dBm), the Dickson rectifier topology circuit was designed by using HSMS-2852 as shown in Fig. 5 with L impedance matching. A single-stage to four-stage was designed and simulated. The voltage multiplier input impedance was obtained theoretically and numerically by the ADS simulation environment.

B. THE HIGH INPUT POWER RANGE CIRCUIT DESIGN

For the high input power range (0 dBm to 30 dBm), different stages were tested included 3, 4, 5, 6, and 7 stages by using HSMS-2852 and HSMS-2862 diodes separately to realize which diode and which the number of stages gets the optimum efficiency in the proposed design. Fig.6 shows the five-stage Dickson rectifier with L matching.

C. THE WIDE INPUT POWER RANGE CIRCUIT DESIGN

In this setup, the high and low input power circuits were combined to achieve a wide range of input power levels. HSMS-2852 was used in the low range rectifier whereas HSMS-2862 was used in the high range rectifier with the same power source. The output of the two circuits was wired through R_L as shown in Fig. 7. The capacitors' values in the two-stage rectifier inside the wide range circuit were modified to be 10 pF to enhance the efficiency of the entire wide range circuit. Different load values for the wide input power range circuit have been tested, most of these values were extracted from the mentioned published results in Table 2. The values were 5 kΩ, 10 kΩ [15], [16], 25 kΩ [14], and 100 kΩ [19] to find the best load for the wide range circuit.

IV. SIMULATION RESULTS AND DISCUSSION

At the low input power range (−50 dBm to 0 dBm) circuit, the single-stage showed the best rectifier input impedance (Z_{in}) vs. the input power (P_{in}) among the other stages. This impedance had more stability and included a capacitive

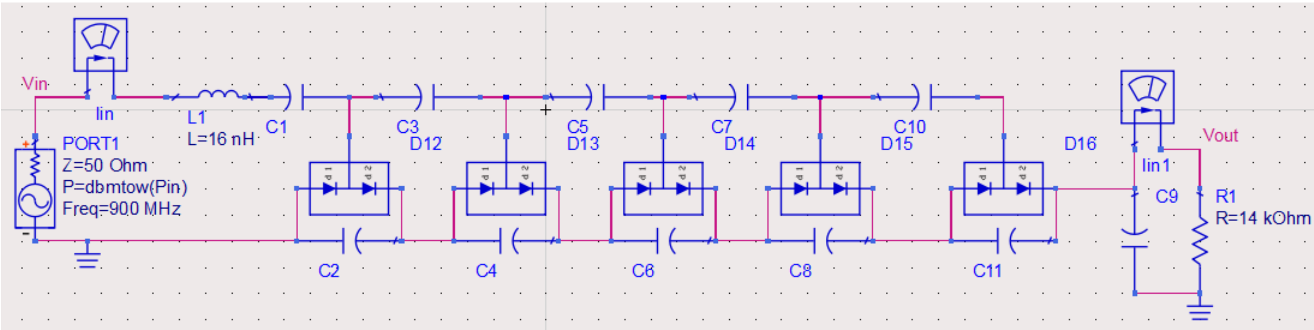


FIGURE 6. Five-stage of Dickson rectifier with L matching for the high input power range.

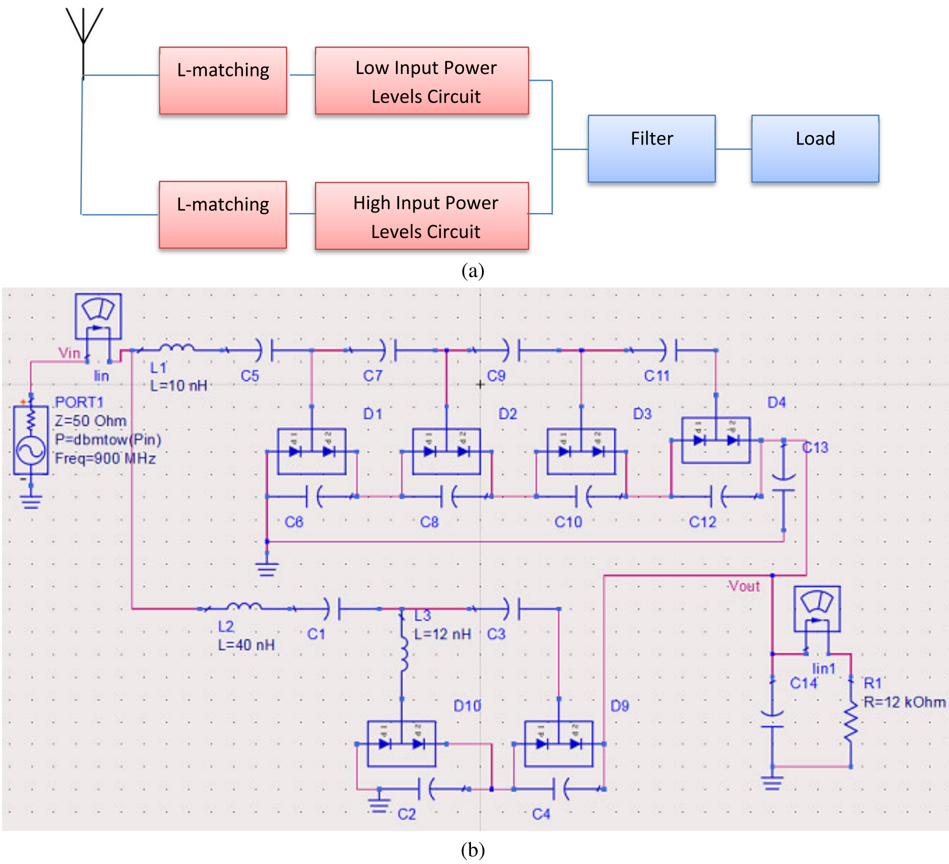
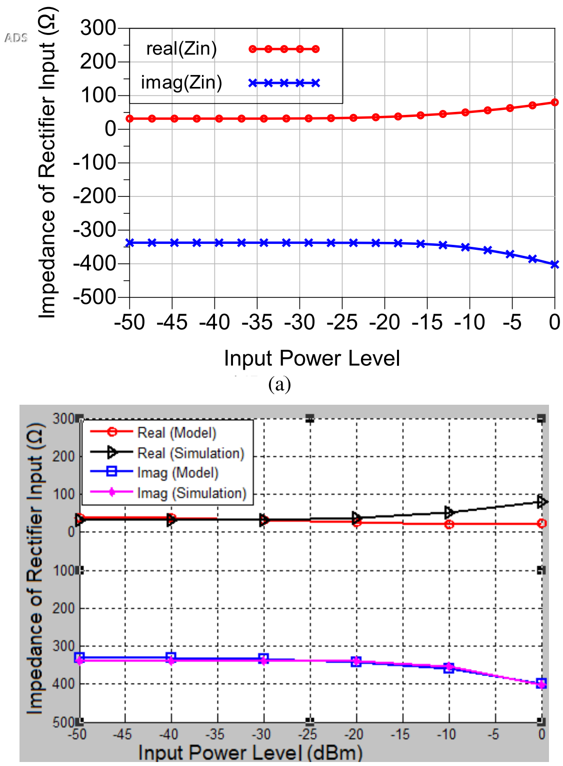


FIGURE 7. The proposed RF energy harvesting design for the wide input power range. (a) Block diagram. (b) The designed circuit.

reactance as shown in Fig.8 due to the diode junction capacitance. The imaginary part exceeded -300Ω, the same impedance had a real part below 60Ω which was close to the power source impedance. Based on the Z_{in} curve, the inductance L was swept between 0.5 nH to 90 nH to eliminate the imaginary part. The inductor 66 nH achieved the optimum matching for this topology. From Fig. 8, there is a good agreement between the results of the theoretical model and the simulation design for the single-stage voltage multiplier at the low input power range. The RF-DC conversion efficiency (η) was calculated via the Harmonic Balance simulation results by the below equation [14]:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2}{R_L} \times \frac{1}{P_{in}} \tag{18}$$

where P_{in} is the input power, P_{out} is the harvested power, and V_{out} is the output voltage across R_L. The peak conversion efficiency was achieved at -15 dBm and 0 dBm with 44.121% and 44.32% respectively as shown in Fig.9. After the input power level of -15 dBm, the efficiency was degraded due to the high power limitations of the HSMS-2852 diode. Figs.10 and 11 show the obtained output voltage and current



(a)

(b)

FIGURE 8. Impedance of rectifier input vs. low input power range. (a) simulation result. (b) theoretical and simulation result.

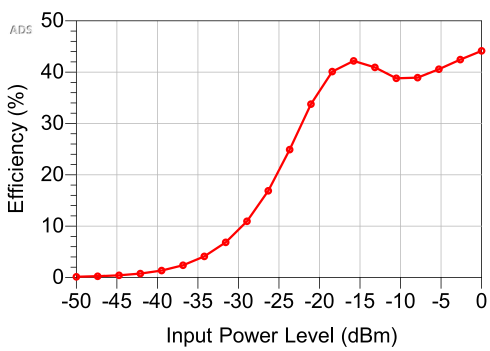


FIGURE 9. RF-DC conversion efficiency vs. low input power level range.

vs. low P_{in}. Considering the relevant curves, it is noticed that both the voltage and current are increased gradually.

In the high input power range (0 dBm to 30 dBm) circuit, results indicated that number of stages affected the total impedance of the rectifier, therefore, the impedance matching element was swept between 0.5 nH to 90 nH during the different stages to remove the imaginary part then investigate the optimum matching since increasing the number of the stages reduced this impedance especially for the imaginary part as shown in Figs. 12, 13.

For the comparison between the two diodes used in this design, HSMS-2862 diode was more suitable than HSMS-2852 for designing the high input power range circuit

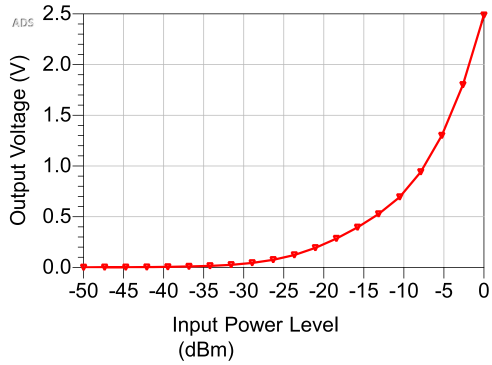


FIGURE 10. Output voltage vs. low input power level range.

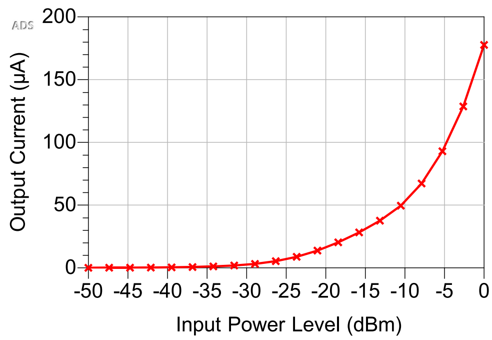


FIGURE 11. Output current vs. low input power level range.

since the different tested stages by using HSMS-2852 demonstrated high efficiency at the low input power levels whereas they got degraded at the high input power range as shown in Fig. 14, this is due to manufacturing specifications of HSMS-285X which are more suitable for low power ranges. On the other hand, when the different stages were tested by using HSMS-2862, according to the depicted Fig. 15 it can be noticed that if we consider the highest efficiency among the different stages circuits, then the five-stage circuit achieved this target by 79.9% at 15 dBm, but considering the efficiency for the comprehensive interested range of the applied input power levels, then the five and six-stage circuits had better efficiency than the three and four-stage circuits; also they had better evaluation than the seven-stage circuit based on the conversion efficiency and the design size. The trade-off became between the five and six-stage circuits since the five-stage circuit achieved 42.88%, 71.59%, 50.89%, and 7.68% for 0, 10, 20, and 30 dBm respectively with optimum inductance of 16 nH whereas the six-stage circuit achieved 37.04%, 69.48%, 55.23%, and 10.02% for 0, 10, 20, and 30 dBm respectively with optimum inductance of 15 nH. The five-stage circuit achieved higher efficiency than the six-stage circuit at 0 dBm and 10 dBm although it achieved less than the six-stage circuit at 20 dBm and 30 dBm. The five-stage circuit realized the highest efficiency by 79.9% whereas the six-stage circuit realized the highest efficiency by 78.55%. Another problem is that the six-stage circuit occupied a larger size than the five-stage circuit hence we think that the five-stage circuit is the best choice based on this evaluation.

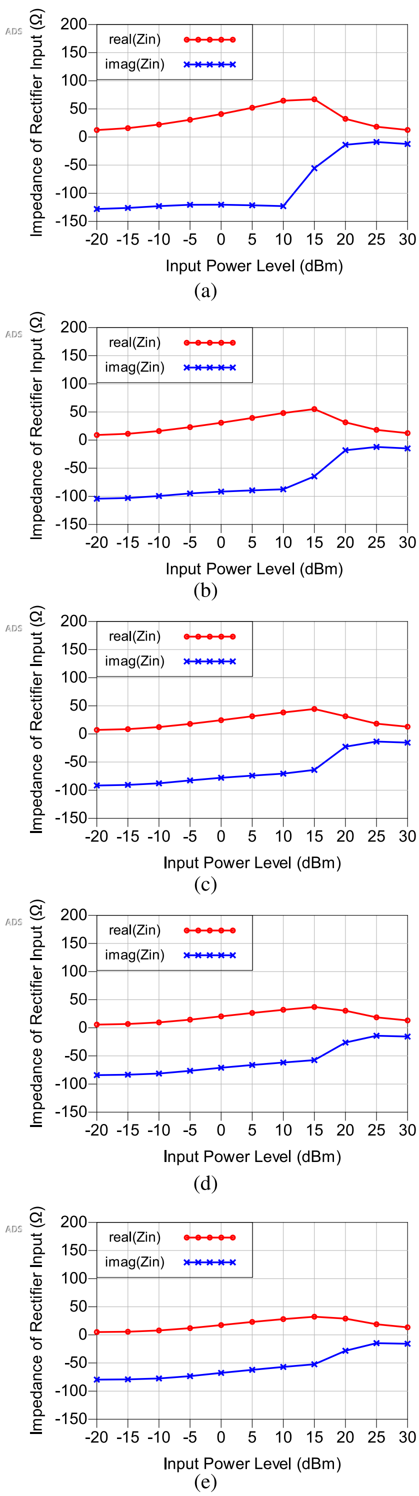


FIGURE 12. **Impedance of rectifier input vs. high input power level range for HSMS-2852 at different stages. (a)Three-stage. (b)Four-stage. (c)Five-stage. (d)Six-stage. (e) Seven-stage.**

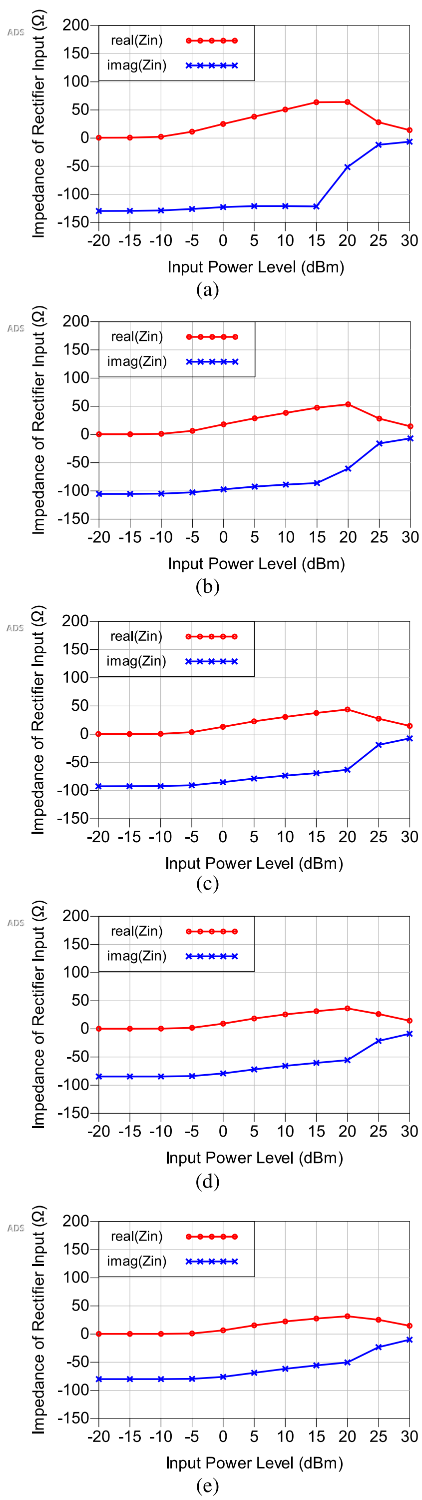


FIGURE 13. **Impedance of rectifier input vs. high input power level range for HSMS-2862 at different stage. (a)Three-stage. (b)Four-stage. (c)Five-stage.(d)Six-stage.(e) Seven-stage.**

In fact, the variation of the rectifier input impedance based on the applied input power levels results in dynamic impedance for the diodes in the circuit besides the number of the stages has the same effect on the total rectifier impedance then a dynamic impedance exists at the rectifier input, another point related to this issue is that an increase in the number of stages leads to an increase in the number of diodes in the circuit i.e. increased voltage drops across these diodes, consequently more power is lost. As a result, the conversion efficiency is affected negatively, that is why when the number

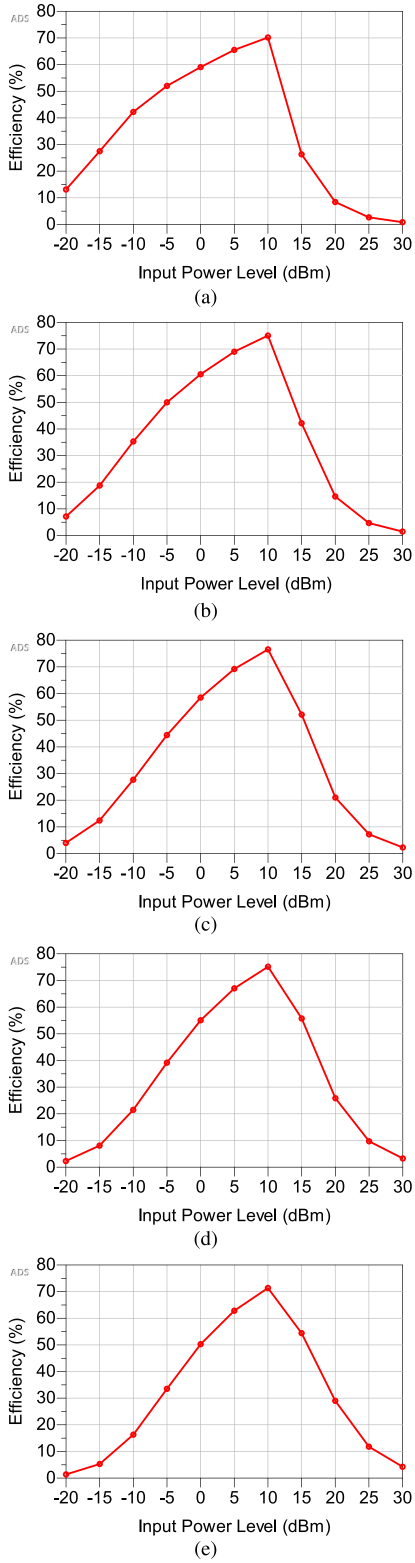


FIGURE 14. RF-DC conversion efficiency vs. high input power level range for HSMS-2852 at different stages. (a)Three-stage. (b)Four-stage. (c)Five-stage.(d)Six-stage.(e) Seven-stage.

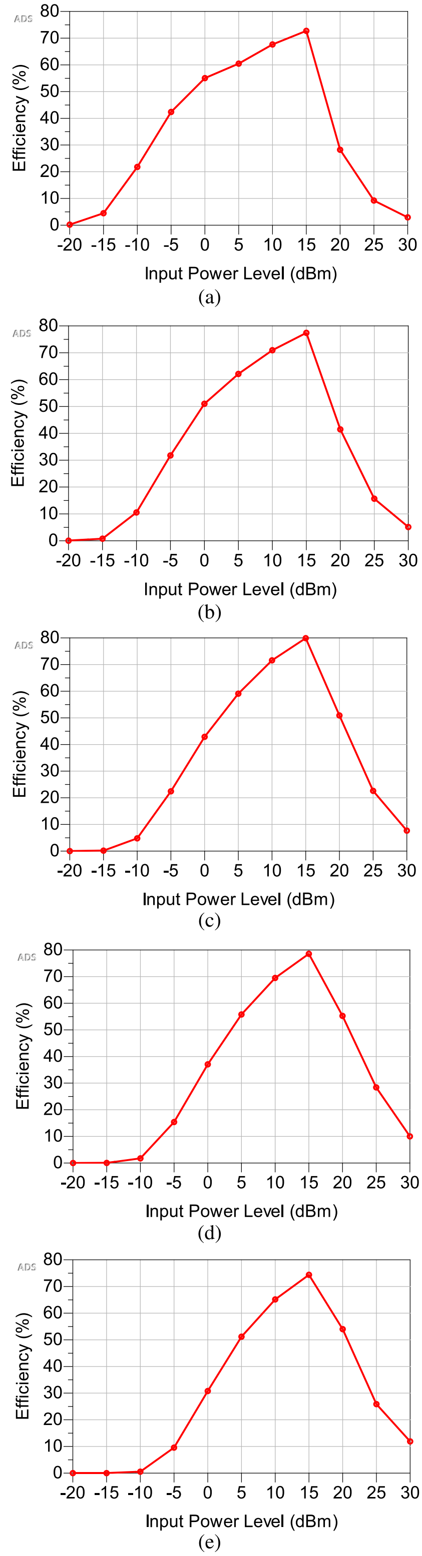


FIGURE 15. RF-DC conversion efficiency vs. high input power level range for HSMS-2862 at different stages. (a)Three-stage. (b)Four-stage. (c)Five-stage. (d)Six-stage. (e) Seven-stage.

of the stages is increased more than six stages in the current design, it leads to degradation of the conversion efficiency of the energy harvesting system. Besides in [16], the researcher tested numerically by ADS software the system conversion efficiency for different stages from 1 to 12, the obtained results by the researcher indicated that increasing the number

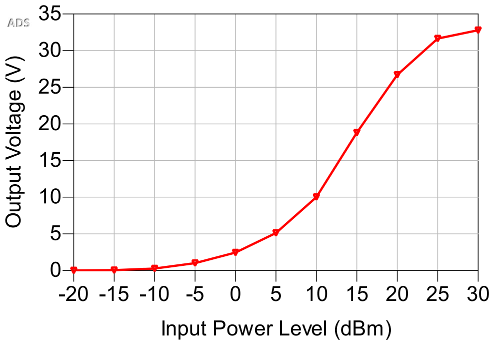


FIGURE 16. **Output voltage vs. high input power level range for the five-stage circuit with HSMS-2862.**

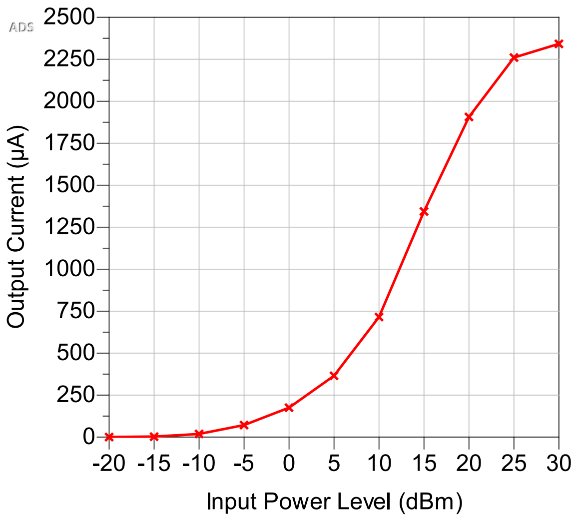


FIGURE 17. **Output current vs. high input power level range for the five-stage circuit with HSMS-2862.**

of stages did not cause a significant change in the conversion efficiency but, this increase may lead to a bulky and expensive circuit. The obtained peak output voltage and current for the high input power range based on Figs. 16, 17 were 32.78 V and 2.34 mA at +30 dBm.

A combination of the two circuits in one circuit for the wide input power range resulted in dynamic impedance at the input and output of the rectifier which affected the RF-DC conversion efficiency. Therefore, the values of the inductors were modified to match the input impedance of the wide range circuit. Both the four and five-stage designs for the high power levels in the wide range circuit were tested separately and the obtained results indicated that a little enhancement was achieved by the five-stage compared to the four-stage circuit resulted in larger design size, for this reason, we preferred to use the four-stage in the wide range circuit, however the five and six-stage rectifiers are more attractive and effective than other stages for the high input power ranges only. Z_{in} vs. P_{in} at the load of 14 $K\Omega$ as an example is shown in Fig. 18 for the wide input power range circuit. This impedance had stability from −40 dBm to +10 dBm. Besides, it had a capacitive reactance that was below −80Ω and the real part was

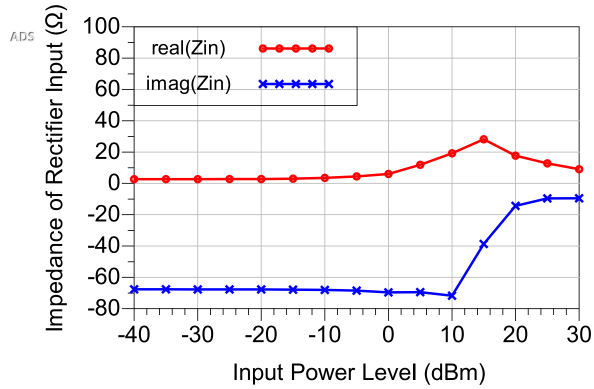


FIGURE 18. **Impedance of rectifier input vs. input power level for the wide range rectifier circuit at the load of 14 $K\Omega$.**

below 50Ω. By reference to Z_{in} curves, L matching elements were swept between 0.5 nH to 90 nH. 10 nH and 40 nH were inserted for the high and low input power circuits inside the wide range circuit. These inductors introduced the suitable matching since 59.18% was reached as the peak conversion efficiency at 0 dBm for the mentioned load.

Results of the wide input power range circuit at different loads are shown in Figs. 20, 21, and 22 which indicated that 5 kΩ, 10 kΩ, 14 kΩ, and 25 kΩ demonstrated convergent results for the maximum obtained efficiency which were 59.75 %, 59.46 %, 59.17 %, and 56.72% at 10 dBm, 0d Bm, 0 dBm, and −5 dBm respectively, whereas the load of 100 kΩ showed a maximum efficiency with a low quality of 33.33 % at −15 dBm as shown in Fig. 19.

Considering the comprehensive efficiency for the different levels in the wide input power range, it can be noticed that the loads 10 kΩ, 14 kΩ achieved the optimum performance, just the difference between these loads is that 14 kΩ realized higher efficiency than 10 kΩ at the low input power levels especially at −20 dBm, −10 dBm levels whereas it achieved the vice versa for the high input power levels especially at 10dBm, 20dBm levels. The main reason for the efficiency variation at the different power levels is based on the dynamic complex impedance which includes the impedance matching element, the rectifier impedance, and the load resistor. To achieve a balanced overall efficiency for both the high and low input power levels in the wide input power range circuit, a load of 12 kΩ which is a middle value between the 10 kΩ and 14 kΩ loads can be be used. The RF-DC conversion efficiency at the suggested load of 12 kΩ is shown in Fig. 20, however, this load achieved 60 % as the highest efficiency for the wide input power range circuit at 0 dBm. The resulted output voltage and current vs. P_{in} are shown in Figs. 21, 22 for the wide input power range. Through the above curves, it is noticed that 22 mV and 1.87μA were the minimum values extracted at -30 dBm where 16.56 V and 1.39 mA were the peak values at +30 dBm.

A. COMPARISON WITH PUBLISHED RESULTS

The results of this work compared with the published results, [1], [14]–[19] achieves a wider input power range

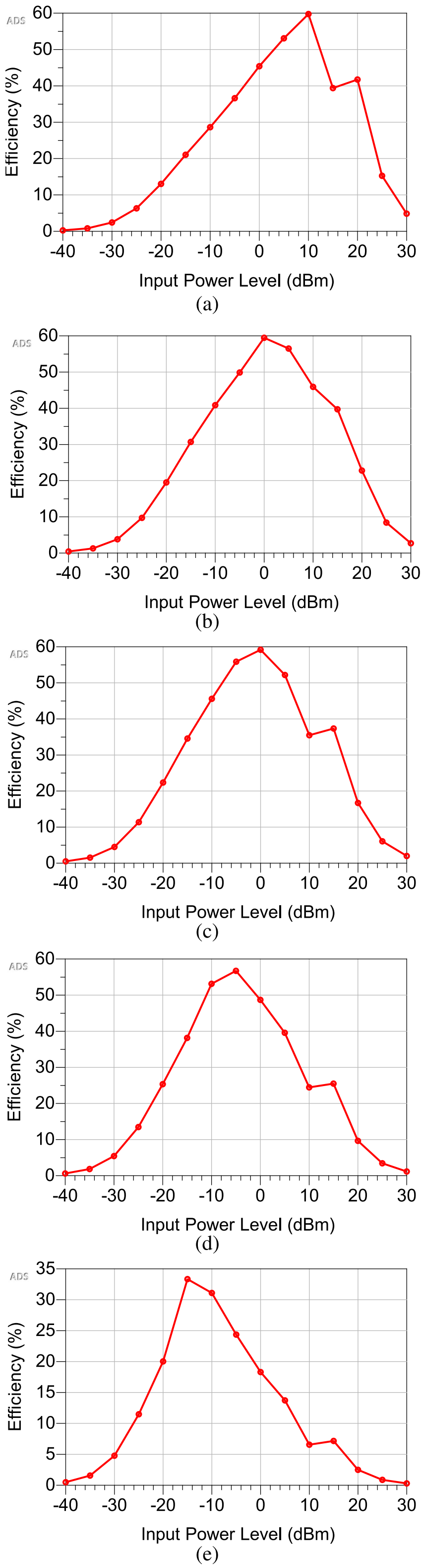


FIGURE 19. RF-DC conversion efficiency vs. input power level for the wide range circuit at different loads. (a) At 5 $K\Omega$. (b) At 10 $K\Omega$. (c) At 14 $K\Omega$. (d) At 25 $K\Omega$. (e) At 100 $K\Omega$.

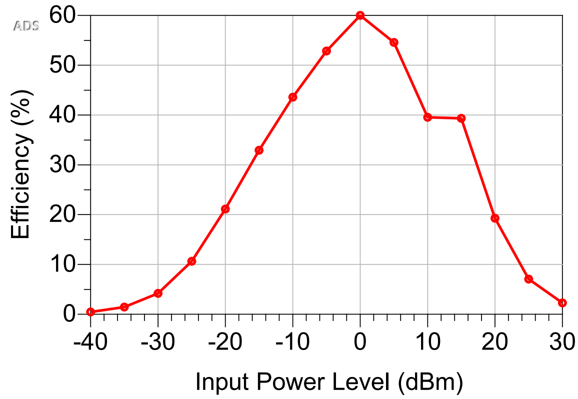


FIGURE 20. RF-DC conversion efficiency vs. input power level for the wide range circuit at the suggested load of 12 $K\Omega$.

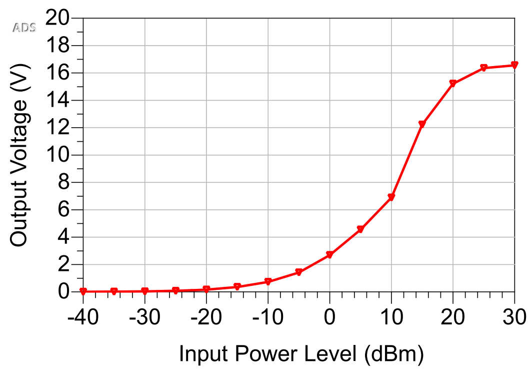


FIGURE 21. Output voltage vs. input power level for the wide range circuit at 12 $K\Omega$.

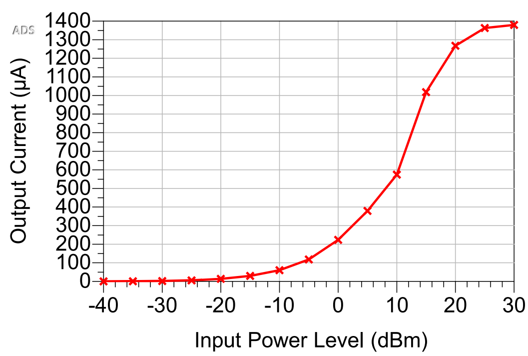


FIGURE 22. Output current vs. input power level for the wide range circuit at 12 $K\Omega$.

with a simple design, especially for the matching element. Acceptable conversion efficiency was obtained compared with the other works. Table 2 shows a comparison for the conversion efficiency between the other works and this work.

The published works in Table 2 which used simulation and experimental, they mentioned that results indicated that a good agreement between the simulation and experimental. Finally, in this work, we have handled both the high and the low power levels not only the sufficiently high power levels since most the published results considered high levels such in [3], [17] or limited levels range as mentioned in [1], [3], [11], [14], [15], [17], and [18], this goal was done by utilizing Dickson voltage multiplier which is classified as one of the voltage multiplier topologies.

TABLE 2. A comparison for the conversion efficiency between the published results and this study.

Ref.	Freq. Band	$P_{in} Range(dBm)$ From	To	Max Efficiency
[14]	GSM 900 MHz	- 10	+ 10	44.8% at +10 dBm [a]
[15]	850 MHz	-30	-10	38% at -10 dBm [a,b]
[16]	900 MHz	-40	+ 10	45 at 0 dBm [a,b]
[18]	900 MHz	-20	+ 10	39% at 0 dBm [b]
[19]	1 GHz	-18	-10	65% at -18 dBm [a,b]
This Study	900 MHz	-40	+ 30	60% at 0 dBm

V. CONCLUSION

This work aimed to design a wide input power range for the RF energy harvesting system at the 900 MHz band with reasonable efficiency since the applied input power level is changed due to different reasons. To achieve this goal, the proposed design passed through three stages: first, design the low input power range circuit with a single-stage Dickson voltage multiplier by using HSMS-2852 Schottky diode. Second, design the high input power range circuit by utilizing HSMS-2862 Schottky diode. Finally, the wide range power circuit was created by combining the low and the high input power circuits as a wide range circuit. L impedance matching was used in the three circuits to reduce the power loss and then getting the optimum efficiency. For the low input power circuit, 43.6 % conversion efficiency was achieved at 0 dBm where 79.9% was reached at + 15 dBm for the high input power level. The wide range circuit accomplished 60 % as the peak efficiency at 0 dBm with the output voltage and current of 16.56 V and 1.39 mA respectively for the load resistance of 12KΩ. Future studies will include the usage of Momentum simulator in ADS software to evaluate and consequently propose methods to overcome challenges in RF energy harvesting. Furthermore, this will help to achieve practical and industry-ready designs. Our work mainly aims to elaborate on the theoretical and simulation progress, and at the same time enhancing the conversion efficiency for multiple frequency bands.

APPENDIX

$$P_{in} \approx \frac{2}{T}\left(\int_0^{t_1} \frac{V_{in}^2}{Z_{in,OFF}}dt + \int_{t_1}^{T/4} \frac{V_{in}^2}{Z_{in,ON}}dt + \int_{T/4}^{T/2} \frac{V_{in}^2}{Z_{in,OFF}}dt\right) \tag{A.1}$$

$$V_{in} = V_m sin(\omega t) \tag{A.2}$$

$$P_{in} \approx \frac{2}{T}\left(\int_0^{t_1} \frac{\left(V_m sin(\omega t)\right)^2}{Z_{in,OFF}}dt + \int_{t_1}^{T/4} \frac{\left(V_m sin(\omega t)\right)^2}{Z_{in,ON}}dt + \int_{T/4}^{T/2} \frac{\left(V_m sin(\omega t)\right)^2}{Z_{in,OFF}}dt\right) \tag{A.3}$$

$$P_{in} \approx \frac{2}{T}\left(\int_0^{t_1} \frac{V_m^2 sin^2(\omega t)}{Z_{in,OFF}}dt + \int_{t_1}^{T/4} \frac{V_m^2 sin^2(\omega t)}{Z_{in,ON}}dt + \int_{T/4}^{T/2} \frac{V_m^2 sin^2(\omega t)}{Z_{in,OFF}}dt\right) \tag{A.4}$$

$$P_{in} \approx \frac{2V_m^2}{T}\left(\int_0^{t_1} \frac{sin^2(\omega t)}{Z_{in,OFF}}dt + \int_{t_1}^{T/4} \frac{sin^2(\omega t)}{Z_{in,ON}}dt + \int_{T/4}^{T/2} \frac{sin^2(\omega t)}{Z_{in,OFF}}dt\right) \tag{A.5}$$

$$P_{in} \approx \frac{2V_m^2}{T}\left(\frac{1}{Z_{in,OFF}}\left[\int_0^{t_1} sin^2(\omega t)dt + \int_{T/4}^{T/2} sin^2(\omega t)dt\right] + \frac{1}{Z_{in,ON}}\int_{t_1}^{T/4} sin^2(\omega t)dt\right) \tag{A.6}$$

$$P_{in} \approx \frac{2V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\frac{1}{2}\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_0^{t_1} + \frac{1}{2}\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{T/2}^{T/4}\right] + \frac{1}{Z_{in,ON}}\left[\frac{1}{2}\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{t_1}^{T/4}\right]\right] \tag{A.7}$$

$$P_{in} \approx \frac{2V_m^2}{T} \times \frac{1}{2}\left[\frac{1}{Z_{in,OFF}}\left[\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_0^{t_1} + \left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{T/2}^{T/4}\right] + \frac{1}{Z_{in,ON}}\left[\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{t_1}^{T/4}\right]\right] \tag{A.8}$$

$$P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_0^{t_1} + \left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{T/2}^{T/4}\right] + \frac{1}{Z_{in,ON}}\left[t - \frac{1}{2\omega}sin(2\omega t)\right]_{t_1}^{T/4}\right] \tag{A.9}$$

$$P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\left[\left(t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right) - (0)\right] + \left[\left(\frac{T}{2} - \frac{1}{2\omega}sin(2\omega\frac{T}{2})\right) - \left(\frac{T}{4} - \frac{1}{2\omega}sin(2\omega\frac{T}{4})\right)\right]\right] + \frac{1}{Z_{in,ON}}\left[\left(\frac{T}{4} - \frac{1}{2\omega}sin(2\omega\frac{T}{4})\right) - \left(t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right)\right]\right] \tag{A.10}$$

$$P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\left[t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right] + \left[\left(\frac{T}{2} - \frac{1}{2\omega}(0)\right) - \left(\frac{T}{4} - \frac{1}{2\omega}(0)\right)\right]\right] + \frac{1}{Z_{in,ON}}\left[\left(\frac{T}{4} - \frac{1}{2\omega}(0)\right) - \left(t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right)\right]\right] \tag{A.11}$$

$$P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[t_1 - \frac{1}{2\omega}sin(2\omega t_1) + \frac{T}{2} - \frac{T}{4}\right] + \frac{1}{Z_{in,ON}}\left[\frac{T}{4} - t_1 + \frac{1}{2\omega}sin(2\omega t_1)\right]\right] \tag{A.12}$$

$$\therefore P_{in} \approx \frac{V_m^2}{T}\left[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4} + t_1 - \frac{1}{2\omega}sin(2\omega t_1)\right]\right.$$

$$+\frac{1}{Z_{in,ON}}\left[\frac{T}{4}-t_1+\frac{1}{2\omega}sin(2\omega t_1)\right]\Bigg] \tag{A.13}$$

$$P_{in} = \frac{1}{T}\int_0^T \frac{V_{in}^2}{Z_{in}}dt = \frac{1}{TZ_{in}}\int_0^T V_{in}^2 dt \tag{A.14}$$

$$P_{in} = \frac{1}{TZ_{in}}\int_0^T (V_m sin(\omega t))^2 dt \tag{A.15}$$

$$P_{in} = \frac{1}{TZ_{in}}\int_0^T V_m^2 sin^2(\omega t)dt \tag{A.16}$$

$$P_{in} = \frac{V_m^2}{TZ_{in}}\int_0^T sin^2(\omega t)dt \tag{A.17}$$

$$P_{in} = \frac{V_m^2}{TZ_{in}} \times \frac{1}{2}\left[t-\frac{1}{2\omega}sin(2\omega t)\right]_0^T \tag{A.18}$$

$$P_{in} = \frac{V_m^2}{TZ_{in}} \times \frac{1}{2}\left[(T-\frac{1}{2\omega}sin(2\omega T))-(0)\right] \tag{A.19}$$

$$P_{in} = \frac{V_m^2}{TZ_{in}} \times \frac{1}{2}\left[(T-\frac{1}{2\omega}(0))-(0)\right] \tag{A.20}$$

$$P_{in} = \frac{V_m^2}{TZ_{in}} \times \frac{1}{2}T \tag{A.21}$$

$$P_{in} = \frac{V_m^2}{2Z_{in}} \tag{A.22}$$

$$\therefore Z_{in} = \frac{V_m^2}{2P_{in}} \tag{A.23}$$

By substituting (A.13) in (A.23), Z_{in} can be obtained as follow:

$$Z_{in} \approx \frac{V_m^2}{2} \times \frac{1}{[}\frac{V_m^2}{T}[\frac{1}{Z_{in,OFF}}[\frac{T}{4}[+t_1-\frac{1}{2\omega}sin(2\omega t_1)] + \frac{1}{Z_{in,ON}}[(\frac{T}{4}-t_1+\frac{1}{2\omega}sin(2\omega t_1)]]]]] \tag{A.24}$$

$$Z_{in} \approx \frac{T}{2} \times \left[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4}\right]+t_1-\frac{1}{2\omega}sin(2\omega t_1)\right] + \frac{1}{Z_{in,ON}}\left[(\frac{T}{4}-t_1+\frac{1}{2\omega}sin(2\omega t_1)\right]^{-1} \tag{A.25}$$

$$\because t_1 = \frac{1}{\omega}sin^{-1}g[\frac{V_{th}+\frac{V_{out}}{2}}{V_m}g] \tag{A.26}$$

$$Z_{in} \approx \frac{T}{2}\Bigg[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4}+\frac{1}{\omega}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) - \frac{1}{2\omega}sin\Big(2\omega\frac{1}{\omega}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right] + \frac{1}{Z_{in,ON}}\left[\frac{T}{4}-\frac{1}{\omega}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) + \frac{1}{2\omega}sin\Big(2\omega\frac{1}{\omega}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right]\Bigg]^{-1} \tag{A.27}$$

since $\omega = 2\pi F = 2\frac{\pi}{T}$, then it can be written as follow:

$$Z_{in} \approx \frac{T}{2}\Bigg[\frac{1}{Z_{in,OFF}}\left[\frac{T}{4}+\frac{T}{2\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) - \frac{T}{4\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right] + \frac{1}{Z_{in,ON}}\left[\frac{T}{4}-\frac{T}{2\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) + \frac{T}{4\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right]\Bigg]^{-1} \tag{A.28}$$

$$Z_{in} \approx \frac{T}{2} \times \frac{4}{T}\Bigg[\frac{1}{Z_{in,OFF}}\left[1+\frac{2}{\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) - \frac{1}{\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right] + \frac{1}{Z_{in,ON}}\left[1-\frac{2}{\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) + \frac{1}{\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right]\Bigg]^{-1} \tag{A.29}$$

$$Z_{in} \approx 2\Bigg[\frac{1}{Z_{in,OFF}}\left[1+\frac{2}{\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) - \frac{1}{\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right] + \frac{1}{Z_{in,ON}}\left[1-\frac{2}{\pi}sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) + \frac{1}{\pi}sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\right]\Bigg]^{-1} \tag{A.30}$$

$$Z_{in} \approx 2\Bigg[\Big(\frac{1}{Z_{in,OFF}}+\frac{1}{Z_{in,ON}}\Big)+\frac{2}{\pi}\Big(\frac{1}{Z_{in,OFF}} - \frac{1}{Z_{in,ON}}\Big)sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big) + \frac{1}{\pi}\Big(\frac{1}{Z_{in,ON}} - \frac{1}{Z_{in,OFF}}\Big)sin\Big(2sin^{-1}\Big(\frac{V_{th}+\frac{V_{out}}{2}}{V_m}\Big)\Big)\Bigg]^{-1} \tag{A.31}$$

$$Z_{in} \approx 2\Bigg[\Big(\frac{1}{Z_{in,OFF}}+\frac{1}{Z_{in,ON}}\Big) + \frac{1}{\pi}\Big(\frac{1}{Z_{in,OFF}}-\frac{1}{Z_{in,ON}}\Big) * \left[2sin^{-1}\Big(\frac{2V_{th}+V_{out}}{2V_m}\Big) - sin\Big(2sin^{-1}\Big(\frac{2V_{th}+V_{out}}{2V_m}\Big)\Big)\right]\Bigg]^{-1} \tag{A.32}$$

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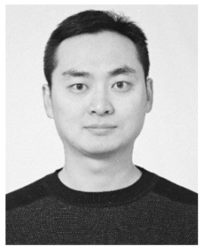

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