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# Matrix Converter Based on SVD Modulation Using a Microcontroller as Unique Controlling Device

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**ABSTRACT** In this paper, the implementation of a complete set of control algorithms for a three-phase Matrix Converter (MC) is addressed. The control algorithms are implemented on a single Microcontroller Unit (MCU) of the enhanced C2000 Delfino family of Texas Instruments (TI). By a suitable programming sequence, the MCU is capable of fully controlling the MC, which avoids the use of special hardware for assuring a reliable commutation process. The Singular Value Decomposition modulation (SVD) and the four-step current commutation technique, fundamental steps in this proposal, were implemented in the TMS320F28379D MCU device. The optimal algorithmic strategies and a proficient design allow a compact implementation in a single device. For validating this study, extensive numerical simulations were carried out, and an experimental prototype was efficiently implemented. Both kinds of results were discussed and analyzed to demonstrate the effectiveness of the proposed implementation.

**INDEX TERMS** Matrix converter, singular value decomposition, microcontroller unit, ac-ac converter.

## I. INTRODUCTION

The AC-AC power converters play an important role in the current operation of the power systems. The most relevant power devices carry out the AC-AC energy conversion by using several well-positioned topologies [1]. Some of them execute the conversion directly, solving the issues associated with the converters based on indirect energy conversion strategies [2]. Nowadays, the Matrix Converter (MC) is one of the most suitable devices that performs this task without using energy storage elements [3]. Some attractive features of the MC include a high-power density, bidirectional power flow, unity input power factor operation, among others [4]–[6]. The MC was initially proposed as motor driver [7]–[9], but due to its operational characteristics, in recent years it has been proposed for other interesting applications such as power quality compensators [10]–[12], wind-turbine controllers [13]–[15] multi-phase drive systems [16], [17], unified power flow controllers [18], and aircraft servicing [19]. The MC is an attractive device that opens the gate to many potential applications. Despite this fact, it exhibits some disadvantages related to the hardware implementation, complex control algorithms, and self-protection schemes, which has limited its wide utilization within the industrial sector [5]. Fortunately, through technological advances as well as the continuous research and development (R&D) between the academy and industry, these concerns have been successfully addressed [20]. Finally, an MC for practical applications is currently available in the market [21]. Regarding the MC control algorithms, these can be divided into two categories: the modulation strategies and the gate signal generation techniques. The modulation strategy is responsible for determining the times in which the bidirectional power switches (BDS) are activated, ''on'' state, or deactivated, ''off'' state, allowing the MC to generate the output voltages and input currents required for the application [22], [23]. These processing times are highly dependent on the input voltage signal, and in this case, the designer must deal with synchronization times and current flow trajectories to accomplish a precise control of the BDS [22]. On the other hand, the gate signal generation technique achieves a reliable transition between the respective BDS states governed by the modulation strategy [24], [25]. These transitions are mostly dependent on logical functions derived from measurements of the output current, input voltage, or both, simultaneously [26]–[28]. From many of the works reported in the specialized literature, it is possible to establish that the correct tuning of these algorithms is the most significant constraint

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for MC implementation. The central issues are due to the complex calculus required by most of the modulation strategies and the proper synchronization of processes, followed by parallel execution of the gate generation algorithms [29]. However, modern digital devices allow addressing these problems by different reliable means [30]. In order to carry out the implementation of this algorithms, the utilization of a digital signal processor (DSP) to perform the modulation operations in conjunction with a Field Programmable Gate Array (FPGA) to execute the gate signal generation is a very common configuration, as described in [19], [31], [32]. Another option is based on the relevance of the gate signal generation and the need for running in parallel, where the MC control algorithm is implemented on a single FPGA device as detailed in [33]–[36]. As it is observed from the cited papers, there is a high demand for devices able to run algorithms in parallel because of the gate signals generation stage, and to the best of authors knowledge, an approach that addresses the complete control of the MC along with the commutation of the bidirectional power switches, in an on-chip solution based on a DSP or MCU has not been presented before. In [37], the gate signals generation is efficiently carried out by an MCU device. The implementation is based on the enhanced pulse width modulation peripheral (PWM) incorporated in the same chip. Unlike this last work, this paper describes the full process for implementing the SVD modulation strategy [38] and the four-step current commutation method [24], algorithms utilized in an MC prototype based on a single low-cost MCU device. Additional details related to the required hardware for the prototype are also included. The rest of the paper is organized as follows: the MC foundations are presented in Section II, while the SVD modulation technique is described in Section III. The implementation of both MC control algorithms is detailed in Section IV, followed by the simulations and experimental results that validate the proposal, presented in Section V. Finally, the conclusions of this work are given in Section VI.

## II. MATRIX CONVERTER

The three-phase direct MC topology is shown in Fig. 1. The core is composed of nine bidirectional switches (BDS) $s_{ij}$, which fashion the matrix $\mathbf{S}$ (where $s_{ij} \in \{0, 1\}$ for $i \in \{A, B, C\}$ and $j \in \{a, b, c\}$). In this case, each one of the BDS is composed of two Insulated Gate Bipolar Transistor (IGBT) in a common-source configuration. Moreover, the input and output (LC) filters were designed to attenuate the high-order harmonics present in voltage and current signals. At the output terminals, a load composed of a resistor and an inductor (RL load) was coupled to test the functionality of the converter. By the proper commutation sequence of the nine BDS in the matrix $\mathbf{S}$, the MC directly links each one of the input voltages $V_{abc} = [v_a\ v_b\ v_c]^\intercal$ with each one of the output voltages $V_{ABC} = [v_A\ v_B\ v_C]^\intercal$. At the same time, the output currents $I_{ABC} = [i_A\ i_B\ i_C]^\intercal$ are linked with the input currents $I_{abc} = [i_a\ i_b\ i_c]^\intercal$. Only one BDS in each vertical arm of the MC must be closed at a given time to guarantee safe commutation, a condition that is established mathematically by $s_{ia} + s_{ib} + s_{ic} = 1$. The MC input-output relationships are described by (1).

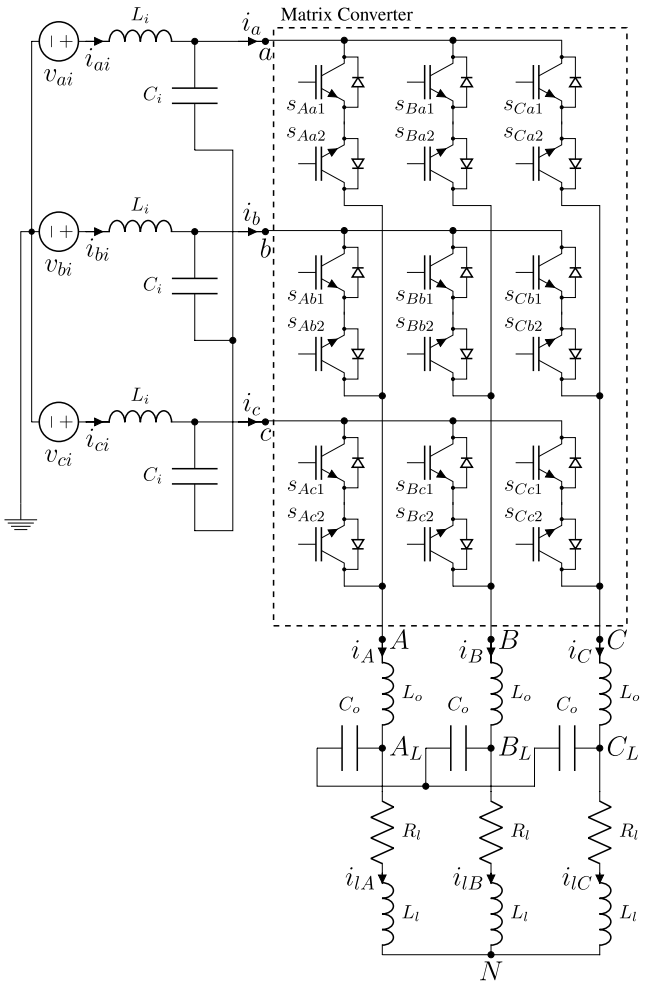


**FIGURE 1.** Matrix Converter (MC) circuit and peripherals.

$$V_{ABC} = SV_{abc},\ I_{abc} = S^\intercal I_{ABC},$$
$$S = \begin{bmatrix} s_{Aa} & s_{Ab} & s_{Ac} \\ s_{Ba} & s_{Bb} & s_{Bc} \\ s_{Ca} & s_{Cb} & s_{Cc} \end{bmatrix}. \quad (1)$$

It must be noticed that an MC vertical arm corresponds to a row of the matrix $\mathbf{S}$. For controlling the MC, several modulation techniques have been proposed in the literature [22], [23], [38], [39], where each one exhibits particular beneficial properties. Some of them are categorized as Direct Duty-Cycle Methods, where elements in matrix $\mathbf{S}$ are defined by their average values computed over a switching period ($T_{sw}$). This process is achieved and defined by matrix $\mathbf{M}$ as (2).

$$V_{ABC} = MV_{abc},\ I_{abc} = M^T I_{ABC},$$
$$M = \begin{bmatrix} m_{Aa} & m_{Ab} & m_{Ac} \\ m_{Ba} & m_{Bb} & m_{Bc} \\ m_{Ca} & m_{Cb} & m_{Cc} \end{bmatrix}, \quad (2)$$

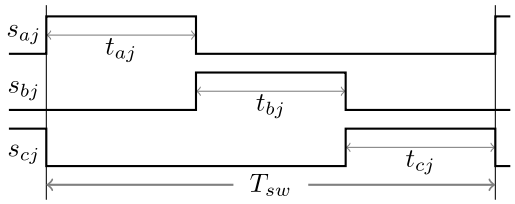


**FIGURE 2.** Single-side switching pattern for a duty-cycle modulation.

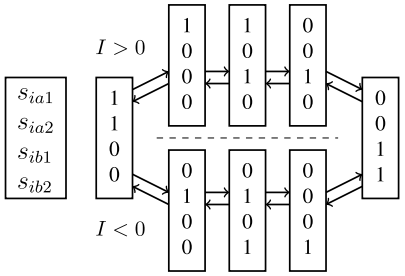


**FIGURE 3.** Four-Steps commutation technique (BDS transitions between $s_{ia}$ and $s_{ib}$).

where $m_{ij} \in [0, 1]$. The elements $m_{ij}$ are linked to a given time $t_{ij}$, while the BDS $s_{ij}$ is operating in the active state. This process is computed by (3).

$$t_{ij} = m_{ij}\, T_{sw}. \tag{3}$$

As previously mentioned, the condition $m_{ia} + m_{ib} + m_{ic} = 1$ should be fulfilled at any time to assure safe operation. Fig. 2 presents the signals involved in the commutation process for an MC arm over a period $T_{sw}$, where it was applied a single-side switching pattern. Accordingly, the modulation methods aim to solve the problem described by (2), where the elements of matrix $\mathbf{M}$ are determined from the knowledge of signals $V_{abc}$ and $I_{ABC}$, and by proposing reference signals for $V_{ABC}$ and $I_{abc}$. In addition to the application of matrix $\mathbf{M}$ into the MC (*cf.* Fig. 2), the transition between a pair of BDS is safely controlled by the four-step current commutation technique [24]. This procedure is shown in Fig. 3, which represents the transition between the BDS $s_{ia}$ and $s_{ib}$.

On the other hand, Fig. 4 shows all the signals involved in the transition between the BDS $s_{Aa}$ and $s_{Ab}$ for the corresponding MC arm. In the case of the off-going current (blue) and on-coming current (red), the process is described as follows: in the first step, the non-conducting switch of the off-going BDS is turned-off. Then, the on-coming conducting switch is turned-on (second step). In the third step, the off-going conducting switch is turned-off, and in the last step, the on-coming non-conducting switch is turned-on. Consequently, these steps are applied in parallel to the remaining arms of the MC.

## III. SINGULAR VALUE DECOMPOSITION MODULATION (SVD-M)

The SVD-M is a Direct Duty-Cycle modulation method originally proposed by Hojabri *et al.* [38]. The main objective of this strategy is to determine the matrix $\mathbf{M}$ from four

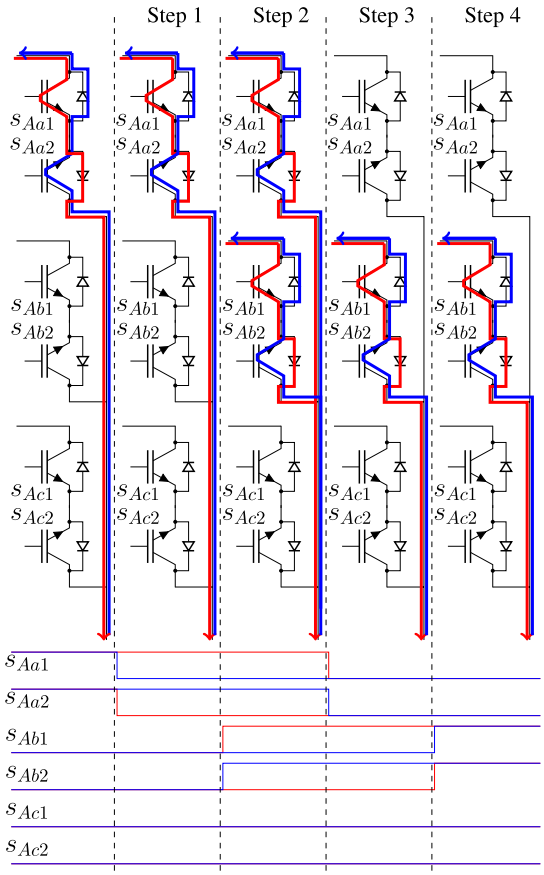


**FIGURE 4.** Four-Steps commutation technique based on current flow direction.

modulation parameters: $q_d$, $q_q$, $\theta_i$, and $\theta_o$. The signals in the reference frame $abc$ (*e.g.*, $V_{abc} = [v_a\ v_b\ v_c]^\intercal$) are transferred to the reference frame $\alpha\beta 0$ (*e.g.*, $V_{\alpha\beta 0} = [v_\alpha\ v_\beta\ v_0]^\intercal$) by using the Clarke transformation (4).

$$V_{\alpha\beta 0} = K\ V_{ABC},$$
$$K = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix}. \tag{4}$$

The $\alpha\beta 0$ signals are represented in the complex plane as an space vector composed of $\alpha$ and $\beta$ as the real and imaginary components. Hence, any signal in the $abc$ reference frame is represented in the complex space as $z = \alpha + i\beta = re^{j\theta}$, where $r = \sqrt{\alpha^2 + \beta^2}$ and $\theta = \arctan\left(\frac{\beta}{\alpha}\right)$. Since the MC works under a three wired system, there is no zero-sequence current. Therefore, a zero-sequence component of the voltage can be added to the output for increasing the MC operating range.

In this way, the output signals are generated by using the modulation parameters as described below. The input voltage $V_{\alpha i} + jV_{\beta i} = V_i e^{j\phi_i}$ and output current $I_{\alpha o} + jI_{\beta o} = I_o e^{j\gamma_o}$ are the input elements for the SVD-M technique.

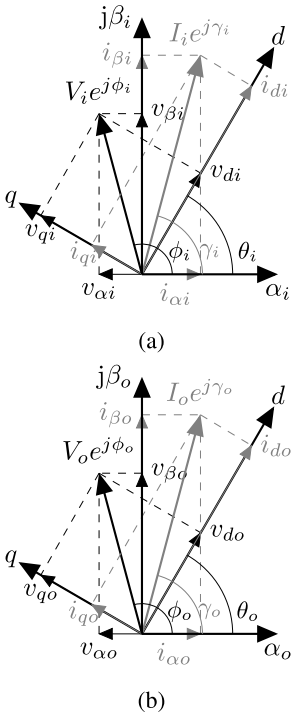


**FIGURE 5.** SVD-M space vector signals: (a) inputs, (b) outputs.

These signals are projected over the rotation reference frame $dq$ given by phase angles $\theta_i$ and $\theta_o$, which results in the transformed input voltage $[v_{di}\ v_{qi}]^\intercal$ and output current $[i_{do}\ i_{qo}]^\intercal$, respectively. The $dq$ output voltages $[v_{do}\ v_{qo}]^\intercal$ and the $dq$ input currents $[i_{di}\ i_{qi}]^\intercal$ are calculated in terms of the SVD-M parameters $q_d$ and $q_q$ as stated in (5). Thus, to satisfy (2), the conditions imposed by relations (6) must be fulfilled.

$$\begin{aligned} v_{do} &= q_d v_{di}, \quad i_{di} = q_d v_{do}, \\ v_{qo} &= q_q v_{qi}, \quad i_{qi} = q_q v_{qo}. \end{aligned} \tag{5}$$

$$\begin{aligned} |q_d| + |q_q| &\leq 1, \\ \max\{|q_d|, |q_q|\} &\leq \frac{\sqrt{3}}{2}. \end{aligned} \tag{6}$$

The input and output signals involved in the SVD-M technique are shown in Fig. 5. Once the variables $\theta_i$, $\theta_o$, $q_d$, and $q_d$ have been determined, the matrix $\mathbf{M}$ is calculated by the system of equations (7).

$$\begin{aligned} M = {} & \frac{q_d - q_q}{3} \begin{bmatrix} \cos(\theta_p) & \cos(\theta_{p-}) & \cos(\theta_{p+}) \\ \cos(\theta_{p-}) & \cos(\theta_{p+}) & \cos(\theta_p) \\ \cos(\theta_{p+}) & \cos(\theta_p) & \cos(\theta_{p-}) \end{bmatrix} \\ & + \frac{q_d + q_q}{3} \begin{bmatrix} \cos(\theta_m) & \cos(\theta_{m+}) & \cos(\theta_{m-}) \\ \cos(\theta_{m-}) & \cos(\theta_m) & \cos(\theta_{m+}) \\ \cos(\theta_{m+}) & \cos(\theta_{m-}) & \cos(\theta_m) \end{bmatrix} \\ & + \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} + \begin{bmatrix} c_1 & c_2 & c_3 \\ c_1 & c_2 & c_3 \\ c_1 & c_2 & c_3 \end{bmatrix}, \end{aligned} \tag{7}$$

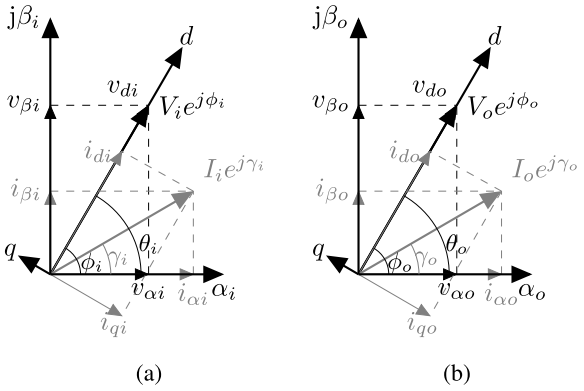


**FIGURE 6.** Implemented SVD-M, (a) input vectors, (b) output vectors.

where the phase angles $\theta$ and coefficients $C_k$ are defined by,

$$\theta_p = \theta_L + \theta_S, \quad \theta_{p+} = \theta_L + \theta_S - \frac{2\pi}{3}, \ \theta_{p-} = \theta_L + \theta_S,$$

$$\theta_m = \theta_L - \theta_S, \quad \theta_{m+} = \theta_L - \theta_S - \frac{2\pi}{3}, \ \theta_{m-} = \theta_L - \theta_S,$$

$$c_k = -min_i\{M_1(i,k)\} + \sum_j \min_i\{M_1(i,j)\} \times \frac{1 - \max_i\{M_1(i,k)\} + \min_i\{M_1(i,k)\}}{3 - \sum_j \max_i\{M_1(i,j)\} + \sum_j \min_i\{M_1(i,j)\}}.$$

The main advantage of the SVD-M relies on the intrinsic properties of the parameters, which have a clear physical interpretation, and consequently provides a fashion to the straightforward assignation of values. For this work, the phase angle $\theta_i$ is assigned with the same value obtained from the input voltage $\phi_i$. In this way, the component $v_{qi}$ is equal to zero, producing an output lacking the component $v_{qo}$. The output phase angle $\theta_o$ can be assigned as $\theta_i$ to obtain the same input operating frequency at the output voltages. Additionally, $\theta_o$ can be assigned with a synthetic phase for any desired output frequency. Furthermore, the input-output voltage ratio is determined by the parameter $q_d$, *i.e.*, $q_d = \frac{V_o}{V_i}$, and the parameter $q_q$ is utilized to reproduce the current component $i_{qi}$ from $i_{qo}$. From this perspective, the input power factor can be modified by controlling the $q_q$ parameter. Fig. 6 shows all assignations just described.

## IV. MC CONTROLLER IMPLEMENTATION IN AN MCU

The implementation of the MC control algorithms on the MCU represents a complicated task due to the intricate computations involved in evaluating the SVD-M technique (Clarke transformation, trigonometric function evaluation, *etc.*), the necessity of executing parallel algorithms (four-step commutation), and the rapid capture of external analog and digital signal measurements. In this case, the Delfino TMS320F28379D board which is based on the 32-bit C28x processor plus a floating-point unit (C28x+FPU), was considered. Additionally, the processor has a Trigonometric Math Unit (TMU) that enables fast execution of algorithms using math functions [40], [41]. This device also has the peripherals required for implementing

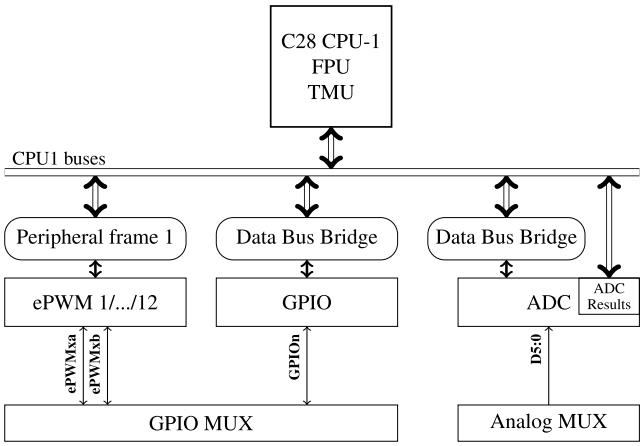


**FIGURE 7.** Functional block diagram TMS320F28379d.

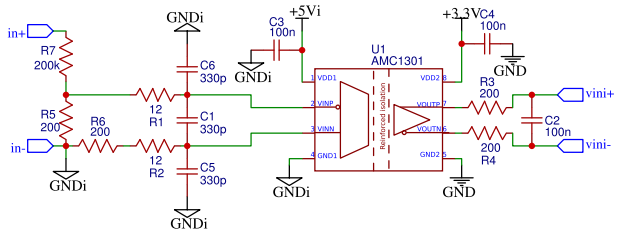


**FIGURE 8.** Voltage sensor circuit.

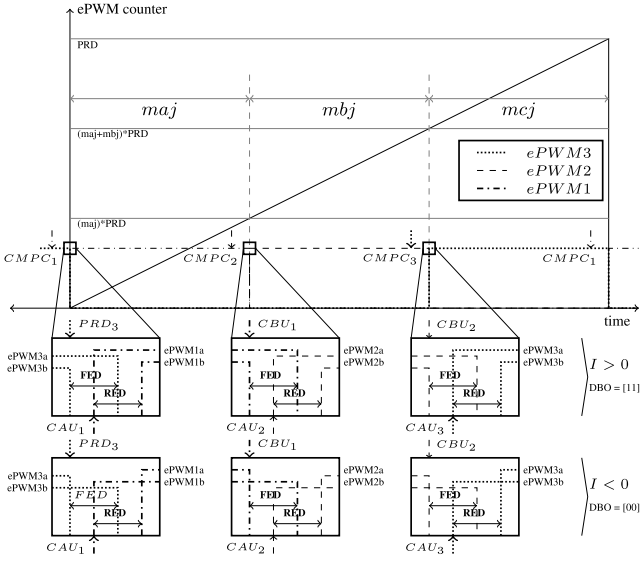


**FIGURE 9.** ePWM four-steps commutation technique.

control algorithms [42]. The functional block diagram of the principal components used in this proposal is presented in Fig. 7, where the building blocks include the core, peripherals, and busses. Actually, by the accurate configuration of these peripherals, the control of the MC can be entirely carried out, allowing the MCU to be configured to run at 200 [MHz], the maximum CPU speed. As explained before, the MC complete control is driven by two algorithms, the SVD-M technique and the Four-Step current commutation method, whose implementation are described in the next subsections.

### A. SVD-M TECHNIQUE IMPLEMENTATION

The SVD-M technique requires the evaluation of complex math functions to calculate the fundamental parameters for the modulation, in addition to the acquisition of the input voltage signals by means of the analog-to-digital converter (ADC) peripheral. The initialization of the ADC is implemented utilizing the differential signal conversion mode, which is necessary for the selected voltage sensor. Likewise, the ADC conversion is governed by an interruption activated at a rate of 10 [kHz] and synchronized with the ePWMs modules used in the four-steps modulation technique. Moreover, a sampling window of 320 [ns] was considered for the ADC. Based on the differential conversion mode, there were used two single channels per each sensor, obtaining a 16-bits resolution in the final digital conversion. Therefore, only 6 ADC channels from the 16 available in the device were utilized for the MC control.

Once the initialization process is completed, the first step in the implementation of the SVD-M technique consists in the measurement of the input voltages through the ADC, which is afforded by the voltage sensor circuit shown in Fig. 8. Then, these input voltages $v_{abc}$ must be transferred to the $\alpha\beta$ reference frame through the Clarke transformation to proceed with the phase angle $\phi_i$ evaluation, which is obtained by the trigonometric function atan2$(x, y)$ for the four quadrants. At this point, the variable $\phi_i$ is known and assigned to the value of variable $\theta_i$. $\theta_o$ must be set to $\phi_i$ if it is desired that the output voltages have the same frequency as the input voltages. Otherwise, $\theta_o$ is assigned with a saw-tooth signal having a phase angle according to the desired output frequency. The parameters $q_d$ and $q_q$ are freely selected, considering only the restrictions imposed by (6).

### B. FOUR-STEP CURRENT COMMUTATION

The implementation of the four-step current commutation technique is based on the enhanced pulse width modulation peripherals (ePWM), as detailed in [37]. The ePWM peripherals are set by estimating the matrix **M** and the output current sign. These peripherals are initialized to generate the signals shown in Fig. 9, which correspond to commutation of an MC arm. In this case, only 9 ePWM peripherals were utilized from the 12 available in the device.

After initialization, the values of the ePWM comparator registers (CMPA, CMPB, and CMPC) are updated at a rate of 10 [kHz], and specifically at the moment when the counter reaches the value of the PRD register, taking into account the value of the elements of matrix **M**. The output current-flow sign was measured by the sensor circuit shown in Fig. 10 and acquired by a digital input in the General-Purpose Input-Output peripheral (GPIO). This measurement is performed just before the commutation takes place through the activation of an interruption signal, which is triggered when the counter reaches the value loaded in the CMPC register.

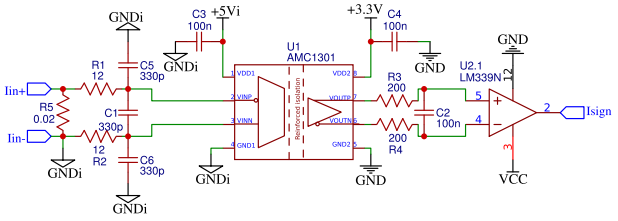


**FIGURE 10.** Current sensor circuit.

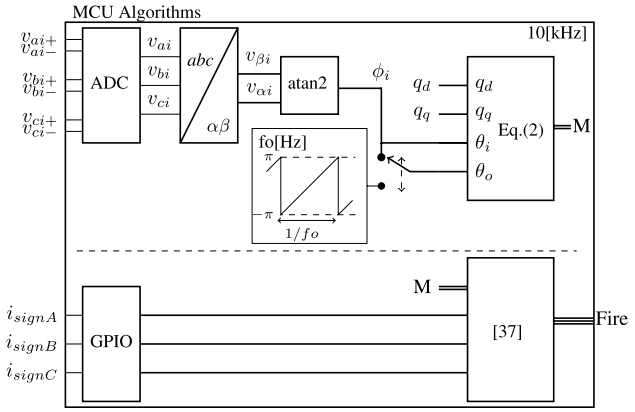


**FIGURE 11.** Matrix Converter Unit (MCU) control.

The GPIO peripheral was configured to read the digital input under a sampling window to generate the respective value of the current-flow sign. In this way, a quality measurement is obtained even under noisy environments. The precious process is implemented using 3 GPIO ports from the 169 ports available in the device. Subsequently, the value of the register DBCTL[OUTSWAP] (DBO) is updated supported by this measurement.

The algorithms described above run sequentially with a period of time equal to $T_{sw} = 0.1[ms]$, with the exception of the input current signal measurement, which depends on the value loaded in the CMPC register. The ePWM peripheral works in continuous operation mode independently of the central processor, and because of this, the peripheral is initialized and configured so that its operation can be modified synchronously and asynchronously while it is running. These conditions are the fundamentals for the proposal of this work, since the synchronous operation ($T_{sw}$) is required for modulation evaluation and update of the comparison registers, while asynchronous operation ($t_{ij}$) is required for the commutation technique. The proper configuration of execution times for these operations represents the main difficulty for the implementation of these algorithms in the proposed MCU. Fig. 11 summarizes the fundamental control algorithms used for the MC control and implemented in the MCU, whilst, Fig. 12 shows the flowchart of the algorithms described previously and coded in the MCU.

## V. SIMULATION AND EXPERIMENTAL RESULTS

A set of simulations and experimental tests were carried out to validate the effectiveness of the proposed MC

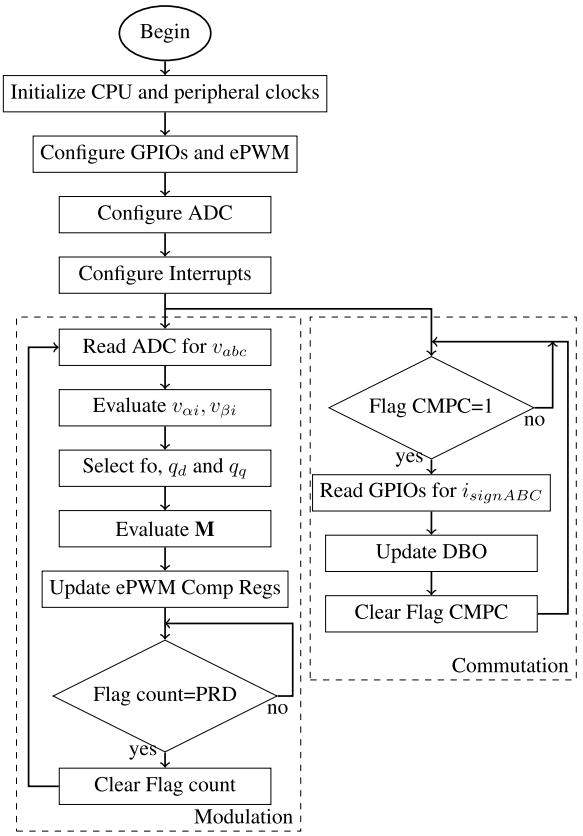


**FIGURE 12.** Matrix Converter MCU flowchart.

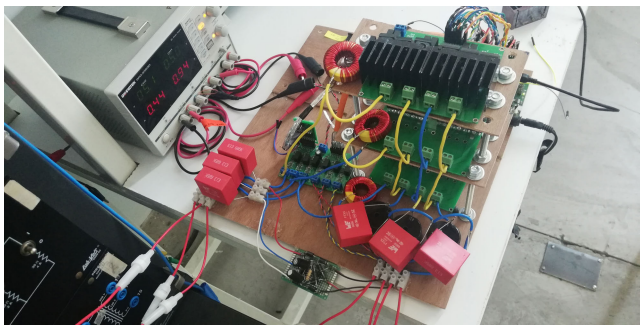

**FIGURE 13.** Matrix converter prototype.

implementation corresponding to the topology shown in Fig. 1. The simulations were performed using Matlab Simulink/SimPowerSystem tools, considering ideal switches to conform the BDS. The experimental tests were performed with the MC prototype shown in Fig. 13. Complementarily, the whole experimental system is shown in Fig. 14. In the design, the TMS320F28379D board was used to develop the MCU module. The MC prototype was assembled using HGT1S1260A4DS IGBTs. The gate driver circuit designed for these devices is fully described by the scheme shown in Fig. 15. Regarding the input and output filters design, the following components were utilized, $L_i = 1.0$ [mH], $C_i = 6.8$ [$\mu$F], $L_o = 0.56$ [mH], and $C_o = 6.8$ [$\mu$F]. Additionally, an RL load was implemented using the following components: $R_L = 13$ [$\Omega$] and $L_l = 25$ [mH].

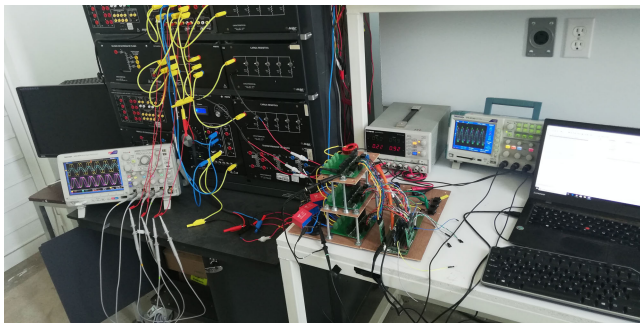

**FIGURE 14.** Matrix converter test system.

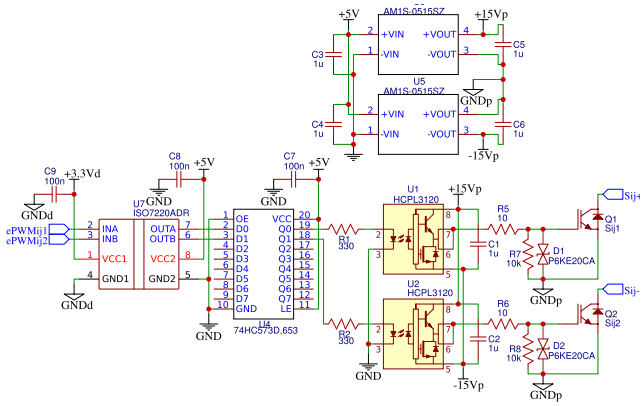


**FIGURE 15.** Gate driver circuit.

For the first test, the system is started considering the output frequency at the same value as the input frequency, and the parameters $q_d$ and $q_q$ are set to 0.5 and 0.0, respectively. The input current $i_{ai}$, input voltage $v_{ai}$, and the unfiltered output voltage $v_{AB}$ experimental signals are registered and shown in Fig. 16a. The same signals are presented in Fig. 16b for the numerical simulation test. It is worth noting the great similarity exhibited by the two sets of signals, which allows verifying the proper functioning of the implemented prototype including the control algorithms. As a second test, the same operating conditions of the previous test are considered, except for the value of parameter $q_q$, which was modified. In this case, the input current $i_{ai}$, input voltage $v_{ai}$, output load voltage $v_{ALN}$, and load current $i_{Al}$, experimental and simulated signals are registered. Fig. 17 shows the evolution in the response of the system while the parameter $q_q$ changes from 0.0 to 0.4. In the behavior of the input current, a delay can be observed at the time when a change in the value of the parameter $q_q$ occurs, which means that the input power factor of the system is improved. Alike, the response signals when $q_q$ changes from $-0.4$ to 0.0 are presented in Fig. 18. In this case, it was also appreciated a delay in the input current, similarly to the previous case, but here there is a clearer decrease in the magnitude of the current. It is relevant to mention that the parameter $q_q$ adds a component to the input current $i_{di}$, thus modifying the phase angle and magnitude of this signal $I_i e^{j\gamma_i}$. Likewise, Fig. 19 presents the results

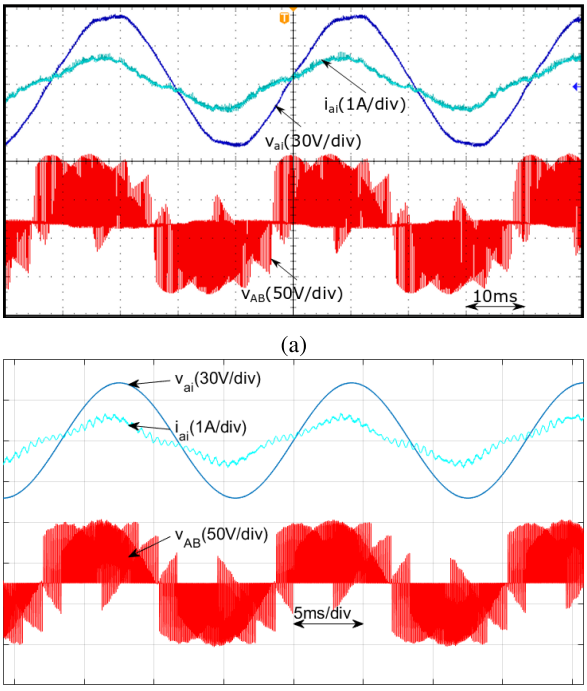


**FIGURE 16.** Unfiltered output voltage, (a) experimental results, (b) simulated results.

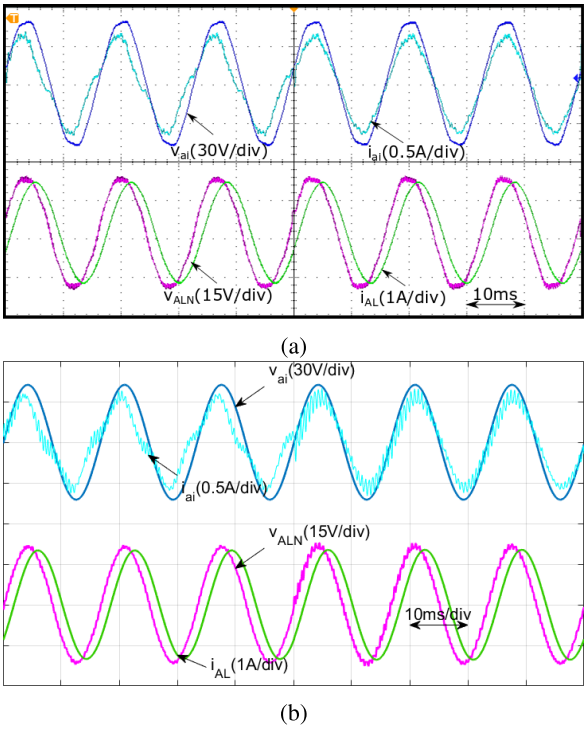


**FIGURE 17.** Voltages and currents evolution as parameter $q_q$ changes from 0.0 to 0.4, (a) Experimental results, (b) Simulation results.

associated with the transition of parameter $q_q$ from 0.4 to -0.4. Unlike the previous cases, this shows a lead in the input current; consequently, the input power factor becomes more capacitive. In general, experimental and simulated signals

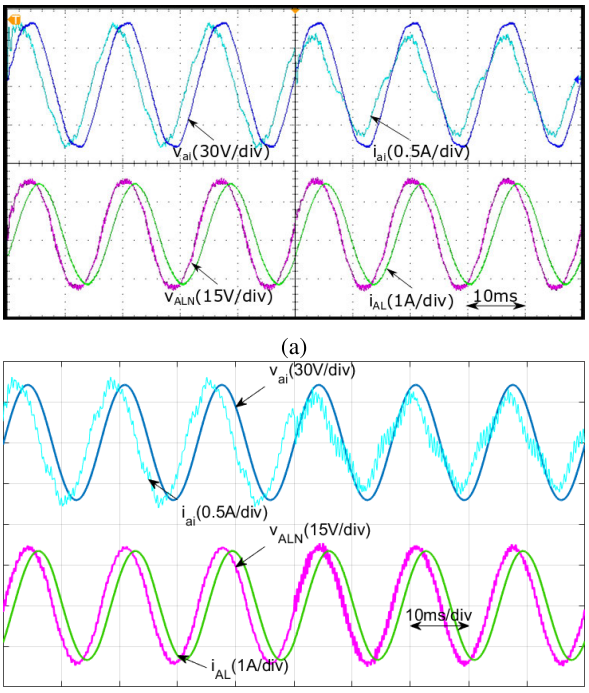


**FIGURE 18.** Response signals when parameter $q_q$ varies from −0.4 to 0.0, (a) experimental results, (b) simulation results.

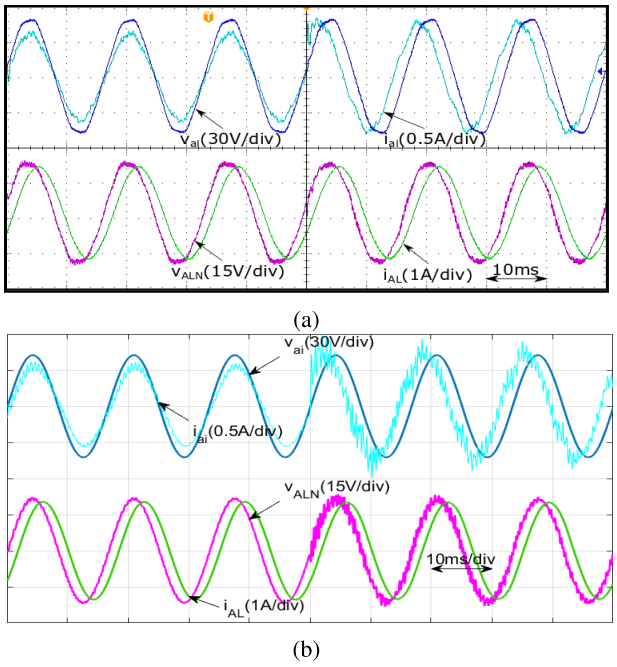


**FIGURE 19.** Voltages and currents evolution as parameter $q_q$ changes from 0.4 to 0.-4, (a) Experimental results, (b) Simulation results.

presented in Figs. 17, 18 and 19 for the different case studies, exhibited great similarity even when the experimental signals contained a certain level of distortion associated with the operation of each of the components utilized for power supply, measurement, commutation, processing, etc., and ideal components were considered for the numerical simulations.

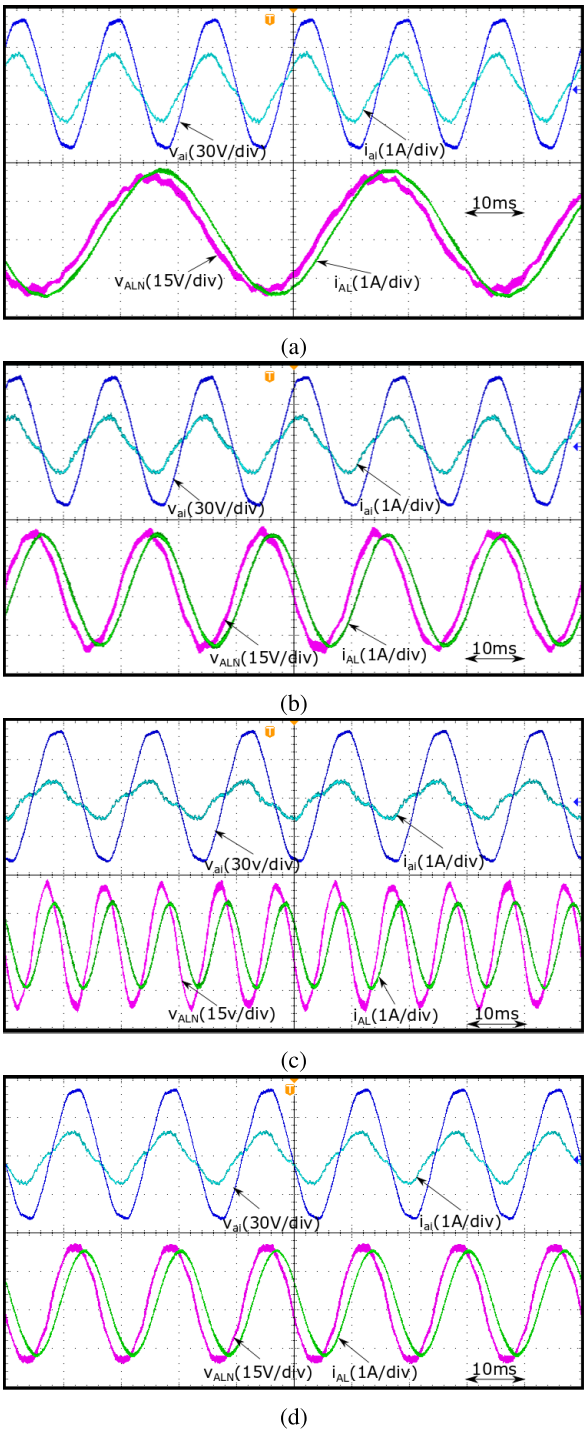


**FIGURE 20.** voltages and currents for different output frequencies, (a) 25 [Hz], (b) 50 [Hz], (c) 100 [Hz], (b) 60 [Hz].

Finally, experimental tests are carried out where synthetic frequencies are considered for the output voltage. The selected values for the output frequency were 25 [Hz], 50 [Hz], and 100 [Hz]. Output voltages and currents for each frequency are displayed in Figs. 20a, 20b, and 20c, respectively. In all these cases, the input signals with a frequency of 60Hz were considered, Fig. 20d. It was observed that as the output frequency varies, the magnitude of the

input current also changes, this is because the magnitude of the RL load is frequency-dependent. Additionally, it is clear that the output voltage is more distorted when the output frequency is different from the frequency of the input signals. In order to improve the quality of the signals generated by the MC, compensation actions must be included in the control algorithms.

## VI. CONCLUSION

A Matrix Converter prototype based on the SVD modulation technique and the four-step current commutation strategy was implemented utilizing an MCU as unique controlling device. The hardware implementation corresponding to the MC prototype was described in detail to facilitate the replication of the results obtained. An easy and comprehensive modulation technique for the MC was presented and discussed, along with the commutation strategy considered. The synchronization between the experimental implementation of the algorithm corresponding to the SVD-M strategy and the algorithm of the four-steps current commutation technique can be pointed out as one of the main contributions of the paper, mainly due to the efficiency in the utilization of hardware resources and the quality of the signals obtained. Additionally, many useful recommendations for the experimental implementation of an MC prototype were included in the paper, with the intention that it can be replicated in a simple way and with low-cost devices. Finally, the proposed implementation was validated through the results obtained from the execution of exhaustive simulations and experimental tests.

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