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A Multi-Layer Sequential Model Predictive Control of Three-Phase Two-Leg Seven-Level T-Type Nested Neutral Point Clamped Converter Without Weighting Factors

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ABSTRACT In this paper, a triple-layer sequential model predictive control (SMPC) approach without weighting factors is proposed for a three-phase two-leg 7-level T-type nested neutral point clamped (T-NNPC) converter. The main objectives of this paper are to eliminate the selection of weighting factors and enhance the reliability of system in the control process. In the proposed design, three cost functions are formulated in a cascaded way to avoid the weighting factors tuning while not compromising the computational complexity. Furthermore, the three-phase two-leg 7-level T-NNPC converter is investigated to improve the fault-tolerance ability in case of a faulty leg condition. Finally, the effectiveness of the control methodology for the three-phase two-leg 7-level T-NNPC converter is validated by comparative simulation studies.

INDEX TERMS T-type nested neutral point clamped (NNPC) converter, fault tolerant operation, weighting factor elimination, low switching frequency.

I. INTRODUCTION

Multilevel voltage source converters (VSCs) are attractive and widely accepted for high-power medium-voltage applications, such as transmission systems, static synchronous compensator and wind turbine applications. Meanwhile, new power converter topologies and latest achievements in terms of control have expanded the application of the multilevel converters to renewable energy conversion, machine drives, among others. Compared with conventional two-level converters, the multilevel converters have a better harmonic performance of the output waveforms, higher operating voltages, lower switching loss, and reduced size of output filter elements and interface transformers [1]–[4].

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Due to the prominent features, a growing body of multilevel topologies have been proposed and developed over the past decades. Typically, the flying capacitor (FC) converter, neutral-point-clamped (NPC) converter, and the cascaded H-bridge (CHB) converter are regarded as the classical multilevel converters and successfully commercialized in manufacturing. However, significant drawbacks of these classical topologies limit their applications for high power density and voltage levels. To be specific, the number of FCs increases substantially for FC topology operating at a higher number of voltage levels, which decreases the reliability of the system. The using of NPC converter for higher power density system requires a large number of clamping diodes. Besides, the requirement of balancing the dc-link capacitor voltages needs an additional control. For the CHB converter, several isolated dc sources generated by the bulky phase-shifting

TABLE 1. Number of components in different 7-level topologies.

	7L-NPC [17]	7L-FC [18]	7L-ANPC [19]	Hybrid 7L-ANPC I [19]	Hybrid 7L-ANPC II [20]	7L T-NNPC
Number of switches	54	36	30	42	42	**24**
Freewheeling diodes	36	36	30	42	42	**24**
Clamping diodes	30	-	-	-	-	**-**
Flying capacitors	18	21	12	21	15	**12**

transformer are mandatory, which increases the cost and volume of the system [5]–[8].

To mitigate aforementioned issues, a variety of advanced multilevel converters have been studied in the literature [9]–[33]. Among them, modular multilevel converter (MMC), active neutral-point-clamped (ANPC) converter, and nested neutral point-clamped (NNPC) multilevel converter gain increasing attention from both academia and industry. MMC is a modular topology and exhibits better scalability, flexible redundant operations and strong fault-tolerance compared with other power converter topologies [9]–[11]. These prominent features of MMC make it especially well suitable for high-voltage direct current (HVdc) transmissions. The ANPC and NNPC converter overcome the inherent drawbacks of conventional multilevel topologies. The balanced dc-link capacitor voltages and identical distribution of power losses can be achieved in the ANPC and NNPC converter, while the bulky and expensive transformer is not needed [12]–[14]. Despite the MMC, ANPC, and NNPC converters have less proportion of clamping diodes and FCs, the number of switching devices still remains high.

Among the modified multilevel topologies, a newly developed 7-level T-type NNPC (T-NNPC) converter, which is first introduced in the literature [15], gains much attention. The single-phase diagram of this topology is shown in Fig. 1. The 7-level T-NNPC converter is developed from a six-level converter in [16]. The prominent feature of this topology is a less proportion of components in comparison to other existing 7-level converters, as illustrated in Table 1. As depicted in Fig. 1, each phase of the 7-level T-NNPC converter consists of eight switching devices and four FCs. Compared with the classical NPC converter [17], FC converter [18], and advanced hybrid 7-level topologies [19], [20], the 7-level T-NNPC converter has a significant reduction in the number of power devices and FCs, which enables a further volume saving and reliability improving. Besides, the isolated dc sources are not needed in this topology as compared with the CHB converter. Due to the aforementioned advantages and the ability to operate over a wide range of voltages, the 7-level T-NNPC converter emerges as a low-cost and high-performance solution for the medium-voltage applications.

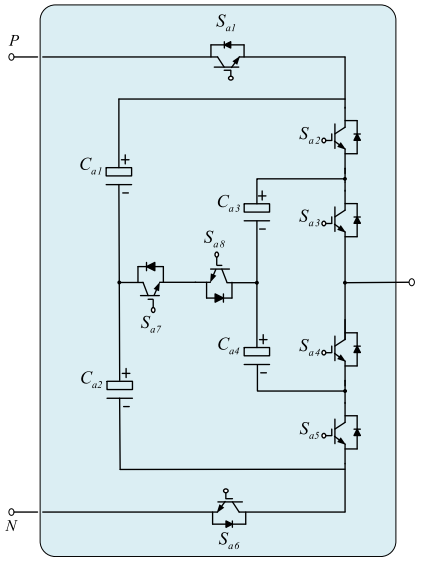

FIGURE 1. Single-phase diagram of 7-level T-NNPC converter [15].

The operation principle of this topology under normal operation condition is well discussed in [15]. However, due to the inevitably damage in switching devices, the investigation of fault-tolerant topology and corresponding control algorithm for multilevel converters is of great significance. In this sense, the three-phase two-leg converter can be regarded as a post-fault reconfigured topology for the traditional three-phase three-leg converter in case of a faulty leg condition. With attempt to ensure continuous operation and mitigate performance degradation of the multilevel converter under faulty leg conditions, substantial modified control schemes have been proposed, such as pulse width modulation (PWM) technology and space vector modulation (SVM) scheme. A fault-tolerant PWM control strategy is proposed in [22] for four-switch three-phase converter. In [23], a new active fault-tolerant SVPWM control strategy for a hybrid seven-level converter is proposed for dealing with single phase short- and open-circuit faults, where the reliability and robustness of the converter is improved by introducing an offset vector. However, all the control schemes mentioned above are based on linear control method, where the control performance is

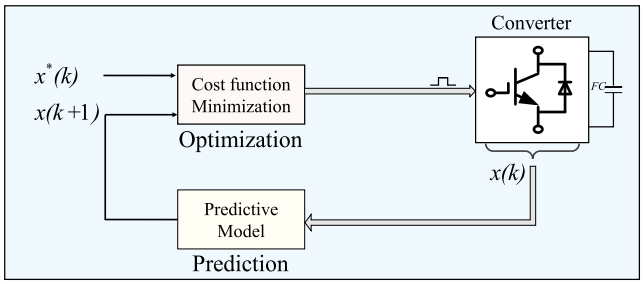

FIGURE 2. Implementation steps of FCS-MPC strategy for power converters.

greatly depended on the proper tuning of control parameters as well as the type of modulation scheme [24].

Recently, thanks to the development of fast digital processors, some intelligent algorithms can be implemented in real-time system. Among them, finite control set model predictive control (FCS-MPC), as a nonlinear control strategy, emerges as another powerful solution for power converters. The FCS-MPC approach takes advantages of discrete nature and limited switching states of power converters, and thus, the tuning of PI regulators and designing of modulators can be eliminated. Meanwhile, the FCS-MPC method has the merits of flexibility to satisfy system constraints and nonlinearities, ability to handle multiple control objectives through a cost function while keeping a fast dynamic response [25]–[27].

The basic operation principle of FCS-MPC approach is illustrated in Fig. 2. Two main steps are involved in the control process: i) prediction; ii) optimization. The future behaviors of control variables are first predicted through a discrete-time domain mathematical model in the prediction process. Then, to obtain a desired control performance, a cost function is established in the optimization process by comparing the predictive and reference value of control variables. The control action which minimizes the predefined cost function is defined as optimum and applied to the converter at next sampling instant. Due to the intuitive concept and excellent control performance, the FCS-MPC scheme is widely accepted in the control of multilevel converters, such as FC converter, NPC converter, ANPC converter, MMC, and NNPC converter [28]–[33].

Even though the FCS-MPC scheme is easy to understand and seems promising, the large computational burden, selection of optimal weighting factors (WFs), and high switching frequency (SF) are main challenges, which hinder the application of FCS-MPC scheme [30]. Besides, the faulty leg operation condition have been proven to be one of the greatest challenges for multilevel converters, which increases the control complexity of the FCS-MPC approach [31].

To mitigate these issues, several modified FCS-MPC schemes have been presented for relieving the computational complexity and determining the desired WFs in an efficient manner. The fast MPC method deployed in [9] decreases the finite control-set from all available switching states, which results in a significant reduction in computational burden. However, the appropriate values of several involved WFs are difficult to select. Different from [9], the WFs can be eliminated in [10], [11] by using a cascaded control structure for MMC. Due to the distinct operation principles, it cannot be implemented in the 7-level T-NNPC converter. Besides, these methods mentioned above are focused on the control in normal condition without fault-tolerant operation. Very recently, a sequential model predictive control (SMPC) is proposed in the control of electrical drives in [34], [35]. Two cost functions for separately minimizing the torque and flux tracking error are evaluated in a cascaded way, which results in the elimination of WFs. However, there is no previous attempt to use SMPC to control the multilevel converters.

This paper proposed a multi-layer sequential model predictive direct power control (S-MPDPC) for a three-phase two-leg 7-level T-NNPC converter. The main contributions of this paper are summarized as follows:

i) A novel triple-layer S-MPDPC approach is proposed in this paper for three-phase two-leg 7-level T-NNPC converter. Multiple control objectives including grid-side powers tracking, FCs voltage balancing, dc-link capacitor voltages regulation, and SF reduction are well fulfilled without including WFs. The proposed S-MPDPC algorithm changes the structure of the cost function rather than thinking of different ways of obtaining optimal WFs. Dealing with the same challenge, the proposed design can provide a comparable control performance with less tuning efforts as compared with conventional WF-based FCS-MPC scheme.

ii) A fault-tolerant three-phase two-leg topology is investigated for post-fault operation of the 7-level T-NNPC converter under faulty leg conditions. The detailed mathematic model of the investigated topology is established in this paper for dc-link capacitor voltages balancing and control performance improving.

The reminder of this paper is organized as follows. The operation principle and mathematic model of the three-phase two-leg 7-level T-NNPC converter are analyzed in Section II. The multi-layer S-MPDPC controller design is briefly introduced in Section III. The simulation results in comparison to the traditional three-phase three-leg topology and conventional WF-based FCS-MPC method are investigated in Section IV with aim to verify the performance of the proposed method. Section V concludes this paper.

II. OPERATION PRINCIPLE AND MATHEMATIC MODEL OF THE THREE-PHASE TWO-LEG 7-LEVEL T-NNPC CONVERTER

A. OPERATION PRINCIPLE ANALYSIS

The configuration of the three-phase two-leg 7-level T-NNPC converter is shown in Fig. 3. As seen in Fig. 3, only two phase legs are connected to the ac grid-side, while the third phase is tapped from the mid-point of the dc-link (o). The dc-side consists two capacitors (C_{d1} and C_{d2}) with a rating of $V_{dc}/2$ and a passive load. Each leg of the converter is realized by

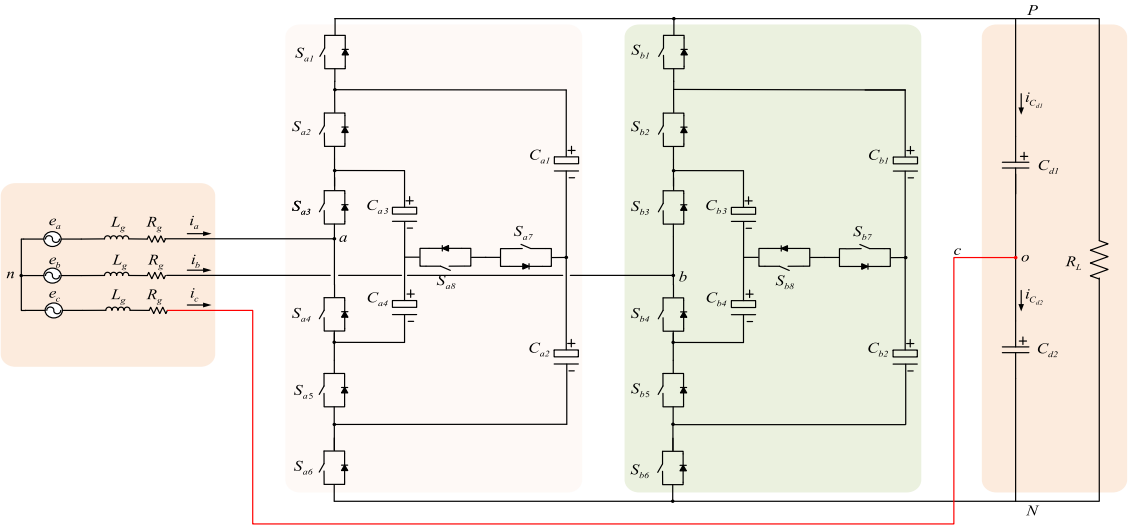

FIGURE 3. Power circuit of the three-phase two-leg 7-level T-NNPC converter.

TABLE 2. The switching states and corresponding vectors of the 7-level T-NNPC converter [15].

Output level	Voltage vector	Switching states								Switching vector
N_j	V_{jN}	S_{j1}	S_{j2}	S_{j3}	S_{j4}	S_{j5}	S_{j6}	S_{j7}	S_{j8}	
6	V_{dc}	1	1	1	0	0	0	0	0	6
5	$5V_{dc}/6$	1	0	1	0	0	0	1	1	5
4	$2V_{dc}/3$	1	1	0	1	0	0	0	0	4C
		1	0	1	0	1	0	0	0	4B
		0	1	1	0	0	1	0	0	4A
3	$V_{dc}/2$	1	0	0	1	0	0	1	1	3B
		0	0	1	0	0	1	1	1	3A
2	$V_{dc}/3$	1	0	0	1	1	0	0	0	2C
		0	1	0	1	0	1	0	0	2B
		0	0	1	0	1	1	0	0	2A
1	$V_{dc}/6$	0	0	0	1	0	1	1	1	1
0	0	0	0	0	1	1	1	0	0	0

using eight power devices and four FCs. By charging the outer FCs C_{j1}, C_{j2} to one-third of the dc-bus voltage ($V_{dc}/3$), inner FCs C_{j3}, C_{j4} to one-sixth of the dc-bus voltage ($V_{dc}/6$), $j = a, b, c$, seven voltage levels with a step of $V_{dc}/6$ can be achieved in the phase out terminal.

Table 2 shows the relationship of the switching states in the 7-level T-NNPC converter with their corresponding output levels. As shown in Table 2, seven output levels are generated by a combination of 12 switching states. Redundant switching states only appear in the intermediate level 2, 3 and 4. Even though the redundancy produces an identical voltage at the phase output terminal, each of them has a specific effect on the FCs voltage respect to the signal of phase current. Thanks to the unique characteristic of the redundancy in multilevel converters, the FCs voltage can be balanced by selecting proper redundant switching states.

B. MATHEMATICAL MODEL OF THE THREE-PHASE TWO-LEG 7-LEVEL T-NNPC CONVERTER

To obtain the future behaviors of control objectives in FCS-MPC approach, a discrete-time model of control variables including grid-side powers, FCs voltage, and the dc-link capacitor voltages is introduced in this subsection.

The mathematical model is derived from the system parameters, measured variables, and available switching states.

1) MODELING OF GRID-SIDE POWERS

According to the Kirchhoff's voltage law (KVL) in Fig. 3, the dynamic behavior of phase-j in stationary abc frame are given by

$$\begin{aligned} V_{an} &= e_a - Ri_a - L\frac{di_a}{dt} \\ V_{bn} &= e_b - Ri_b - L\frac{di_b}{dt} \\ V_{cn} &= e_c - Ri_c - L\frac{di_c}{dt} \end{aligned} \tag{1}$$

where V_{an}, V_{bn}, and V_{cn} are the phase-to-neutral voltages. e_a, e_b, and e_c are the grid-side voltage of each phase. i_a, i_b, and i_c are the grid-side currents of three phase. R and L are the grid-side resistance and inductance, respectively.

The phase-to-neutral voltages V_{jn} can be expressed in terms of phase-to-midpoint voltage V_{jo} and a common-mode voltage V_{on}, as given by

$$\begin{aligned} V_{an} &= V_{ao} + V_{on} \\ V_{bn} &= V_{bo} + V_{on} \\ V_{cn} &= V_{on}. \end{aligned} \tag{2}$$

Here, due to the phase-c is directly connected to the midpoint of dc-link, thus $V_{co} = 0$. Under the balanced grid-side conditions, the summation of three phase voltage and current equals to zero (i.e. $V_{an} + V_{bn} + V_{cn} = 0$, $i_a + i_b + i_c = 0$). Thus, the common-mode voltage in (2) can be deduced by

$$V_{on} = -\frac{V_{ao} + V_{bo}}{3}. \tag{3}$$

Table 3 shows the switching vectors and their corresponding phase-to-midpoint voltage V_{jo} of the 7-level T-NNPC converter. By employing distinct switching state, different FCs are incorporated into the current path. The detailed relationship between V_{jo} and switching states is summarized in (4).

$$\begin{aligned} V_{jo} = {} & V_{C_{d1}}(S_{j1}) + V_{C_{d2}}(S_{j1} - 1) \\ & + V_{C_{j1}}(S_{j2} - S_{j3} - S_{j4} + S_{j6}) + V_{C_{j2}}(S_{j6} - S_{j5}) \\ & + V_{C_{j3}}(S_{j3} - S_{j2}) + V_{C_{j4}}(S_{j5} - S_{j4}). \end{aligned} \tag{4}$$

Here, $V_{C_{d1}}$ and $V_{C_{d2}}$ are the voltages of two dc-link capacitors, respectively. $V_{C_{jx}}$ is the voltage of FC C_{jx} in phase-j, $x = 1, 2, 3, 4$.

Combining the analysis above, the continuous-time domain dynamic model of grid-side current in $\alpha\beta$ stationary frame can be deduced as

$$\frac{di_g}{dt} = \frac{1}{L}e_g - \frac{R}{L}i_g - \frac{1}{L}V_g \tag{5}$$

TABLE 3. Phase output voltage of different switching vectors.

Switching vector	V_{jo}
6	$V_{C_{d1}}$
5	$V_{C_{d1}} - V_{C_{j1}} + V_{Cj3}$
4C	$V_{C_{d1}} - V_{Cj3} - V_{Cj4}$
4B	$V_{C_{d1}} - V_{Cj1} - V_{Cj2} + V_{Cj3} + V_{Cj4}$
4A	$-V_{C_{d2}} + V_{C_{j1}} + V_{Cj2}$
3B	$V_{C_{d1}} - V_{Cj1} - V_{Cj4}$
3A	$-V_{C_{d2}} + V_{Cj2} + V_{Cj3}$
2C	$V_{C_{d1}} - V_{Cj1} - V_{Cj2}$
2B	$-V_{C_{d2}} + V_{Cj1} + V_{Cj2} - V_{Cj3} - V_{Cj4}$
2A	$-V_{C_{d2}} + V_{Cj3} + V_{Cj4}$
1	$-V_{C_{d2}} + V_{Cj2} - V_{Cj4}$
0	0

where V_g is the voltage vector in $\alpha\beta$ stationary frame, it's $\alpha-$ and $\beta-$axis component are calculated by

$$\begin{bmatrix} V_{g\alpha} \\ V_{g\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}. \tag{6}$$

For the purpose of implementing the FCS-MPC approach, the continuous-time model needs to be transformed to the discrete-time domain through a Euler approximation approach. It yields

$$\frac{di_j}{dt} = \frac{i_j(k+1) - i_j(k)}{T_s} \tag{7}$$

where, T_s denotes the system sampling time.

The discrete-time model of grid-side current is deduced by substituting (7) into (5), as given by

$$i_g(k+1) = \frac{T_s}{L}(e_g(k) - V_g(k)) + (1 - \frac{RT_s}{L})i_g(k). \tag{8}$$

The dynamic behavior of grid-side active power and reactive power (represented by p and q) can be deduced according to the instantaneous power theory, as shown in (9)

$$\begin{cases} p = 1.5(e_{g\alpha}i_{g\alpha} + e_{g\beta}i_{g\beta}) = 1.5Re(i_g^* e_g) \\ q = 1.5(e_{g\beta}i_{g\alpha} - e_{g\alpha}i_{g\beta}) = 1.5Im(i_g^* e_g). \end{cases} \tag{9}$$

In digital application, the sampling frequency usually is much higher, thereby the grid voltage is assumed to remain constant among contiguous sample instant. Then the predictive values of active power and reactive power in $(k+1)th$ sample instant (represented by $p(k+1)$ and $q(k+1)$) can be

calculated by

$$\begin{cases} p(k+1) = 1.5(e_{g\alpha}(k)i_{g\alpha}(k+1) + e_{g\beta}(k)i_{g\beta}(k+1)) \\ q(k+1) = 1.5(e_{g\beta}(k)i_{g\alpha}(k+1) - e_{g\alpha}(k)i_{g\beta}(k+1)). \end{cases} \tag{10}$$

Equation (10) indicates that the future behavior of active and reactive powers can be predicted by using the measured variables and switching states.

2) MODELING OF FCs VOLTAGE

As analyzed above, the voltages of four FCs in each phase are affected by the applied switching state and the signal of phase current. To proper regulate these FCs voltage, a discrete-time domain model of FCs is established in this subsection.

The dynamic behavior of capacitor voltage in continuous-time domain is given by

$$V_{Cjx}(t) = V_{Cjx}(0) + \frac{1}{C}\int_{0+}^{t} i_{Cjx}(\tau)\, d\tau. \tag{11}$$

Here, $V_{Cjx}(0)$ denotes the initial value of capacitor voltage. C is the capacitance of FCs. i_{Cjx} is the current flowing through capacitor $V_{C_{jx}}$. The capacitor is charged and discharged according to the internal switch state and the direction of phase current. Thus, the one-step prediction of capacitor voltage in discrete-time domain is deduced from (11) as

$$V_{Cjx}(k+1) = V_{Cjx}(k) + \frac{T_s}{C} i_{Cjx}(k) \tag{12}$$

where $V_{Cjx}(k+1)$ and $V_{Cjx}(k)$ denote the predictive and measured capacitor voltage, respectively.

The currents flowing through four FCs in phase-j are determined by

$$\begin{aligned} i_{C_{j1}}(k) &= (S_{j2} - S_{j1})i_j(k) \\ i_{C_{j2}}(k) &= ((S_{j2}||S_{j7}) - S_{j1})i_j(k) \\ i_{C_{j3}}(k) &= (S_{j3} - S_{j2})i_j(k) \\ i_{C_{j4}}(k) &= (S_{j3} - (S_{j2}||S_{j7}))i_j(k). \end{aligned} \tag{13}$$

3) MODELING OF DC-LINK CAPACITOR VOLTAGE

The dc-link of the three-phase two-leg topology is composed of two capacitors C_{d1}, C_{d2} with the capacitance of C_d. Due to the special structure, the balancing of these two capacitors voltage should be considered. Same as the procedure to deduce the discrete-time model for FC voltage, the discrete-time dynamic equations for dc-link capacitor voltage are given by

$$\begin{aligned} V_{C_{d1}}(k+1) &= V_{C_{d1}}(k) + \frac{T_s}{C_d} i_{C_{d1}}(k) \\ V_{C_{d2}}(k+1) &= V_{C_{d2}}(k) + \frac{T_s}{C_d} i_{C_{d2}}(k) \end{aligned} \tag{14}$$

where $V_{C_{di}}(k+1)$, $V_{C_{di}}(k)$ are the predicted and measured values of two dc-link capacitor voltages, respectively, $i = 1, 2$. $i_{C_{d1}}$ and $i_{C_{d2}}$ are the upper and lower capacitor currents, respectively. The positive direction of two capacitor currents are shown in Fig. 1, and their values are given by

$$\begin{aligned} i_{C_{d1}}(k) &= S_{a1}i_a(k) + S_{b1}i_b(k) - (V_{C_{d1}}(k) + V_{C_{d2}}(k))/R_L \\ i_{C_{d2}}(k) &= (S_{a1} - 1)i_a(k) + (S_{b1} - 1)i_b(k) \\ &\quad -(V_{C_{d1}}(k) + V_{C_{d2}}(k))/R_L. \end{aligned} \tag{15}$$

III. MULTI-LAYER S-MPDPC CONTROLLER DESIGN FOR THE THREE-PHASE TWO-LEG 7-LEVEL T-NNPC CONVERTER

A. CONVENTIONAL MPDPC SCHEME FOR THREE-PHASE TWO-LEG CONVERTER

To obtain a desired control performance, the cost functions are established in this section for selecting the optimal switching state. The control diagram of the conventional WF-based MPDPC is illustrated in Fig. 4(a). In the conventional MPDPC approach, multiple control objectives are incorporated into a single cost function in conjunction with corresponding WFs, as given by

$$\begin{aligned} g = {} & \lambda_p \left|p_{ref}(k+1) - p(k+1)\right| + \lambda_q \left|q_{ref}(k+1) - q(k+1)\right| \\ & + \lambda_c \sum_{j=a,b} \sum_{x=1}^{4} \left|V_{C_{jx}}(k+1) - V_C^*\right| \\ & + \lambda_d \sum_{i=1}^{2} \left|V_{C_{di}}(k+1) - V_{dc}^*/2\right|. \end{aligned} \tag{16}$$

Here, λ_p, λ_q, λ_c, λ_d are WFs corresponding to each control variables, V_C^* is the reference value of FCs voltage, $p_{ref}(k+1)$ and $q_{ref}(k+1)$ are the reference active and reactive powers, respectively. In the conventional MPDPC scheme, multiple control objectives are well satisfied by tuning the WFs appropriately. However, due to the different characteristics of each control variable, the variance of specific control variable will also affect the performance of other control objective simultaneously [36]. Since the WFs have a crucial effect on the quality of control objectives, the selection of these parameters has become the important task in the FCS-MPC designing.

B. PROPOSED MULTI-LAYER S-MPDPC APPROACH FOR THREE-PHASE TWO-LEG CONVERTER

To circumvent this issue, a novel control structure is proposed in this paper. The control diagram of the proposed multi-layer S-MPDPC is illustrated in Fig. 4(b). In the modified S-MPDPC approach, apart from the control objectives in (16), the SF reduction is also considered. Multiple control objectives are divided into three separated groups corresponding to the regulation of capacitor voltages, tracking of grid-side powers, and the reduction of SF. Three independent cost functions F_1, F_2, and F_3 are employed in a cascaded structure as shown in Fig. 4(b), such that the WFs are eliminated in the control process. The detailed cost function design is given as follows.

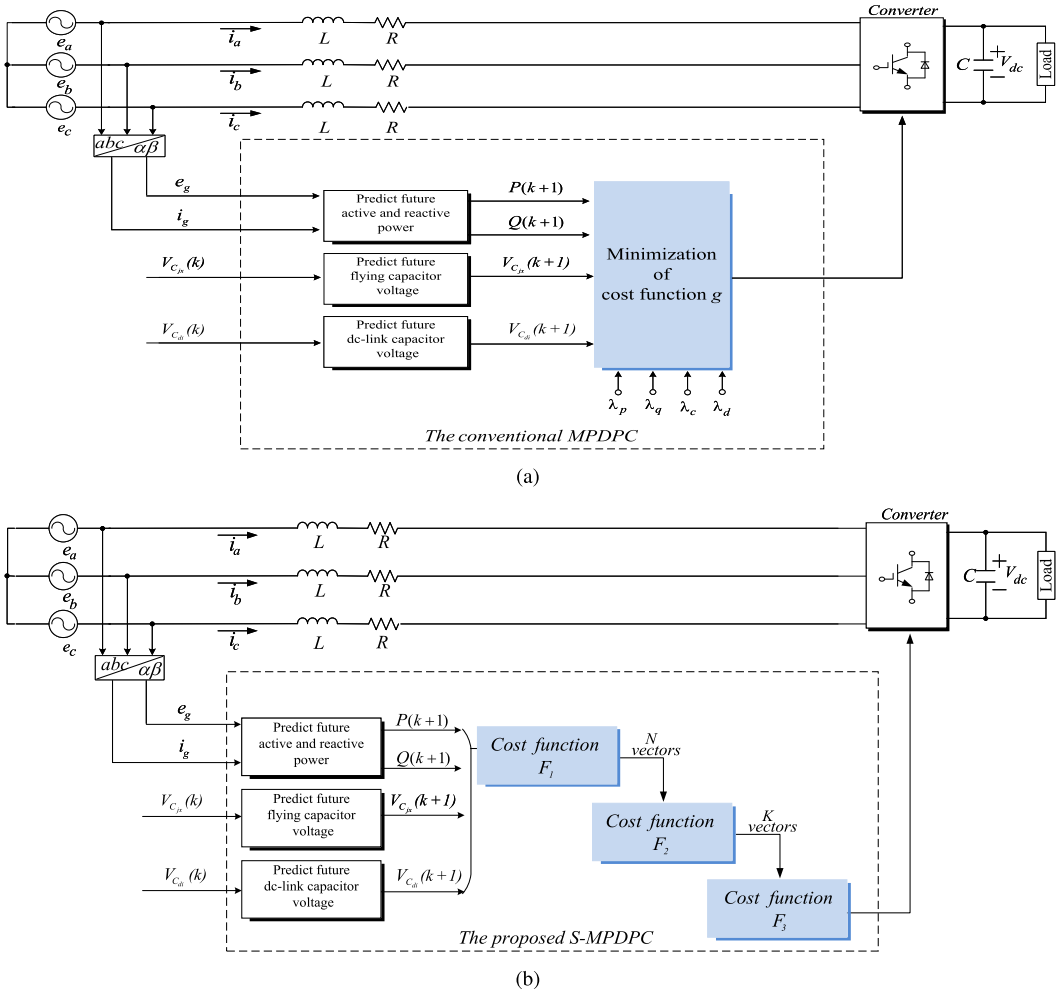

FIGURE 4. Control block diagrams for (a) conventional WF-based MPDPC and (b) proposed multi-layer S-MPDPC.

1) CAPACITOR VOLTAGE BALANCING RELATED COST FUNCTION DESIGN

The balanced capacitor voltage is the basis for proper operation of the multilevel converters. In this design, the FCs voltage balancing and the dc-link capacitor voltages regulation are considered simultaneously. Similar to the cost function in (16), the capacitor voltage related cost function F_1 is given by

$$F_1 = \sum_{j=a,b}\sum_{x=1}^{4}\left|V_{C_{jx}}(k+1)-V_C^*\right|+\sum_{i=1}^{2}\left|V_{C_{di}}(k+1)-\frac{V_{dc}^*}{2}\right|. \tag{17}$$

2) POWERS TRACKING RELATED COST FUNCTION DESIGN

To obtain a desired grid-side powers performance, the powers tracking related cost function F_2 is designed in such a way that the predictive active and reactive powers at the end of this control interval are as close as possible to their reference values. Besides, it is well known that the one-step delay in digital implementation should be considered in the design of predictive strategy. To compensate for this delay and obtain a better control performance, the active and reactive powers are predicted for the future $(k+2)th$ instant in this design.

$$F_2 = \left|p_{ref}(k+1)-p(k+2)\right|+\left|q_{ref}(k+1)-q(k+2)\right|. \tag{18}$$

3) SWITCHING FREQUENCY REDUCTION RELATED COST FUNCTION DESIGN

Since the optimal switching state is determined independently during adjacent control interval in the conventional MPDPC scheme, thus the induced switching frequency is pretty high. To mitigate this issue, an additional cost function is established in this subsection so as to reduce the changes of switching states.

$$F_3 = \left|S_i - S_{old}\right|. \tag{19}$$

where S_i is the switching state of next sample instant and S_{old} represents the applied switching state from previous control period.

As illustrated in Fig. 4(b), in the optimization process, the cost function F_1 is first evaluated by enumerating all the available switching states of the converter. N switching states

that produce smaller values for capacitor voltage related cost function F_1 are pre-selected, and then, delivered to next control step. Afterward, these switching states are further optimized by evaluating the power tracking related cost function F_2, K switching states giving smaller values for F_2 are selected and delivered to next control step. Finally, the optimal switching state which minimizes the cost function F_3 is determined and applied to the converter.

It is worth noting that a larger N or a smaller K means higher priority for the power tracking performance performed in F_2, which leads to a better active/reactive power waveforms and grid-side current quality. At the same time, the performance of dc-bus voltage and FCs voltage is compromised due to the fact that the final select switching state may leads to a high value of cost function F_1. If all the available switching states are selected in F_1 and only one switching state is optimized from F_2, it means that the objective of capacitor voltage balancing and the SF reduction are totally abandoned in the optimization process. Conversely, for an extreme case of only one switching state is selected in F_1, the capacitor voltage regulation has highest priority and the system losses the ability for grid-side powers control. To obtain a comparable dc-bus voltage and balanced FCs voltage, the N is not recommended larger than the half number of total available switching states. Besides, on the grounds that the reduction of SF will affect the quality of grid-side powers and capacitor voltages, K is not recommended larger than 7 in this design.

4) DESIGN STEPS

The designing process of the proposed multi-layer S-MPDPC approach involves various steps. To further indicate how the proposed algorithm works, complete design steps are given as follows:

1) Measure the grid-side voltage and currents e_{abc}, i_{abc}, capacitor voltages $V_{C_{jx}}$, $V_{C_{di}}$ at the *kth* sampling instant;
3) Calculate the voltage vector V_g;
4) Predict the future behaviors of capacitors voltage $V_{C_{jx}}$, $V_{C_{di}}$ based on (12) and (14), respectively;
5) Evaluate all the available 144 (12^2) switching states for capacitor voltage balancing related cost function (17) and pre-select the N desired switching states producing smallest value over the other states;
6) Calculate the predicted values of active and reactive powers at $(k+2)th$;
7) Evaluate pre-selected N switching states for power tracking related cost function (18). K switching states that give smallest values for (18) are selected and delivered;
8) Evaluate K switching states for SF reduction related cost function (19). The desired switching state which gives minimization value for (19) is selected as the final optimal state and applied in the next control period.

In the control process, the total computational cost is no more than $(144+N+K)$ in this design.

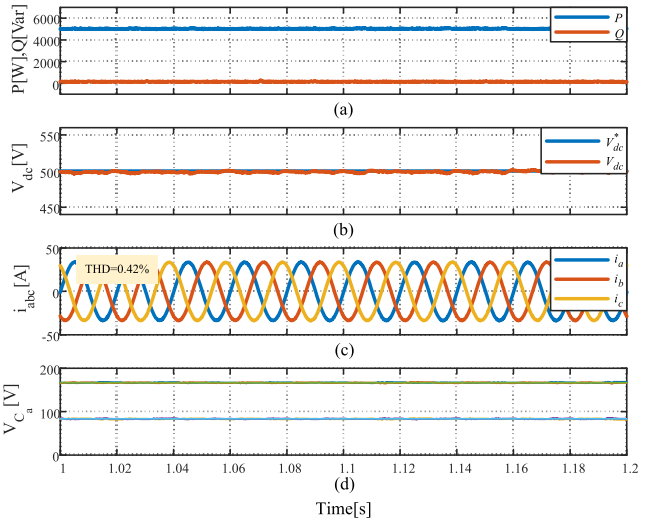

FIGURE 5. Simulation results for traditional three-phase three-leg 7-level T-NNPC converter. [(a) grid-side active and reactive powers,(b) dc-bus voltage, (c) three-phase grid-side currents, (d) capacitor voltages of phase-*a*.]

TABLE 4. System parameters.

Variable	Description	Simulation
P	Active power (kW)	5
e	Grid phase voltage (V)	100
L	Grid-side inductance (mH)	10
R	Grid-side resistance (Ω)	0.01
V_{dc}	DC bus voltage (V)	500
C	FCs capacitance (μF)	3300
C_d	dc-link capacitor capacitance(μF)	4400
T_s	Sampling period (μs)	50

IV. SIMULATION RESULTS

The comparison simulation studies are performed to validate the effectiveness of the proposed multi-layer S-MPDPC scheme by using the Matlab/Simulink software. The main circuit parameters and operation conditions are listed in Table 4. Since the selection of WFs is still an open question, there is no definitive solution to establish an optimal WF to satisfy multiple control objectives simultaneously. For fair assessing the proposed scheme, the optimization of four WFs in conventional MP-DPC cost function shown in (16) are determined based on the principle introduced in [15]. In this design, coefficients $\lambda_p, \lambda_q, \lambda_c, \lambda_d$ in (16) are 1, 1, 50, 20, respectively. To obtain a comparable performance of multiple control objectives, N and K in this design are set to 40, 3, respectively.

A. COMPARATIVE SIMULATION RESULTS WITH TRADITIONAL CONVERTER

The comparison simulation studies for the traditional three-leg based converter and the investigated two-leg based structure is performed in this subsection. Fig. 5 shows the simulation results of the traditional three-phase three-leg

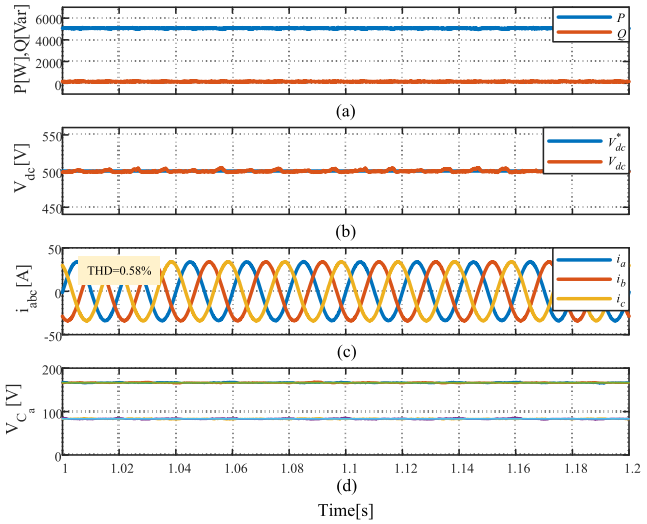

FIGURE 6. Simulation results for three-phase two-leg 7-level T-NNPC converter. [(a) grid-side active and reactive powers,(b) dc-bus voltage, (c) three-phase grid-side currents, (d) capacitor voltages of phase-*a*.]

converter with the conventional WF-based FCS-MPC scheme. Fig. 6 shows the simulation results of the three-phase two-leg topology with the proposed S-MPDPC approach, both studies are conducted under the balanced grid-side voltage conditions. The reference reactive power is set to 0 for unit power factor operation in both studies.

As depicted in figures, active power, reactive power, and dc-bus voltage remain almost constant in both scenarios. The waveforms of current indicate that both schemes can provide satisfactory control performance in terms of symmetrical and sinusoidal grid-side current. The total harmonic distortion (THD) of the three-leg based converter is 0.42%, as shown in Fig. 5. The THD of the three-phase two-leg topology is 0.58%, and the harmonic performance is illustrated in Fig. 7. It can be concluded that the three-phase two-leg topology can provide a comparable performance in terms of high grid-side current quality as compared with the traditional three-leg based converter. Besides, the voltages of four FCs in phase-*a* are well regulated at their nominal values with less fluctuation, as displayed in Fig. 5 and Fig. 6. The results reflect that although only two phase legs are deployed in the three-phase two-leg fault-tolerant structure, a comparable performance can be achieved in comparison to the traditional three-phase three-leg converter.

B. COMPARATIVE SIMULATION RESULTS WITH CONVENTIONAL MPDPC METHOD

Fig. 8 and Fig. 9 demonstrate the steady-state and transient-state performance of the conventional WF-based MPDPC scheme and the proposed multi-layer S-MPDPC approach by using the three-phase two-leg 7-level T-NNPC topology. Initially, the reference dc-bus voltage is set to 500 V, multiple control objectives are well satisfied under the steady-state in both algorithms. The dc-bus voltage steps 500 to 550 V at $t = 1.5$ s, the grid-side active power, currents, and FCs voltage

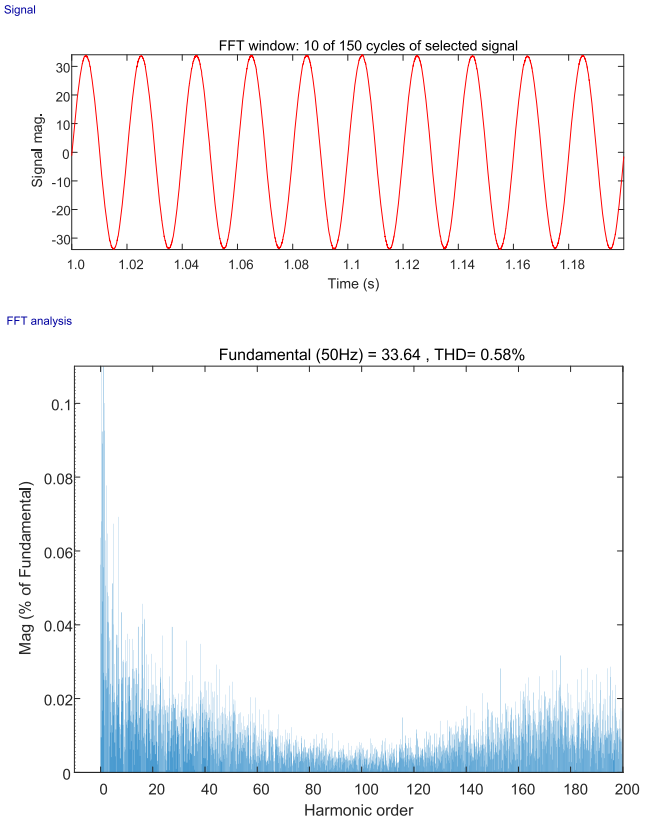

FIGURE 7. Harmonic spectrum of grid-side currents with the proposed S-MPDPC approach.

are correspondingly increased, as shown in Fig. 8 and Fig. 9. Compared with the convention WF-based MPDPC, the proposed scheme produces a comparable transient performance, with less active, reactive power fluctuations as well as dc-bus voltage decrease after the step in dc-link voltage variation, as depicted in Fig. 9. For specific, the conventional WF-based MPDPC scheme leads to a 34.3% overshoot of active power and a 13% degradation of dc-bus voltage, while the active power overshoot and variation percentage in dc-bus voltage of the proposed S-MPDPC approach are 23.3% and 7.2%, respectively. However, due to the optimal switching state is restrained by the SF reduction criterion employed in the proposed S-MPDPC approach, the transient-state performance of the FCs voltage is slightly decreased, as displayed in Fig. 9.

C. DC-LINK CAPACITOR VOLTAGE REGULATION

In the proposed design, the dc-link capacitor voltage is considered in the cost function F_1, as shown in (17). To exam the effectiveness of the proposed algorithm for the dc-link capacitor voltage regulation, the comparative simulation with conventional WF-based MPDPC approach and proposed S-MPDPC method is carried out in this subsection. Fig. 10(a) shows the simulation result of the conventional WF-based MPDPC approach. In this sense, the dc-link capacitor voltages are regulated by the WF λ_d in (16). As depicted in Fig. 10(a), an obvious dc offset is existed between the two

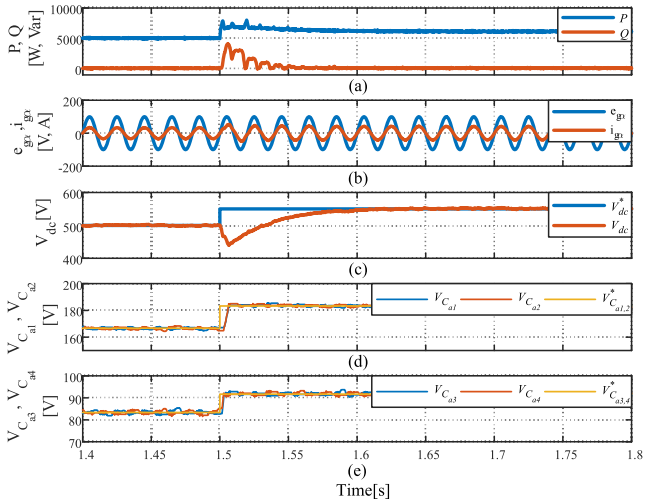

FIGURE 8. Simulation results for conventional WF-based MPDPC method: transient-state performance. [(a) grid-side active and reactive powers,(b) grid-side voltage and current, (c) dc-bus voltage, (d) voltages of outer FCs, (e)voltages of inner FCs.]

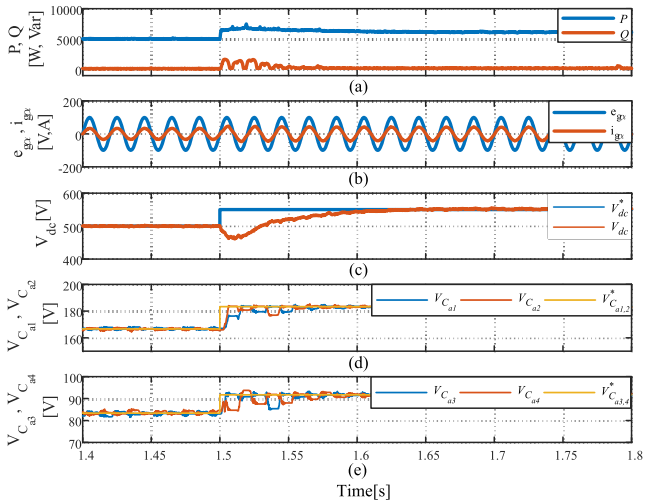

FIGURE 9. Simulation results for proposed S-MPDPC method: transient-state performance. [(a) grid-side active and reactive powers,(b) grid-side voltage and current, (c) dc-bus voltage, (d) voltages of outer FCs, (e)voltages of inner FCs.]

dc-link capacitor voltages. Fig. 10(b) shows the simulation result of the proposed S-MPDPC approach. Due to the incorporation of the dc-link capacitor voltage regulation criterion in (17), the waveform of two capacitors voltages are balanced and symmetrical, while the WF is eliminated.

D. SF REDUCTION

Due to the implementation of FCS-MPC approach results in a variable SF, thereby the concept of average SF is introduced to assess the power loss in this subsection. The average SF is calculated by (20)

$$f_{avg} = \frac{f_{avg,a} + f_{avg,b}}{2} = \sum_{j=a,b} \sum_{s=1}^{8} \frac{N_{js}}{16\Delta T}. \tag{20}$$

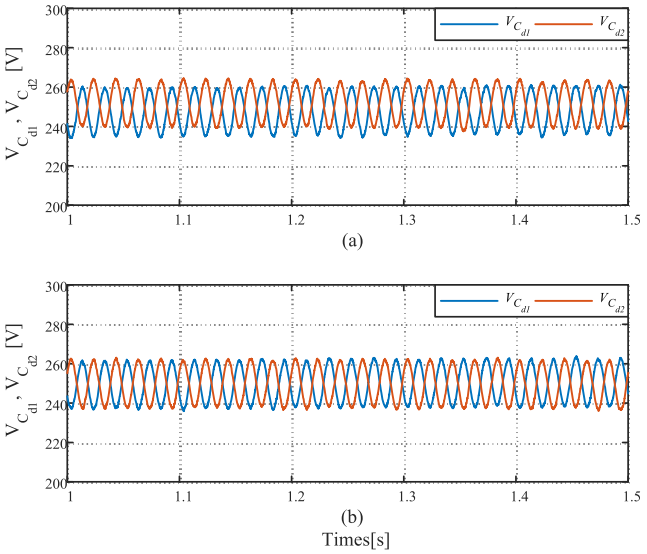

FIGURE 10. Simulation results for three-phase two-leg 7-level T-NNPC converter. [(a) conventional WF-based MPDPC approach, (b) proposed S-MPDPC approach.

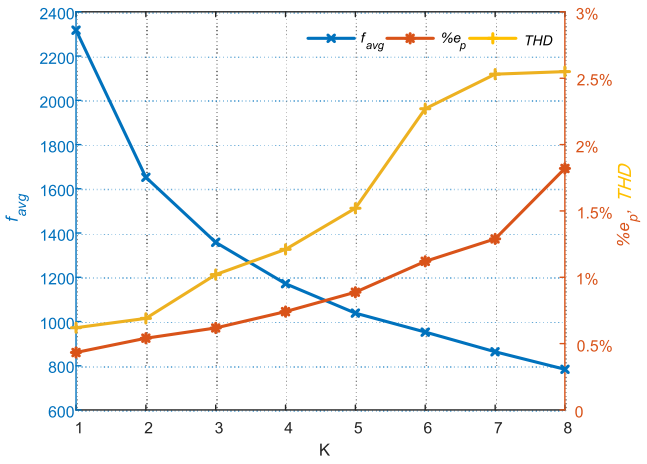

FIGURE 11. Impacts of different values of K.

Here, $f_{avg,a}$ and $f_{avg,b}$ are the average SF of phase-a and phase-b, respectively. N_{js} denotes the number of commutations in upper leg of switch S_{js}, ΔT is the time interval. As analyzed above, the restrain on the SF will affect the power quality of the converter to a certain degree. To exam the power tracing accuracy, a performance metrics named active power tracking error ($\%e_p$) is concerned in this design. The calculation of $\%e_p$ is given by

$$\%e_p = \frac{\frac{1}{n}\sum_{k=0}^{n} |P^*(k) - P(k)|}{P^*} \times 100. \tag{21}$$

Fig. 11 illustrates the impacts of different K on the control performance in terms of SF, active power tracking error $\%e_p$, and THD. As mentioned above, K is not recommended larger than 7. In the case of $K = 1$, which means that the SF reduction is not considered in the optimization process. At this time the $\%e_p$ is 0.433%, THD is 0.58%, f_{avg} is 2317. The high

power quality is obtained through frequent switching actions. In the case of $K = 2$, the SF reduction is incorporated into the optimization criterion, thus the SF is dramatically reduced to 1652. However, due to the restrain on the optimal switching state, the control performance of power tracking error and THD is slightly decreased, as displayed in Fig. 11. In this design, the K is set to 3, at this time the SF is reduced to 1358 while $\%e_p = 0.618\%$, $THD = 1.01\%$, which are acceptable. Under some specific scenario, the SF can be further restrained by increasing K. However, even though the grid-side current can provide a satisfactory performance, the active power fluctuation is correspondingly increased and being impracticable.

V. CONCLUSION

This paper proposes a multi-layer sequential model predictive control (SMPC) without weighting factors (WFs) for a three-phase two-leg 7-level T-NNPC converter. The novelty of this paper lies not only in a multi-objectives optimization design that eliminates the WF by using a cascaded control structure, but also in investigating a post-fault structure so as to improve the fault-tolerant ability of the 7-level T-NNPC converter. Finally, the proposed multi-layer SMPC and investigated fault-tolerant structure are tested under various operating conditions to confirm the effectiveness.

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