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Hybrid and Three-Level Three-Phase Rectifiers Using Interleaved DCM Boost Converters

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ABSTRACT Two new three-phase high-power-factor rectifiers using an interleaved discontinuous conduction mode (DCM) boost converters in a three-level configuration are proposed in this paper. The input currents waveforms follow the input voltages waveforms without a current control loop and the input currents present low current ripple without additional input filter due to the interleaved operation. The main advantage of the proposed rectifiers is the low voltage stress with the voltage applied across all semiconductors and output filter capacitors lower than the output voltage. A high gain rectifier version is presented in a hybrid configuration, including resonant voltage multiplier cell. The structures use only two active switches and current sensors and current control loops are not necessary, becoming a possible solution for low power and low cost applications. The low voltage stress operation and the reduction of the switch current stress due to the interleaved operation allows the reduction of the switches conduction losses of the DCM operation. The experimental results obtained from two prototypes are presented and efficiency equal to 97.26% is obtained for the three-level converter (V_i = 127 V / P = 2 kW) and 94% for the hybrid configuration (V_i = 64 V/ P = 1 kW).

INDEX TERMS Power electronics, ac-dc power converters, wind energy generation.

I. INTRODUCTION

The wind energy generation system is an important renewable energy source and the technological development of high power systems already reached an advance stage [1]–[4]. However, the area of low-power small wind turbines systems (SWT) is not a so established technology and many solutions are proposed mainly in order to obtain high performance minimizing the cost. Wind turbines with a rotor area lower than 200 m^2 are classified as a SWT system including a rated power range of 1-15 kW for residential applications [1].

A challenge is the development of high performance three-phase rectifier stage in the lowest power range (1 kW - 3 kW) due to cost limitations.

Some widely used three-phase ac-dc converter topologies are the two-level and the three-level boost type rectifiers presented in Fig. 1. These topologies normally operate in continuous conduction mode (CCM) and are good solutions for the highest power range in SWT [1]–[5]. However, current sensors and relatively complex control system are necessary to obtain high power factor (HPF) and the cost including several controlled switches, drive circuits and current sensors can be high for the lowest power range.

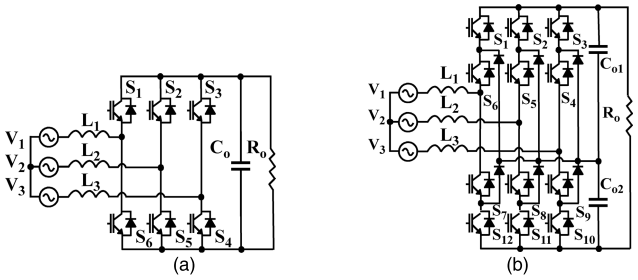

FIGURE 1. Three-phase rectifiers operating in CCM. (a) Two-level boost type. (b)Three-level boost type.

A simple solution for the SWT lowest power range is the three-phase boost type rectifiers operating in discontinuous

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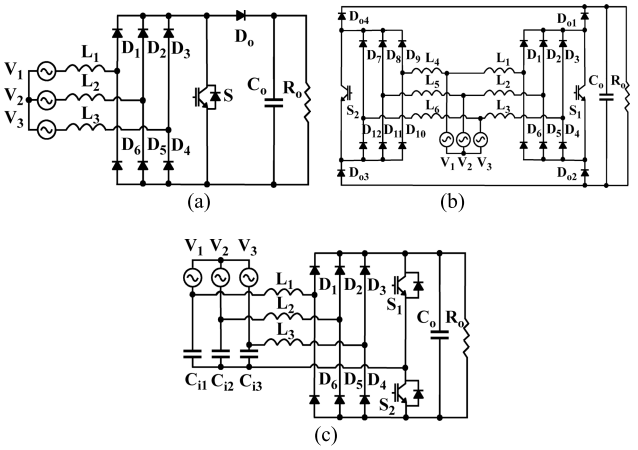

FIGURE 2. Three-phase rectifiers operating in DCM. (a) Single switch boost type. (b) Interleaved boost type. (c) Two switches boost type.

conduction mode (DCM), as the converters presented in Fig. 2 [5]. The DCM operation ensures the operation as a voltage follower where the input current waveform follows the input voltage without current control loops and without current sensors. In addition, the use of only one or two active switches results in low complexity solutions.

However, some problems presented by these topologies limits the rectifier performance.

The typical problems presented by the simplest circuit presented in Fig. 2(a) are the high peak current due to the DCM operation, high electromagnetic interference (EMI) filtering effort and low frequency distortion of mains currents [5]. The HPF and low current distortion are important parameters in order to reduce the losses in the generator and also for the operation with the maximum active power.

The interleaved version presented in Fig. 2(b) increases the component number but improves the operation reducing the current stress using two active switches and reduces the high frequency ripple of the input currents due to the multiphase operation. However, the low frequency distortion of mains currents remains, limiting the rectifier power factor.

Some developments for SWT using the boost DCM are presented in [6]–[8]. Others solutions using the SEPIC DCM are presented in [9]–[11]. An interesting alternative for low cost systems was proposed in [12] and is presented in Fig. 2(c). Two boost converters operate in DCM in an interleaved mode, reducing the conduction losses of the DCM operation and resulting in low current ripple as a CCM operation without additional input filters. The low frequency distortion of the mains current is lower than presented in Fig. 2(a) and Fig. 2(b) due to the circuit configuration. The use of this topology in a small-scale wind energy conversion system is proposed in [13]. The intrinsic inductance of the generator operating with the rectifier input capacitors of the Fig. 2(c) circuit can filter all the high frequency components of the rectifier input currents as presented in [13]. However, the semiconductor voltage stress in all structures presented in Fig. 2 is equal to the output voltage as a classical boost converter.

The output voltage of low power generators can be low in relation to the DC bus voltage of an inverter to be integrated with a microgrid and a high static gain rectifier can be necessary in these applications.

Two new interleaved DCM rectifier configurations presented in Fig. 3 are proposed in this paper in order to reduce the components voltage stress and also increasing the rectifier static gain for low voltage generators.

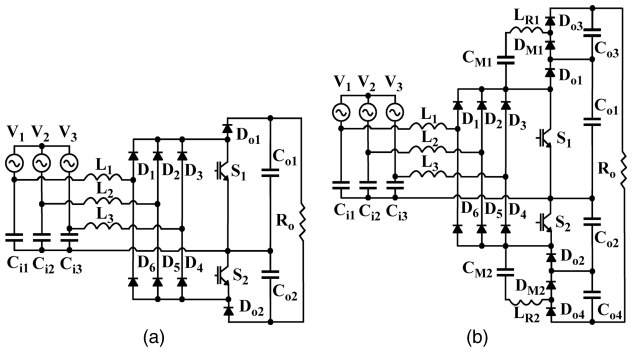

FIGURE 3. Proposed rectifiers. (a) Three-phase three-level DCM interleaved boost rectifier. (b) Three-phase three-level DCM interleaved boost rectifier with voltage multiplier cells (Hybrid configuration).

The three-level configuration, shown in Fig. 3(a), is obtained from Fig. 2(c) rectifier including two output diodes ($D_{o1} - D_{o2}$) and two output capacitors ($C_{o1} - C_{o2}$) with a middle point connection, reducing the semiconductor voltage stress to half of the output voltage. The output voltage of the proposed rectifier is the double of the structures presented in Fig. 2 for the same operation conditions.

A hybrid version of the three-level HPF rectifier is proposed in Fig. 3(b) including a resonant voltage multiplier cell in each interleaved boost, presenting an output voltage four times higher than the structures presented in Fig. 2. The voltage across the semiconductors and filter capacitors is four times lower than the output voltage in the hybrid structure.

The proposed rectifier's configuration also offer automatic voltage balancing and symmetric voltage across the output capacitors, which makes it possible to design the converter with lower voltage-rated component that offer better performance and are less expensive than their high-voltage-rated counterparts. The proposed rectifier's output configuration is suitable for the integration with different structures as half-bridge inverters and different types of multilevel inverters.

The operation of the switches S_1 and S_2 must be complementary in the original rectifier presented in Fig. 2(c) due to the circuit configuration. The usual rectifier modulation is the operation with constant duty-cycle $D = 0.5$ and variable switching frequency [12], [13]. However, a large frequency range can be necessary to regulate the output voltage in some applications.

The operation of each interleaved boost converter presented in Fig. 3(a) and in Fig. 3(b) is independent with the inclusion of the output diodes ($D_{o1}-D_{o2}$) and filter capacitors ($C_{o1}-C_{o2}$) and different modulation can be used. Besides the frequency modulation, the classical multiphase PWM modulation with constant switching frequency and variable duty-cycle is proposed in this paper and classical analog PWM integrated circuits and low cost pulse transformer can be used in the control and command circuits.

II. THREE-PHASE RECTIFIERS OPERATION ANALYSIS

A. AC-DC CONVERTER OPERATION

The operation of the input section of the rectifiers presented in Fig. 3(a) and in Fig. 3(b) is the same and is similar to the circuits presented in Fig. 2 because all these topologies are derived from the boost DCM converter. The operation is detailed for the three-level rectifier presented in Fig. 3(a). The operation of the resonant voltage multiplier cell is added to the basic rectifier operation to explain the operation of the hybrid rectifier version. The three-level three-phase rectifier presented in Fig. 3(a) is composed by the input capacitors (C_{i1}-C_{i2}-C_{i3}), three input boost inductors (L_1-L_2-L_3), two active switches (S_1-S_2) and two output diodes (D_{o1}-D_{o2}). The output capacitors (C_{o1}-C_{o2}) share the total output voltage. The input capacitors creates a virtual neutral that is connected to the midpoint between two switches S_1 and S_2 and also to the midpoint of two output capacitors C_{o1} and C_{o2}.The operation of the switches S_1 and S_2 are integrated with the input three-phase diode bridge (D_1-D_6). There are different circuit configurations depending of the three-phase input voltages segment and the segment (c) shown in Fig. 4(a) is considered for the presentation of the rectifier operation stages. The operation in the others segments of the input voltage are similar. The input rectifier diodes D_1-D_2-D_3 conduct when their correspondent phase voltages are positive and the diodes D_4-D_5-D_6 conduct when their correspondent phase voltages are negative. Thus, only the diodes D_1-D_2-D_4 are conducting in the segment (c) where $V_1 > 0$, $V_2 > 0$ and $V_3 < 0$. The operation stages of three-phase rectifier during a switching cycle operating with $D = 0.5$ within the segment (c) is shown in Fig. 4 and the theoretical current waveforms are presented in Fig. 5.

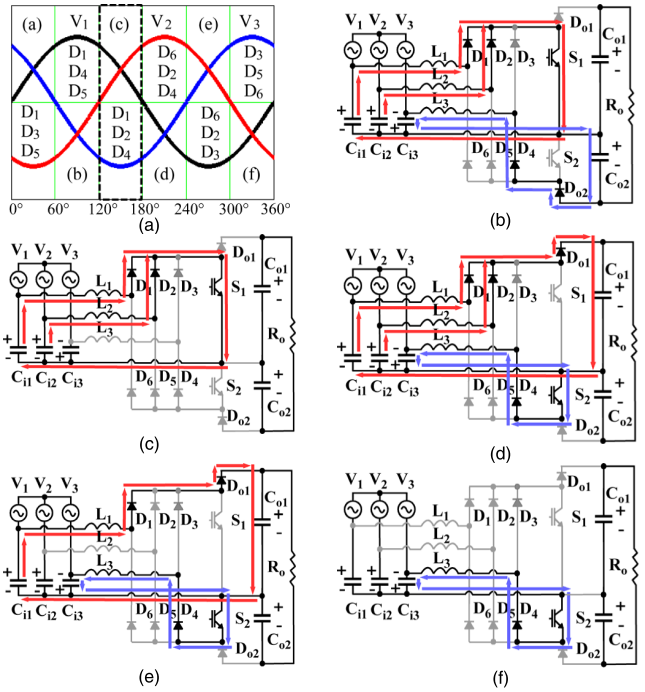

FIGURE 4. Input voltages segments and the three-phase rectifier operation stages. (a) Input voltages segments and input diodes conduction period. (b) First stage. (c) Second stage. (d) Third stage. (e) Fourth stage. (f) Fifth stage.

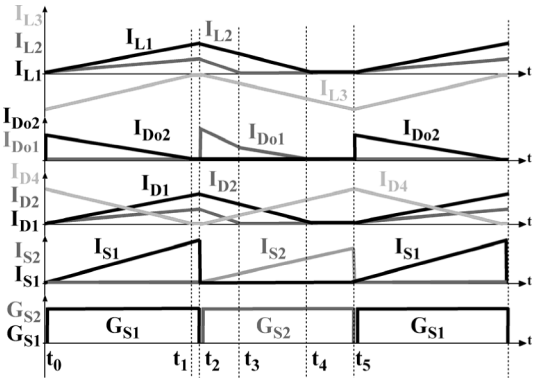

FIGURE 5. Three-phase three-level rectifier theoretical waveforms.

1) FIRST STAGE - Fig. 4(B)

The switch S_1 is turned-on at the instant t_0 and the voltages V_{Ci1} and V_{Ci2} are applied across the input inductor L_1 and L_2 through the rectifier diodes D_1 and D_2, storing energy in these inductors. The energy stored in the inductor L_3 is transferred to DC bus capacitors C_{o2} through the rectifier diode D_4 and output diode D_{o2}.

2) SECOND STAGE - Fig. 4(C)

The switch S_1 remains turned-on and the inductors L_1 and L_2 continue storing energy. However, the energy transference from inductor L_3 to the capacitor C_{o2} is finished at the instant t_1 due to the DCM operation. The current at the inductor L_3 is null, blocking the diodes D_4 and D_{o2} without reverse recovery current due to the low di/dt.

3) THIRD STAGE - Fig. 4(D)

At the instant t_2, the switch S_1 is turned-off and the switch S_2 is turned-on. The energy stored in the input inductors L_1 and L_2 are transferred to the output capacitor C_{o1}. The input inductor L_3 stores energy with the input voltage V_{Ci3} applied through the switch S_2 and diode D_4.

4) FOURTH STAGE - Fig. 4(E)

The current at the inductor L_2 decreases until zero at the instant t_3 blocking the diode D_2. The energy transfer from

the inductor L_1 to the capacitor C_{o1} remains and the inductor L_3 is still storing energy.

5) FIFTH STAGE - Fig. 4(F)

The energy transference from the inductor L_1 is finished at the instant t_4 blocking the diodes D_1 and D_{o1}. Only the input inductor L_3 remains storing energy until the instant t_5 when the switch S_2 is turned-off and S_1 is tuned-on, returning to the first operation stage.

The theoretical current waveforms are presented in Fig. 5. The switches S_1 and S_2 turn-on with zero current switching (ZCS), reducing the switching losses. All diodes are blocked with low di/dt and without reverse recovery current due to the DCM operation.

The voltage stress in all semiconductors is equal to the output capacitor voltage (C_{o1}-C_{o2}) that is equal to half of the output voltage due to the three-level configuration.

B. VOLTAGE MULTIPLIER CELL OPERATION

The operation of the input section of the hybrid rectifier presented in Fig. 3(b) is basically the same of the three-level rectifier presented in Fig. 3(a). Therefore, only the operation of the voltage multiplier cell included in the hybrid rectifier is explained for this topology.

The capacitor C_{M1} is responsible by the energy transference from the output capacitor C_{o1} to C_{o3}, increasing the static gain. This energy transference can be accomplished in two different forms: the classical transference and the resonant transference. The classical energy transference in switched capacitor circuits can be classified in three different operating modes as presented in Fig. 6(a): Total Charge (TC), Partial Charge (PC), and No Charge (NC) [14], depending of some circuit parameters as the switching frequency, capacitance values, intrinsic resistances of the capacitors and semiconductors (R_{eq}). The relation between the constant time of the circuit and the switching period defines the charge mode. Some analysis presented in the literature as in [14], [15], shows that the TC mode presents greater loss due to the higher peak current; however, it requires a lower capacitance value. The NC mode presents less loss, but it requires higher capacitance values. Considering the relation losses and volume, PC is the best operating mode. However, even for the operation in the PC mode, a high switching frequency and a capacitance of hundreds of microfarads can be necessary increasing the cost and volume of the converter.

Other problem is that the intrinsic ZCS switch turn-on of the DCM operation cannot be maintained with the switched capacitor energy transference and a peak current can occurs at the commutation instant, increasing the switching losses.

An alternative to solve these problems is the inclusion of a small resonant inductor between the capacitors as presented in Fig. 6(b), becoming the energy transference resonant.

The resonant operation limits the di/dt and the peak current of the energy transference, maintaining the ZCS switch turn-on in the DCM operation and reducing the losses. The capacitor used in the energy transference can be significantly

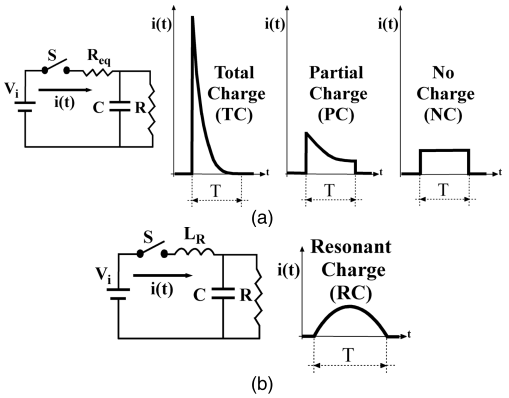

FIGURE 6. Energy transference in a switched capacitor circuit. (a) Classical transference. (b) Resonant transference.

reduced, decreasing the volume and cost and maintaining a high efficiency. Therefore, a small resonant inductor (L_{R1}-L_{R2}) is used in the voltage multiplier of the hybrid configuration allowing the use of reduced voltage multiplier capacitance (C_{M1}-C_{M2}) [16]. The operation of the resonant voltage multiplier circuit and the theoretical waveforms are presented in Fig. 7 and in Fig. 8 respectively.

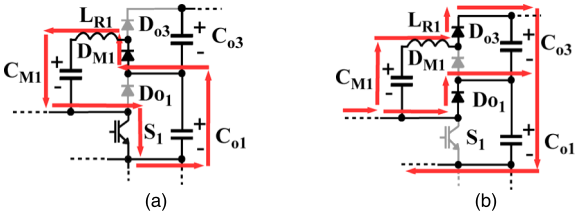

FIGURE 7. Operation stages of the voltage multiplier cell. (a) Switch turned-on. (b) Switch turned-off.

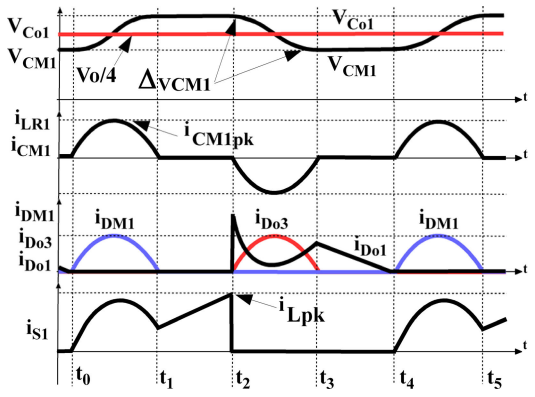

FIGURE 8. Theoretical waveforms of the resonant voltage multiplier cell.

The output DC bus capacitors (C_{o1}-C_{o4}) are considered much higher than the voltage multiplier capacitors and operate as a constant voltage source ($V_o/4$) during the switching period. When the switch S_1 is turned-on at the instant t_o, there is the energy transference in a resonant way from the output capacitor C_{o1} to the multiplier capacitor C_{M1} through the

diode D_{M1}, resonant inductor L_{R1} and switch S_1. Otherwise, when the switch S_1 is turned-off, the multiplier capacitor C_{M1} transfers the energy in a resonant way to the output capacitor C_{o3} through the diode D_{o3}, resonant inductor L_{R1} and diode D_{o1}, ensuring that output capacitors C_{o1} and C_{o3} will be charge with the same voltage level.

The resonance frequency is calculated by (1) and the half resonant period must be lower than the switch turn-on period, blocking the diode D_{M1} at the instant t_1 with zero current.

The voltage and current variation in the multiplier capacitor are presented in (2) and (3) respectively, where (Δ_{VCM1}) is the voltage ripple of the multiplier capacitor.

$$\omega_o = \frac{1}{\sqrt{L_{R1} \cdot C_{M1}}} \tag{1}$$

$$i_{CM1}(t) = \sqrt{\frac{C_{M1}}{L_{R1}}} \frac{\Delta_{VCM1}}{2} \cdot \sin(\omega_o \cdot t) \tag{2}$$

$$V_{CM1}(t) = \frac{V_o}{4} - \frac{\Delta_{VCM1}}{2} \cdot \cos(\omega_o \cdot t) \tag{3}$$

The rectifier input inductor remains storing energy during the switch turn-on period until the instant t_2 when the switch S_1 is turned-off. When the switch S_1 is turned-off, the energy stored in the input inductors is transferred to the output capacitor C_{o1} through the diode D_{o1}. There is also the resonant energy transference from the multiplier capacitor C_{M1} to the output capacitor C_{o3} through the diodes D_{o1} and D_{o3}. At the instant t_3 the resonant energy transference is finished and energy transference of the input inductor remains until the instant t_4.

With the three-level configuration and with the inclusion of the voltage multipliers, the rectifier output voltage is four times higher than the classical structures presented in Fig. 2 and the voltage stress in all rectifier semiconductors is equal to one quarter of the output voltage. The switches turn-on is ZCS and all diodes are blocked with zero current without reverse recovery current problems, reducing the switching losses.

III. SIMPLIFIED DESIGN PROCEDURE

The rectifiers operating in DCM present an intrinsic limitation of the maximum input power because the rectifier operates as a constant input power source for a constant input voltage and a fixed duty-cycle. Therefore, the design of the input inductors defines the maximum input power of the rectifier operating at maximum input voltage with the nominal duty-cycle. The lowest current and voltage stress can be obtained designing the rectifiers at the boundary of CCM and DCM at the maximum allowed power. The voltage across the DC bus output capacitors that is also the voltage across all semiconductors, must be higher than the peak of the maximum line generator input voltage to maintain the HPF operation. A value equal this limit is chosen for the lowest semiconductor voltage stress. The maximum voltage applied to the input inductors during energy storing stage is half of the peak line voltage. The voltage at each boost output, that is the DC bus capacitor, is equal to the peak line voltage. Therefore, the static gain of each boost converter is equal to 2 and the nominal duty-cycle must be equal to $D = 0.5$ operating at the boundary of DCM and CCM. The output voltage of the three-level rectifier is equal to (4).

$$V_o = V_{Co1} + V_{Co2} = 2 \cdot V_{Lpk} = 2 \cdot \sqrt{3} \cdot V_{pk} \tag{4}$$

where V_{Lpk} and V_{pk} are the generator line and phase peak voltages respectively. The input inductors can be calculated by (5) operating with the maximum power (P), duty-cycle $D = 0.5$ and at the boundary of CCM and DCM.

$$L = L_1 = L_2 = L_3 = \frac{V_{pk}^2}{3 \cdot P \cdot f_s} \tag{5}$$

Considering the rectifier power equal to (6), where R is the load resistance, and replacing (4) and (6) in (5), the input inductor design is obtained and presented in (7) for the three-level rectifier.

$$P = \frac{V_o^2}{R} \tag{6}$$

$$L_1 = L_2 = L_3 = \frac{R}{36 \cdot f_s} \tag{7}$$

The input inductor value for the operation at the boundary of the DCM and CCM is a function only of the load resistance and the switching frequency.

Considering the hybrid configuration, the output voltage is equal to (8).

$$V_o = V_{Co1} + V_{Co2} + V_{Co3} + V_{Co4} = 4 \cdot \sqrt{3} \cdot V_{pk} \tag{8}$$

Replacing (6) and (8) in (5), the input inductor calculation for the hybrid configuration is obtained and presented in (9), as a function of the load resistance and switching frequency.

$$L = L_1 = L_2 = L_3 = \frac{R}{144 \cdot f_s} \tag{9}$$

If the output power is reduced, the switching frequency must be increased or the switches duty-cycle must be reduced to regulate the output voltage and the rectifier will operate in DCM.

The maximum input inductor peak current is calculated by (10).

$$i_{Lpk} = \frac{\sqrt{3} \cdot V_{pk} \cdot D}{2 \cdot L \cdot f_s} \tag{10}$$

The input capacitance (C_{i1}-C_{i3}) can be calculated by the charge variation and by the high frequency voltage ripple specification (Δ_{VCi}) as shown in (11).

$$C_{i1} = C_{i2} = C_{i3} = \frac{i_{Lpk}}{8 \cdot \Delta_{VCi} \cdot f_s} \tag{11}$$

The DC bus capacitors (C_{o1}-C_{o4}) are defined by the energy demand of the second stage connected with the rectifier, as the low frequency input ripple of a grid connected inverter.

The multiplier capacitors (C_{M1}-C_{M2}) used in the hybrid configuration to increase the output voltage are calculated

also by a voltage ripple specification (Δ_{VCM}). Thus, the multiplier capacitors are calculated by (12).

$$C_{M1} = C_{M2} = \frac{P}{\Delta_{VCM} \cdot V_o \cdot f_s} \tag{12}$$

The resonant inductor (L_{R1}-L_{R2}) allows the ZCS switch turn-on commutation and limits the peak current in the energy transference between the capacitors, reducing the losses. The peak current in the energy transference is equal to (13) and the energy transference period ($T_o/2$) is presented in (14).

$$i_{CM1pk} = \sqrt{\frac{C_{M1}}{L_{R1}}}\frac{\Delta_{VCM1}}{2} \tag{13}$$

$$\frac{T_o}{2} = \pi \cdot \sqrt{L_{R1} \cdot C_{M1}} \tag{14}$$

The parameters used in the converters design and the components values used in the prototypes are presented in Table 1.

TABLE 1. Design specifications and prototype components.

Parameter / Value	Three-level rectifier Fig. 3(a)	Hybrid rectifier Fig. 3(b)
Peak phase input voltage	V_{pk}=180 V	V_{pk} = 90 V
Peak line input voltage	V_{Lpk} = 311 V	V_{Lpk} = 155.5 V
Output capacitors voltage	C_{o1}-C_{o2} = 311 V	C_{o1}-C_{o4} = 155.5 V
Total output voltage	V_o = 622 V	V_o = 622 V
Output power	P = 2 kW	P = 1 kW
Load	R = 193 Ω	R = 386 Ω
Switching frequency	f_s = 45 kHz	f_s = 24.5 kHz
Line frequency	f_L = 60 Hz	f_L = 60 Hz
Nominal duty-cycle	D = 0.5	D = 0.5
Input capacitor voltage ripple	Δ_{VCi}= 25 V	Δ_{VCi}= 25 V
Multiplier capacitor voltage ripple	–	Δ_{VCM}= 45 V
S_1-S_2	65C7019	65C7019
D_{o1}-D_{o4}/ D_{M1}-D_{M2}/ D_1-D_6	MUR1560	MUR1560
C_{o1} - C_{o4}	470 µF/400V *	470 µF/400V *
C_{i1} - C_{i2} - C_{i3}	2.7 µF/400V **	2.7 µF/400V **
C_{M1}-C_{M2}	-	2.2 µF/400V**
L_1 – L_2 – L_3	100 µH - EE 42/20	100 µH - EE 42/20
L_{R1} - L_{R2}	-	5 µH/ air core

* Electrolytic capacitor **Polypropylene capacitor

IV. EXPERIMENTAL RESULTS

The prototypes experimental results are presented operating at the nominal specifications shown in Table 1. As the hybrid rectifier has double gain, its input voltage has been specified with half the value of the three-level rectifier. Thus, the output voltage will be the same for the both rectifiers. To maintain the same input current levels, the rated power of the three-level rectifier was specified at 2 kW and the rated power of the hybrid rectifier at 1 kW. The same inductance value was used in both rectifiers and the switching frequency 45 kHz was used for the three-level rectifier and 24.5 kHz for the hybrid rectifier.

The output voltage and the voltage and current in the switch S_1 are presented in Fig. 9. The switch voltage is the half of total DC bus for the three-level configuration and is half of this value for the hybrid configuration. The switch turn-on is ZCS in both configurations.

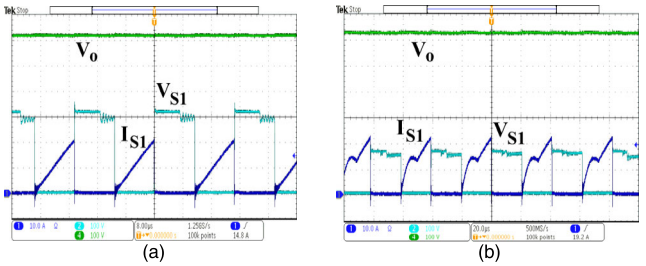

FIGURE 9. Output voltage and switch voltage and current. (a) Three-level rectifier (100V/div) (10A/div) (8µs/div). (b) Hybrid rectifier (100V/div) (10A/div) (20µs/div).

The resonant energy transference of the capacitor C_M in hybrid configuration can be observed in the switch current in Fig. 9(b).

The input inductors currents (I_{L1}-I_{L3}) are shown in Fig. 10. The operation close to the boundary of the DCM and CCM can be observed in the I_{L3} current.

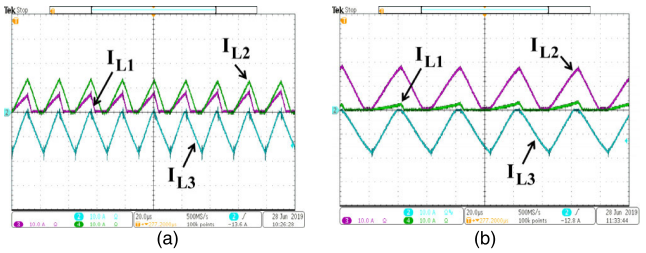

FIGURE 10. Input inductor currents. (a) Three-level rectifier (10 A/div) (20µs/div). (b) Hybrid rectifier (10 A/div) (20µs/div).

The current and voltage in the output diodes are shown in Fig. 11. All diodes are blocking without reverse recovery current due to the DCM operation.

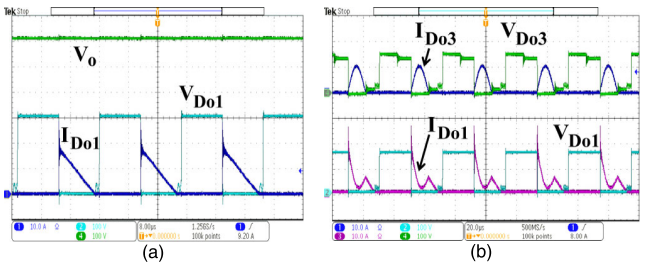

FIGURE 11. Diodes voltage and current. (a) Three-level rectifier output diode voltage and current (100 V/div) (10 A/div) (8µs/div). (b) Hybrid rectifier output diodes voltage and current (100 V/div) (10 A/div) (20µs/div).

The voltage across the DC bus capacitors are presented in Fig. 12. The capacitors voltages are balanced and are close to the value specified in Table 1.

The three-phase input currents and input voltage in phase 1 are presented in Fig. 13. The waveforms are similar in both rectifiers and present low current ripple without additional input filter even operating in DCM.

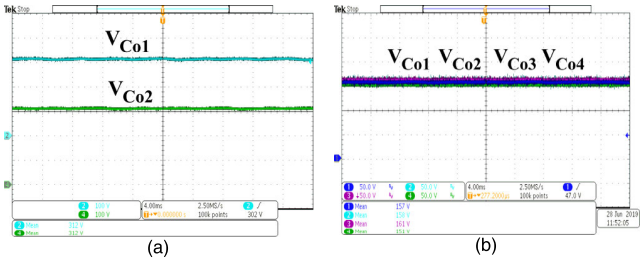

FIGURE 12. DC bus capacitors voltages. (a) Three-level rectifier capacitors voltages (V_{co1} -V_{co2}) (100V/div) (4ms/div).

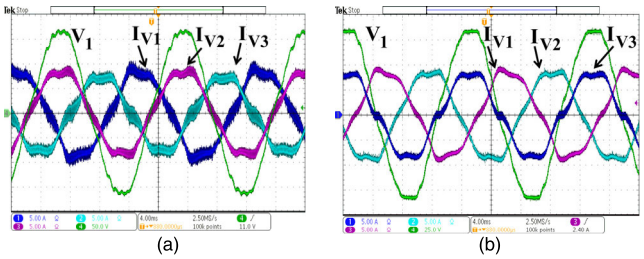

FIGURE 13. Input voltage and input currents. (a) Three-level rectifier (50 V/div) (5 A/div) (4ms/div). (b) Hybrid rectifier (25 V/div) (5 A/div) (4ms/div).

The THD of the input voltage and current presented in Fig.14 are equal to 4.77% and 7.68% respectively for the three-level rectifier. Thus, the current distortion relative to the rectifier operation is equal to 2.91%.

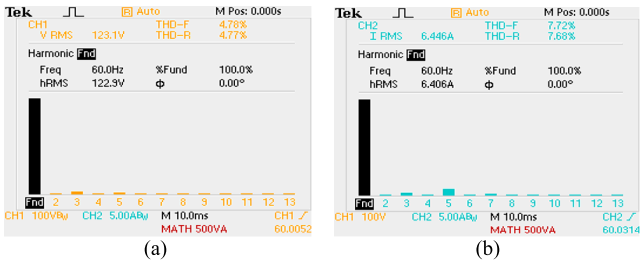

FIGURE 14. THD of the three-level rectifier. (a) THD of the phase input voltage. (b) THD of the phase input current.

The THD of the input voltage and current presented in Fig.15 are equal to 4.72% and 8.18% respectively for the hybrid rectifier. Thus, the current distortion relative to the rectifier operation is equal to 3.41%.

The power factor of the three-level and hybrid rectifiers is equal to 0.99 and 0.992 respectively as shown in Fig. 16.

The classical PWM analog integrated circuits SG3525 is used in the command circuit of the proposed rectifiers operating with the classical PWM modulation with fixed switching frequency and variable duty-cycle. The control circuit is a single output voltage control loop using a PI controller. The load transient from 20% to 100% of the output power is presented in Fig. 17 for the three-level and the hybrid rectifiers. The under voltage presented in the load transient is equal to 6.5% and the settling time close to 15 ms for both rectifiers.

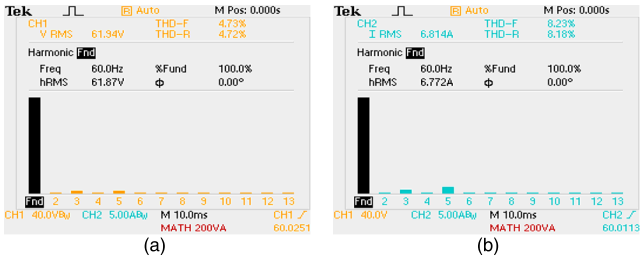

FIGURE 15. THD of the hybrid rectifier. (a) THD of the phase input voltage. (b) THD of the phase input current.

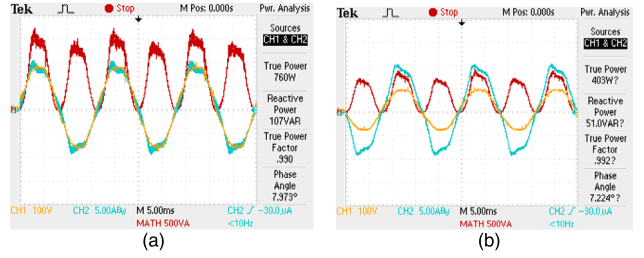

FIGURE 16. Rectifier power factor. (a) Three-level rectifier power factor. (b) Hybrid rectifier power factor.

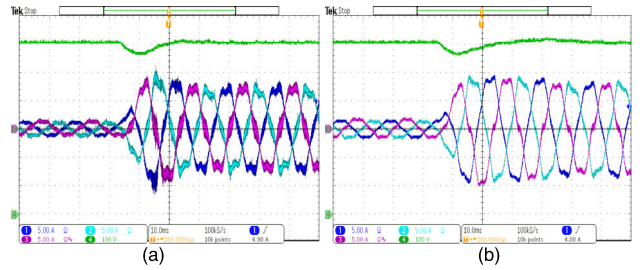

FIGURE 17. Rectifiers load transient 20% to 100% (100 V/div) (5 A/div) (10ms/div). (a) Three-level rectifier. (b) Hybrid rectifier.

The load transient from 100% to 20% of the output power is presented in Fig. 18 for the three-level and the hybrid rectifiers.

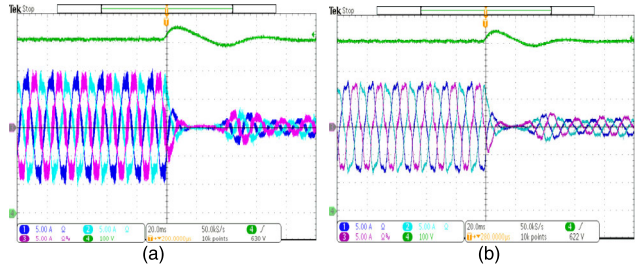

FIGURE 18. Rectifiers load transient 100% to 20% (100 V/div) (5 A/div) (20ms/div). (a) Three-level rectifier. (b) Hybrid rectifier.

The voltage overshoot presented in the load transient is equal to 8% and the settling time close to 60 ms for both rectifiers.

The efficiency curves for both rectifiers as a function of the output power are shown in Fig. 19. The efficiency at the

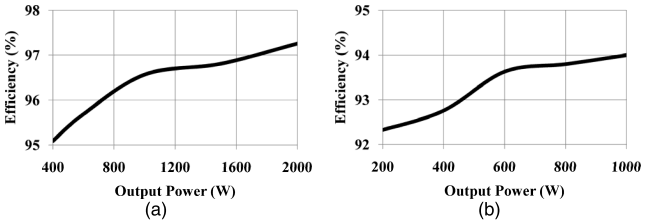

FIGURE 19. Efficiency curve. (a) Three-level rectifier. (b) Hybrid rectifier.

nominal output power is equal to 97.26% for the three-level rectifier and 94% for the hybrid rectifier.

The results of the proposed rectifier's losses analyses are presented in Fig. 20, considering the components and specifications presented in Table 1. The average current in the output diodes of the three-level rectifier (D_{o1}-D_{o2}) and in the voltage multiplier diodes and output diodes of the hybrid rectifier (D_{o1}-D_{o4}/D_{M1}-D_{M2}) are equal to the output current.

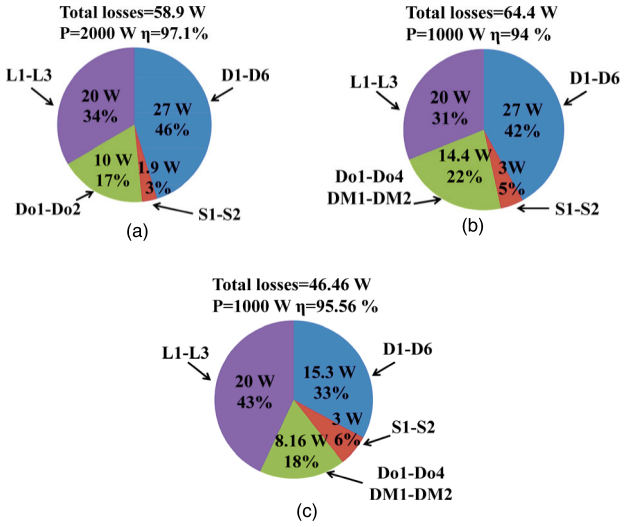

FIGURE 20. Losses analysis. (a) Three-level rectifier. (b) Hybrid rectifier. (c) Hybrid rectifier using low voltage schottky diodes.

Therefore, the modifications of the original structure presented in Fig. 2(c) to the three-level configuration with the inclusion of the output diodes increases 10 W in the converter losses. However, the semiconductors voltage is reduced to half of the output voltage and the static gain is the double of the original structure. The inclusion of the output diodes and voltage multiplier diodes in the hybrid configuration increases the rectifier losses in 14.4 W using conventional ultra-fast diodes. But the semiconductors voltage is reduced to a quarter of the output voltage and the static gain is four times higher than the original structure. The conduction losses of the switches S_1-S_2 is increased in only 1.1 W using the resonant voltage multiplier in the hybrid configuration.

However, the most part of the rectifier's losses occurs in the input inductors L_1-L_3 due to the DCM operation and in the input rectifier diodes D_1-D_6. The total losses in these components are equal in the three-level and in the hybrid configuration even the hybrid rectifier operating with nominal output power (P = 1000 W) half of the output power of the three-level rectifier (P = 2000 W). This occurs due to the low input voltage specification of the hybrid rectifier (V_{pk} = 90 V) resulting in the same input current for both topologies.

Therefore, a lower efficiency is expected in the rectifier operating with the lower input voltage. The efficiency of the three-level rectifier is equal to 97.1% and the efficiency of the hybrid rectifier is equal to 94% using conventional ultra-fast diodes. Considering the use of low voltage (250V) schottky diode for all rectifier diodes, the efficiency of the hybrid rectifier is increased to 95.5%, as presented in Fig. 20(c).

V. COMPARATIVE ANALYSIS

A comparison of the proposed converters with three Boost type rectifiers operating in DCM is presented in Table 2. The rectifiers do not need input current control due to the DCM operation, avoiding the use of current sensors and input currents control loop. Therefore, all these rectifiers use a single output voltage control with a voltage sensor.

TABLE 2. Comparative analysis.

Characteristic	Rect. of Fig. 2(a) [5]	Rect. of Fig. 2(b) [5]	Rect. of Fig. 2(c) [12]	Proposed Three-level Rect.	Proposed Hybrid Rect.
Input current control	0	0	0	0	0
Current sensor	0	0	0	0	0
Output voltage control	1	1	1	1	1
Voltage sensor	1	1	1	1	1
Number of switches	1	2	2	2	2
Number of diodes	7	16	6	8	12
Number of inductors	3	6	3	3	5
Number of polypropylene capacitors	0	0	3	3	5
Number of electrolytic capacitors	1	1	1	2	4
Voltage stress on switches	V_o	V_o	V_o	$V_o/2$	$V_o/4$
Voltage stress on output diodes	V_o	$V_o/2$	-	$V_o/2$	$V_o/4$
Voltage stress on electrolytic capacitors	V_o	V_o	V_o	$V_o/2$	$V_o/4$

The rectifier of Fig. 2(a) [5] has the advantage of a single switch realization. However, the switch voltage stress is equal to the output voltage level and the current stress is higher than the others topologies. An additional input filter is necessary only in this topology due to the DCM operation.

The interleaved version presented in Fig. 2(b) [5] increases the component count but improves the operation reducing the current stress using two active switches and reduces the high frequency ripple of the input currents due to the multiphase operation. However, the switches voltage stresses are equal to the output voltage level.

The low cost rectifier presented in Fig. 2(c) [12] operates in DCM in an interleaved mode, reducing the conduction losses of the DCM operation and resulting in low current ripple as a CCM operation without additional input filters. However, the switches voltage stresses are equal to the output voltage level.

The proposed rectifiers have the ability of dividing the voltage stress across the switches through the three-level and hybrid concepts without additional switches when compared to the rectifier presented in Fig. 2(b) and Fig. 2(c). The switches voltage stresses are equal to the half of output voltage level for the three-level rectifier and one fourth of the output voltage level for the hybrid rectifier, allowing the use of switches with lower conduction losses.

VI. CONCLUSION

Three-phase high-power-factor rectifiers based on an interleaved DCM boost converters in a three-level configuration and in a hybrid configuration are proposed in this paper. The main characteristics of the proposed converters are low input current ripple, low input current distortion, high power factor and low voltage stress in all semiconductors and output filter capacitors. The proposed structures also present high gain compared to the classical rectifier with the same operation characteristics. The structures use only two active switches and current sensors and current control loops are not necessary, becoming a possible solution for low power and low cost applications.

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