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Energy Efficient Generic Demodulator for High Data Transmission Rate Over an Inductive Link for Implantable Devices

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ABSTRACT In this paper, we present a new Carrier Width Modulation (CWM) scheme for simultaneous transfer of power and data over a single inductive link. An ultra-low power CWM demodulator is also proposed. Unlike conventional demodulators for a similar modulation scheme, the proposed CWM circuit allows higher-speed demodulation and simple implementation. It works well as a generic demodulator operating at a frequency range between 10 and 31 MHz. It also supports a wide range of data rates under any selected frequency from the operating range. A CWM-based scheme encoding two-bit-per-symbol, called Quad-level CWM (QCWM) is also proposed. The latter allows high data-rates-to-frequency ratios. Using a 0.13-μm CMOS process and 1.2 V power supply, both CWM and QCWM demodulators were implemented and fabricated. They respectively occupy die sizes of 2137 and 3256 μm^2 and dissipate, in worst conditions, 16.9 and 35.5 μW. Compared with state-of-the-art demodulators used for inductive forward data transmission, the proposed demodulators are distinctive given their low-energy efficiency and small silicon areas.

INDEX TERMS Carrier width modulation, demodulator, downlink data transmission, inductive link.

I. INTRODUCTION

There has been strong interest for wireless power transfer and fast data communication to Implantable Medical Devices (IMDs) [1], [2]. The main goal is to ensure high power transfer efficiency and reliable high speed data transfer, while maintaining a small size and low power consumption of the implantable electronic circuits [3].

Among several wireless technologies such as RF [4], capacitive [5], ultrasonic [6], and optical [7] links, the inductive link, which consists of a magnetic-coupled pair of coils, is the most widely used wireless technique for both power and data transfer. This is mainly due to its ability to provide both power and bidirectional data transmission with appropriate reliability, safety, cost, and simplicity of implementation [8], [9].

Although considerable progress has been achieved in inductively coupled links for IMDs, many obstacles and design challenges still need to be addressed. Actually, the design of a transcutaneous data and power transmission system poses two main challenges. The first one is to achieve an efficient power transfer and high data rates at the same time. In fact, for conventional modulation techniques, the bandwidth needs to be widened to obtain high data rates, but narrowed to obtain efficient power delivery. The second challenge is to implement a small size and low power consumption IMD when establishing a robust high-speed communication link. The first challenge was addressed in our previous paper [10], and we proved using simulations that the bandwidth of our proposed CWM is independent of the quality factor of the primary and secondary coils Q_1 and Q_2,

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respectively. Therefore, high Q factors associated with narrow bandwidth do not limit the CWM communication rate.

In this paper, we mainly address the second challenge targeting downlink communications (from the external device to the IMD); particularly we focus on the demodulator circuit which plays a major role in data integrity and overall power efficiency of the IMD.

Several techniques have been proposed for downlink communication. Some notable proponents are Frequency Shift Keying (FSK) [11], Phase Shift Keying (PSK) [12], and Amplitude Shift Keying (ASK) modulation techniques [13]. PSK, FSK and their derivatives may offer high data rates and high immunity against noise, but they suffer from high implementation complexity and power consumption [14]. ASK is the most commonly used approach due to its easy implementation and the low power consumption of its demodulation circuit compared to other methods. However, the ASK scheme is less robust against disturbances that affect the carrier amplitude, such as interference and coupling variations. For better immunity, ASK with 100% amplitude modulation index; called On-Off keying (OOK); can be used [15]. Considered as the simplest and the least power-hungry modulation technique, special attention will be given to OOK and an analysis of its demodulator limitations will be discussed here to motivate our proposed solution.

Despite its low design complexity and reduced power consumption, the data rate of OOK modulation, as it is the case for ASK modulation, is low due to the limited speed of its demodulator circuit. Figure 1 shows a typical block diagram of a conventional OOK demodulator. It uses an envelope detector (ED), which represents the weakest-link of the chain in ASK demodulators. Typically, the ED is composed of a diode followed by a capacitor C in parallel with a resistor R, as shown in Fig. 1. The time constant $\tau = RC$ determines the discharging time of the capacitor. For a faithful extraction of the modulated signal envelope, the time constant should satisfy the following inequality [16].

$$\frac{1}{f_c} \ll \tau \ll T_{min_{data}} \tag{1}$$

where $T_{min_{data}}$ is the shortest time interval between two binary words. This condition cannot be fulfilled for high data rate applications, as will be shown in Section III. It has also been shown that the ED can consume significant power due to high dissipated power in the diode during the conduction phase [17].

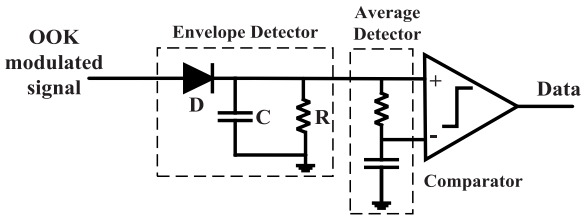

FIGURE 1. Typical block diagram of an OOK demodulator in an inductive link. It consists of an envelope detector, an average detector, and a comparator.

Our work aims to solve this limitation to achieve a high data rate downlink communications over a single inductive link intended also for power transfer. In this paper, we propose two data modulation schemes for forward data transmission based on OOK called Carrier Width Modulation (CWM) and Quad-level CWM (QCWM), together with generic-CWM and QCWM demodulators allowing for high data rates, ultra-low power consumption, and small-silicon area.

Compared to our previous works in [10], [18], [19], this paper presents the following contributions: (1) A generic CWM demodulator able to cover a wide range of carrier frequencies from 10 to 31 MHz; (2) A sensitivity analysis on the main block (PW-to-SP converter) of the proposed demodulator; (3) An improved QCWM demodulator circuit design; as well as (4) Chip fabrication and experimental validation of the generic-CWM and QCWM demodulators.

The remaining parts of this paper are organized as follows: Section II presents analytical and simulation results of an inductive link implementing the proposed CWM modulation. Section III provides the proposed design solution allowing a high-speed demodulation as well as architectural and implementation details of the generic-CWM and the QCWM demodulators. Section IV validates the functionality of the proposed demodulators and shows experimental results and performance comparisons with competitive demodulators. Finally, concluding remarks are given in Section V.

II. PROPOSED MODULATION TECHNIQUES

A. MODULATION SCHEMES

The data rate of the proposed CWM technique can be configured by selecting different modulation codes and carrier frequencies f_c. This new technique looks similar to a pulse width encoded OOK modulation [20]. However, there are two key differences. The first one concerns the modulation circuit design; as will be discussed in the next section; and the second difference is related to the modulation timing. Unlike OOK switching that can be performed at any time, CWM data switching is performed at specific times which are the zero-crossing of the primary coil current.

The modulated waveform is characterized by the carrier cycle time $T_c = (1/f_c)$, the data bit period T_d and the ON and OFF widths for '1' and '0' data bits: t_{ON_1}, t_{OFF_1}, t_{ON_0} and t_{OFF_0}. These time-widths can also be expressed using the number of carrier cycles. As shown in Fig. 2, t_{OFF_0} and t_{OFF_1} are fixed to one cycle and two cycles, respectively. OFF widths are chosen to be as short as possible to ensure a short interruption of power transmission. However, t_{ON_0} and t_{ON_1} widths take (n-1) T_c and (n-2) T_c, respectively, where n is the number of carrier cycles per data bit cycle. This number is an integer value that should be greater than or equal to 3. Three different data encoding of the proposed CWM scheme

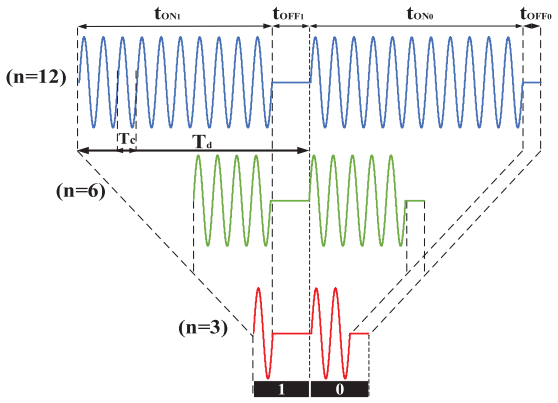

FIGURE 2. Proposed CWM scheme for different numbers of carrier cycles per data bit cycle, *n*: 12, 6 and 3 (from top to bottom).

are shown in Fig. 2 according to various selected n values (12, 6 and 3 respectively from top to bottom).

Table 1 shows the corresponding data rates ($Data\ rate = 1/T_d = f_c/n$) calculated for some n values at 13.56 MHz and 27.12 MHz carrier frequencies. These frequencies belong to the range that can penetrate water and skin without tissue heating and potential damage (3 kHz-30 MHz) [21], [22]. As shown in this table, the maximal achievable data rate is obtained for $n = 3$. This topology allows achieving a data rate as high as 9.04 Mbit/s at 27.12 MHz carrier frequency.

TABLE 1. Combinations of data rates for different *n* values.

	f_c	
	13.56 MHz	27.12 MHz
n	Data rates (Mb/s)	
100	0.1356	0.2712
50	0.2712	0.5427
6	2.26	4.52
3	4.52	9.04

For even higher data rates, we also proposed an enhanced CWM modulation scheme with quaternary symbols data encoding, called Quad-level CWM (QCWM) [18]. It consists of sending two bits per symbol by using four combinations of duty cycle ratio. One of the possible solutions consists on allocating a duty cycle ratio of 20% for the binary word '11', 40% for '10', 60% for '01', and 80% for '00', as shown in Fig. 3. In this manner, high data rates of $2/5^{th}$ of the carrier frequency can be reached. At 27.12 MHz, the binary data rate would then reach 10.84 Mbit/s, i.e. 1.8 Mbit/s higher than the CWM maximal achievable data rate.

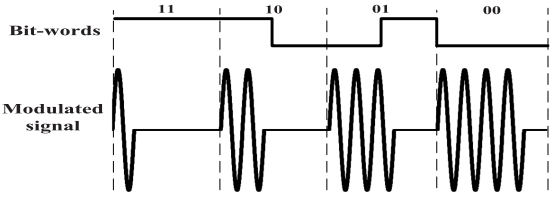

FIGURE 3. The waveforms of the proposed QCWM technique.

B. PRINCIPLE OF OPERATION

CWM and QCWM data modulations can be carried out by opening and closing the primary LC circuit using a modulation switch S_1. Figure 4 shows a simplified circuit of the proposed wireless power and downlink data transfer system. L_1 and L_2 are the self-inductances of the primary and secondary coils, respectively, with a mutual inductance M, where $M = k\sqrt{L_1 L_2}$ and k is the coupling factor between the two coils. C_1 and C_2 are capacitors used to tune the resonant frequency f_r $(= 1/2\pi\sqrt{LC})$ of the primary and secondary circuits at the carrier frequency f_c. R_1 represents the total serial loss resistance on the primary side, including the loss resistance of the voltage source v_s and the internal series resistance of the primary coil. On the other side, r_{L2} is the series loss resistance in the secondary coil and R_L is the total equivalent load of the implant. The non-linear behaviour of the rectifier load is neglected in this analysis and R_L is considered as a DC load.

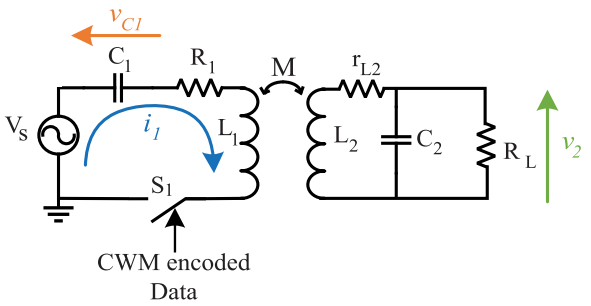

FIGURE 4. Simplified circuit of an inductive link with CWM modulation for wireless power and downlink data transfer system.

The switching of S_1 is synchronized with the zero-crossing of the current i_1 flowing into the primary coil. In other words, i_1 is instantaneously interrupted at its zero-crossing (t_0). In this manner, all the energy of the primary LC circuit is stored as voltage on the series capacitor C_1 and v_{C1} is at its extremum at the time instant t_0, as shown in Fig. 5. This principle of preserving the energy in an LC tank at switching time; to achieve high data rates with efficient power transfer over a single inductive link; is the same as the one adopted by the suspended-carrier modulation [23] and COOK [24] for forward and backward data communication, respectively. The energy preserving phenomenon was also validated by simulation in our previous paper [10].

As the OFF periods for CWM and QCWM are very short (one to four cycles), v_{C1} maintains almost this maximum voltage value until the next closing of the primary LC circuit at the time instant t_1. Virtually no energy is lost during the current interruption. Hence, the suspension and resumption of i_1 oscillation occurs without any transient responses, independently of the quality factor of the primary RLC circuit

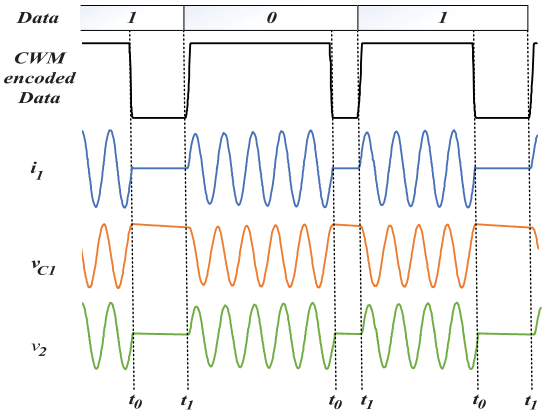

FIGURE 5. Simulated waveforms of CWM modulation scheme.

Q_1 ($= \omega L_1/R_1$, where ω is the angular operating frequency ($= 2\pi f_c$)).

At resonance, the voltage across the secondary coil v_2 and i_1 are in phase [25] and theoretically the waveform of v_2 should be similar to i_1. However, the secondary capacitor and coil discharging and charging through the resistive load R_{eq}, during the primary current interruption, may induce some unwanted transient responses in v_2 [10]. This phenomenon will be analyzed in-depth in a future work.

For this paper, ideal modulated signals are generated using an arbitrary waveform generator and only the demodulators circuits will be developed.

III. CIRCUITS IMPLEMENTATION

Typically, the proposed CWM and QCWM schemes can be demodulated using an OOK demodulator (Fig. 1) followed by an integrator circuit as used in ASK-PW demodulators [26]. The integrator is used to generate sawtooth waveforms whose amplitudes are proportional to the ON widths of the modulated signal. Figure 6 shows the simulated waveforms in

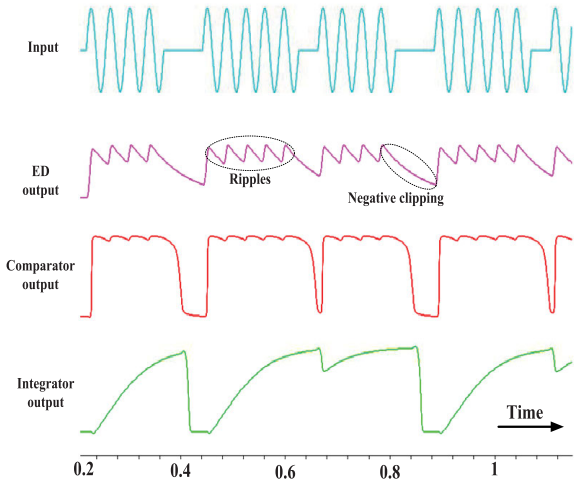

FIGURE 6. Simulated voltage waveforms (using cadence) of the front-end ASK-PWM demodulator using the CWM modulation scheme.

a typical front-end ASK-PW demodulation stages when an ideal CWM signal is used as input. Even with an optimal time constant τ, the envelope detector (ED) output voltage has high ripples and negative peak clipping. Under practical situations, this signal will be degraded to some extent due to the presence of noise and amplitude disturbances [27].

To avoid conventional ED limitations, a proposed solution consisting of a dedicated module, called a Pulse Width to Sawtooth Peak (PW-to-SP) converter, is proposed. This module produces a waveform similar to that generated by an ASK-PW front-end demodulator, but it allows a high-speed demodulation and simpler implementation.

A. PULSE WIDTH TO SAWTOOTH PEAK CONVERTER

The circuit diagram of the proposed PW-to-SP converter is shown in Fig. 7. It consists of a constant current source generating a fixed current of 2.7 μA (using a resistor and a PMOS current mirror), and a complementary pair of p-type and n-type MOSFETs that switch alternately in order to charge or discharge the capacitor C_{out} ($= 200\,fF$). To improve the linearity of the generated sawtooth signal, C_{out} is integrated by a linear metal-insulator-metal (MIM) capacitor. The charging occurs when the input signal has an amplitude lower than the gate threshold voltage, while the discharging happens in the opposite case.

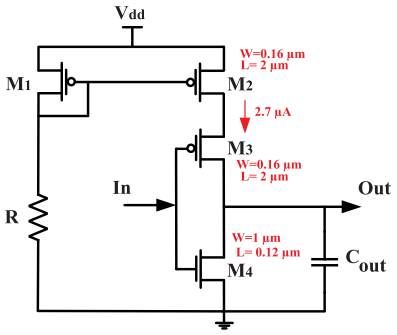

FIGURE 7. Circuit diagram of the proposed PW-to-SP converter.

The PW-to-SP converter output signal *Out* has peak amplitudes that depend mainly on the amount of charges stored into the output capacitance during OFF widths. The voltage across the output capacitor may be expressed as:

$$Out = \begin{cases} V_i(1 - e^{-t/\tau_C}) & \text{during the charging phase} \\ V_i e^{-t/\tau_D} & \text{during the discharging phase} \end{cases} \quad (2)$$

where V_i is the initial voltage across the capacitor i.e. at t=0. τ_C and τ_D are the time constants for charging and discharging C_{out}, respectively.

$$\tau_C = (R_{DS_2} + R_{DS_3})C_{out} \quad (3)$$

$$\tau_D = R_{DS_4}C_{out} \quad (4)$$

where R_{DS_2}, R_{DS_3} and R_{DS_4} are the ON-state resistances of M_2, M_3 and M_4 respectively. The aspect ratio (W/L) of these

transistors have been designed in a way to increase sufficiently τ_C while reducing τ_D as much as possible, as shown in Fig. 7.

1) SENSITIVITY TO n AND f_c

Figure 8 shows the simulated input and output signals of the PW-to-SP converter at two carrier frequencies for two different n. At a specific f_c, as the OFF-widths of the CWM signal are the same for all n from 3 to infinity, the sawtooth peak amplitudes would also be the same for all corresponding data rates. On the other hand, these peak amplitudes vary with f_c. However, the output signal keeps its sawtooth shape for a wide frequency range and the proposed PW-to-SP converter circuit is designed to operate at an f_c range from 10 MHz to 31 MHz as will be experimentally validated in Section IV.

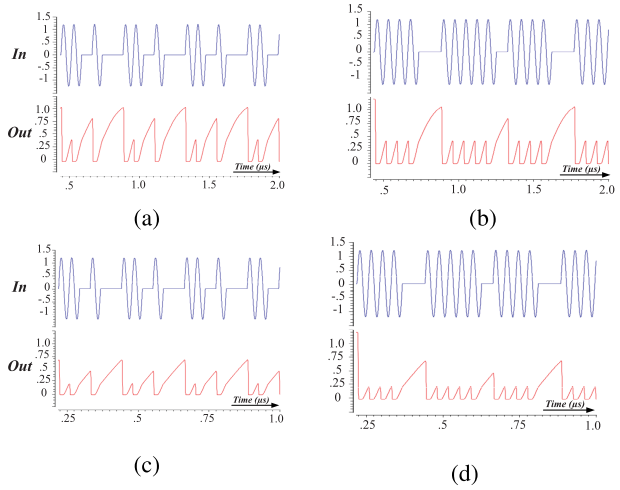

FIGURE 8. Simulated input and output signals of the PW-to-SP converter at $f_c = 13.56$ MHz for (a) $n = 3$ and (b) $n = 6$, and at 27.12 MHz for (c) $n = 3$ and (d) $n = 6$.

2) SENSITIVITY TO THE INPUT AMPLITUDE

In a typical inductive link application, the amplitude of the incoming modulated signal may vary due to noise amplitude as well as coupling or load variations. Therefore, the sensitivity of the PW-to-SP converter to input voltage amplitude variations is studied using a parametric analysis simulation. For a more realistic simulation, the ESD (Electro Static Discharge) protection circuit placed between the input/output pad and the PW-to-SP converter is also taken into consideration. A typical double-diode network is used to protect the IC from positive and negative overvoltages as shown in Fig. 9. At positive over voltage conditions, D_1 become forward-biased (D_1 conducts) and the input voltage will be clamped to $V_{dd} + V_{D_1} = 1.2V + 0.9V = 2.1V$, where V_{D_1} is the voltage drop across D_1. The 0.9V may appear high for the turn on voltage of a Si diode but it is obtained by circuit simulation of the foundry cell with its associated parameters using Cadence-Spectre. Thus, In can never exceed $2.1V$ during the positive half cycle as shown in Fig. 10(a). During negative overvoltage conditions, D_2 is forward-biased and In will be clamped to $-V_{D_2} = -0.9V$.

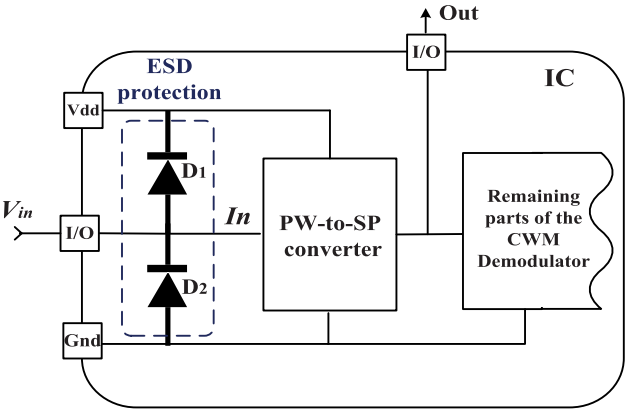

FIGURE 9. Typical double-diode ESD protection circuit. It ensure that the PW-to-SP converter input voltage never exceeds a certain level.

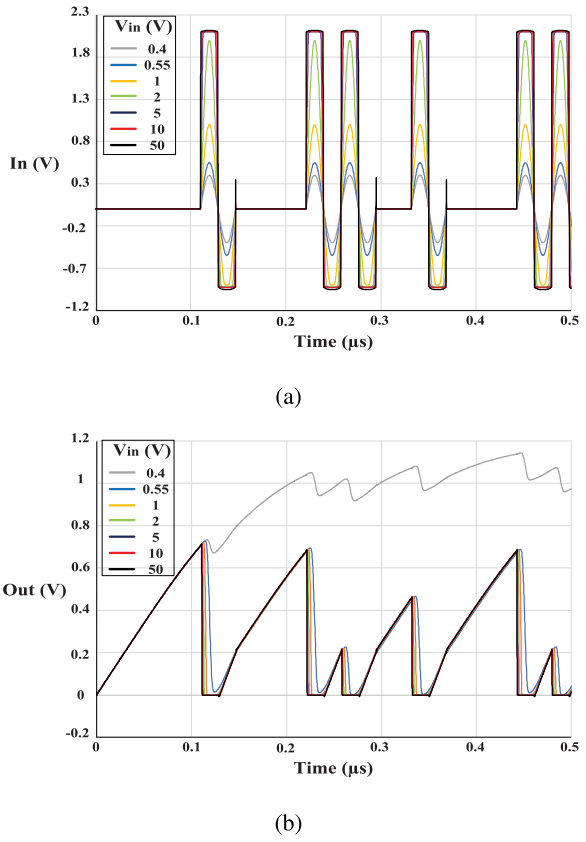

FIGURE 10. Simulated (a) input, and (b) output signals of the PW-to-SP converter for different amplitude peak to peak values of V_{in} at $f_c = 27.12$ MHz and n=3.

Figure 10(b) shows the simulation results of the output signal of the PW-to-SP converter for different amplitude levels of V_{in} when applied to the I/O pad (taken from the foundry cell library).

When the amplitude of the input signal is below the threshold voltage of M4 ($V_{th} = 430$ mV), M4 could not provide a discharge path for C_{out} (Fig. 7). Therefore, the voltage across the capacitor will accumulate as shown in Fig. 10(b). As long

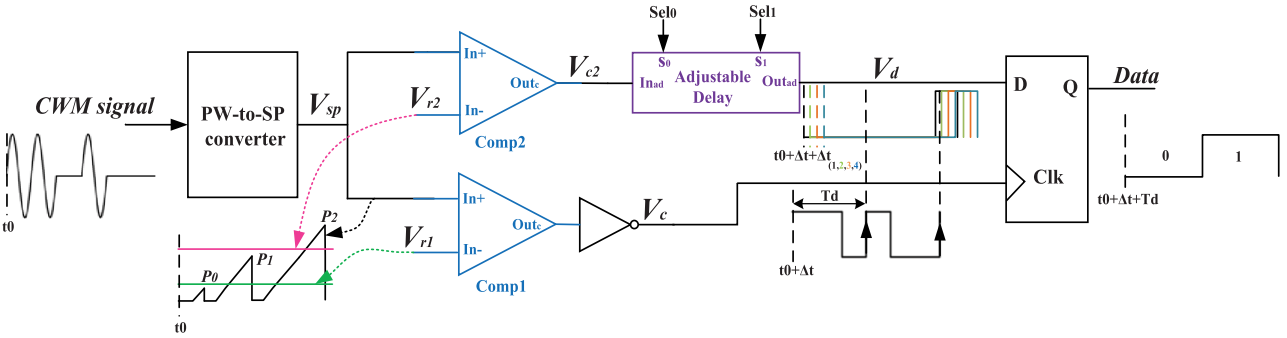

FIGURE 11. Block diagram and associated waveforms of the proposed CWM demodulator.

as V_{in} is sufficiently larger than V_{th}, the PW-to-SP converter provides almost the same peak levels. ESD protection is designed to withstand very high voltage surges up to few KVs. Accordingly, as the signal recovered in the secondary coil v_2 does not exceed a few tens of volts, the proposed design associated with the ESD protection provides a high immunity against amplitude variations.

Also, the simulated results confirmed that the proposed PW-to-SP converter achieves an ultra low power consumption of 4.8 μW and occupies a small silicon area of 486 μm^2.

B. CWM DEMODULATOR

The proposed PW-to-SP converter is the main and the first block of the CWM demodulator. Its analog output voltage V_{sp} is translated into two digital bit-streams by level detectors using two comparators and two voltage reference levels. The first bit-stream V_c, used for synchronization purposes, corresponds to the envelope of the modulated signal. It is generated from the comparison between V_{sp} and the voltage level V_{r1} followed by a digital inversion. As shown in Fig. 11, V_{r1} should be lower than the two sawtooth peaks (P_1 and P_2) but higher than P_0. On the other hand, the second bit-stream V_{c2} is recovered from the comparison between V_{sp} and another voltage level V_{r2} situated between P_1 and P_2 in order to distinguish between data bits '1' and '0'. The circuit diagram of the comparator is shown in Fig. 12(a). In this version of our proposed demodulator, the voltage levels are applied from outside the chip and are adjusted according to the carrier frequency used.

Fig. 13 shows the ranges of V_{r1} and V_{r2} for different carrier frequencies where the proposed demodulator is functional. While decreasing the carrier frequency, the gaps between the peaks P_0, P_1 and P_2 increase and the operating range of the voltage references widens. However, this is not the case for 10 MHz compared to 13.56 MHz because at 10 MHz, the duration of t_{OFF_1} is too long, so that the peak P_2 saturates at the supply voltage 1.2 V and the gap between it and P_1 is reduced.

Afterwards, an adjustable delay, shown in Fig. 12(b), is used to synchronize the V_{c2} bit-stream with the rising-edge of the delayed V_c. It integrates four delay elements and one

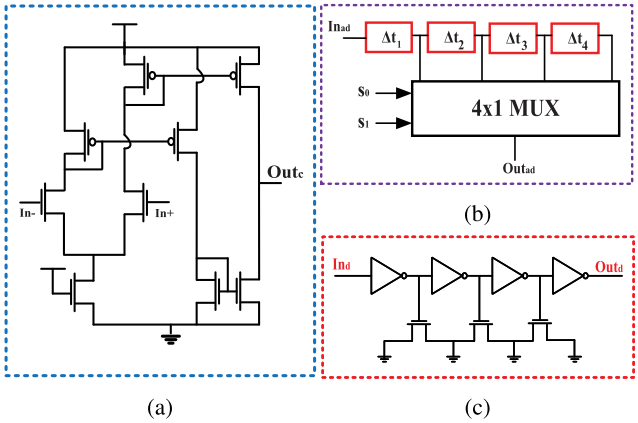

FIGURE 12. Schematics of the (a) comparator, (b) block diagram of the adjustable delay, and (c) the delay circuit.

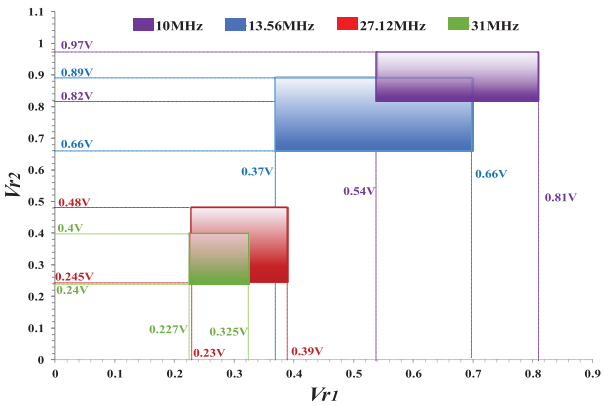

FIGURE 13. Ranges of V_{r1} and V_{r2} for different carrier frequencies at which the proposed system is functional.

4:1 multiplexer (MUX) to select the appropriate delay for synchronization. The delay circuit is constructed using a number of inverter stages loaded by capacitors implemented by NMOS transistors, as shown in Fig. 12(c).

Depending on the state of the selection signals (Sel_0 and Sel_1), the resulting delay can be $\sum_{i=1}^{m} \Delta t_i$, where $m \in \{1, 2, 3, 4\}$. This adjustment mechanism was implemented

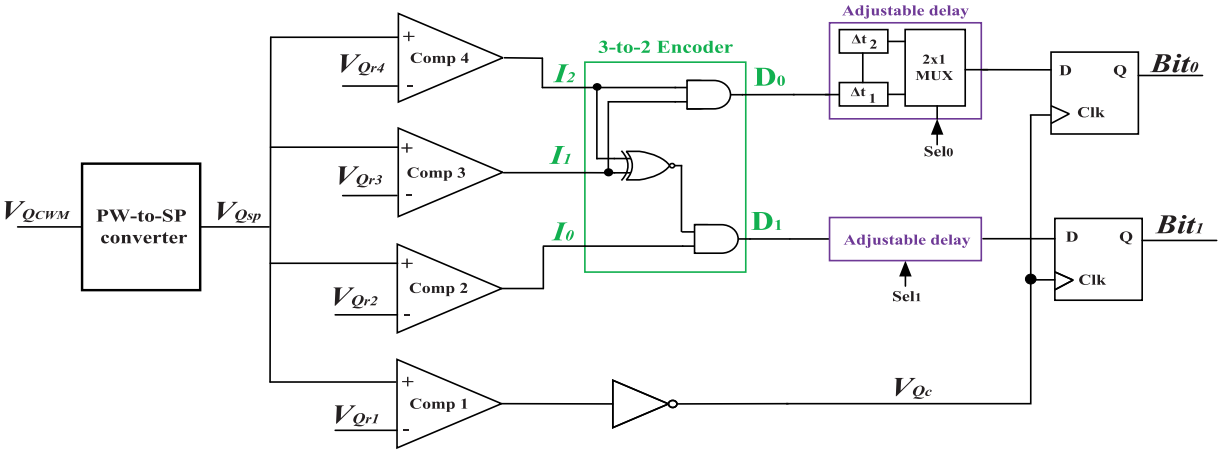

FIGURE 14. Block diagram of the QCWM demodulator.

only to have more control for calibration after chip fabrication. In the experimental results reported in the next section, we used only one delay element ($\Delta t_1 = 10$ ns).

C. QCWM DEMODULATOR

Figure 14 shows the block diagram of the QCWM demodulator operating at 27.12 MHz carrier frequency. Like the CWM demodulator, it is based on the proposed PW-to-SP converter. However, the sawtooth signal V_{Qsp} is applied to four comparators (instead of two in CWM demodulator) to be compared with four different voltage references. The comparator Comp1 followed by an inverter are used to retrieve the envelope of the modulated signal V_{QCWM}, and applied to the sequential logic circuit as a clock signal. The three other comparators act as a two-bit flash for simultaneous analogue-to-digital conversion (ADC) producing 4 output states, as shown in Table 2. Digital outputs resulting from the comparison of the analogue signal with three voltage levels are then encoded into 2 bits using a 3-to-2 logic encoder. According to the truth table (Table 2), only one XNOR gate and two AND gates are used to produce outputs D_0 and D_1, where $D_0 = I_1$ AND I_2 and $D_1 = I_0$ AND (I_1 XNOR I_2). Conforming to the same principle of CWM demodulator, delay cells and D flip-flop elements are used for synchronization and data recovery purposes.

TABLE 2. Truth table of the encoder.

State	I_0	I_1	I_2	D_0	D_1
$V_{Q_{sp}} > V_{Q_{r2}}, V_{Q_{r3}}$ and $V_{Q_{r4}}$	1	1	1	1	1
$V_{Q_{sp}} > V_{Q_{r2}}$ and $V_{Q_{r3}}$	1	1	0	1	0
$V_{Q_{sp}} > V_{Q_{r2}}$	1	0	0	0	1
$V_{Q_{sp}} < V_{Q_{r2}}$	0	0	0	0	0

Compared to a CWM demodulator, two comparators, one encoder, and one flip-flop element have been added in order to provide a 10.84 Mbit/s data rate (1.8 Mbit/s higher than that provided by CWM) at 27.12 MHz. The selection of the best modulation scheme between CWM and QCWM depends on the application requirements.

IV. EXPERIMENTAL RESULTS

Standalone CWM and QCWM demodulators were fabricated and tested to prove the concept. Figure 15 shows the chip micrograph and the layout view of the fabricated demodulators in 0.13-μm CMOS process. CWM and QCWM demodulators occupy small active areas of 2137,5 μm^2 and 3256 μm^2, respectively.

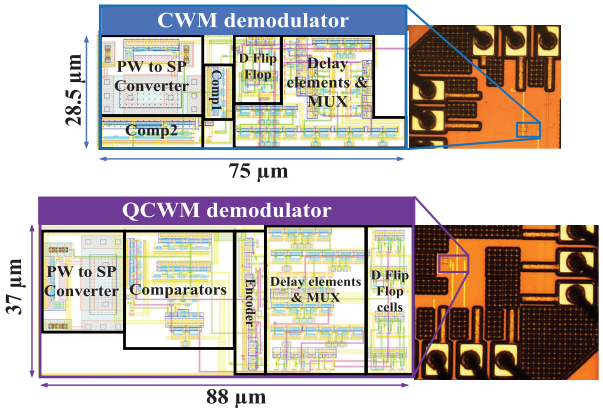

FIGURE 15. Chip micrograph and layout view of the proposed CWM and QCWM demodulators.

In order to experimentally validate the functionality of our CWM demodulator with a wide frequency range, a Keysight Benchlink waveform builder software and 33622A Function/Arbitrary Waveform Generator were adopted to produce the modulated signals. Also, power supplies are used to power the demodulators and to generate the different reference voltages.

Figure 16 shows the measured voltage waveforms for repeated '0'-'1' pattern sequence using a CWM signal with four combinations of f_c and n. The applied CWM signals have been perfectly demodulated, however the reference voltage

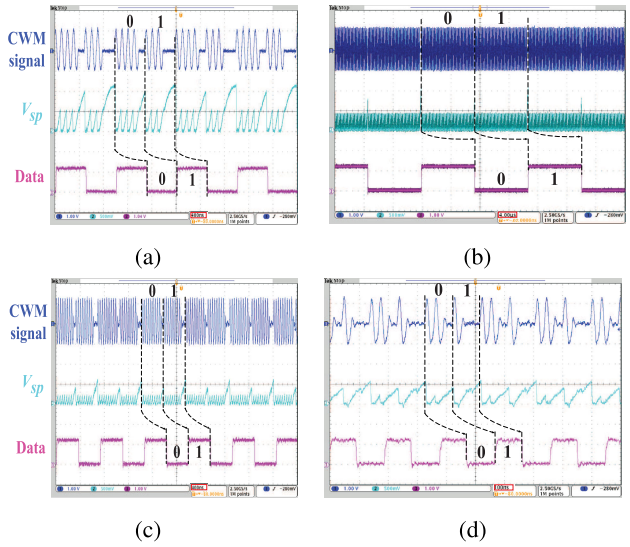

FIGURE 16. Measurement waveforms results of the proposed CWM demodulator for (a) $f_c = 10$ MHz at n=5, (b) $f_c = 13.65$ MHz at n=100, (c) $f_c = 27.12$ MHz at n=10, and (d) $f_c = 31$ MHz at n=3.

levels V_{r1} and V_{r2} had to be adjusted according to the used carrier frequency f_c (Fig. 13). Hence, practically, for a given application, V_{r1} and V_{r2} should be fixed from the beginning according to the application frequency.

Also, in order to confirm the genericity of our proposed CWM demodulator, the functionality of this demodulator under different f_c versus n is experimented as shown in Fig. 17 using a shmoo plot. The Pass/Fail criteria is defined by the reliability of the output data displayed on the oscilloscope during 40 ms.

f_c (MHz) \ n	100	10	5	4	3
9			Fail		
10					
13.56					
27.12			Pass		
31					
32			Fail		

FIGURE 17. Shmoo plot for carrier frequencies f_c versus the number of carrier cycles per data bit cycle n.

The functionality of the proposed CWM demodulator is validated for a frequency band limited by a lower frequency of 10 MHz and an upper frequency of 31 MHz. Beyond these values, the distinction between the two sawtooth peak amplitudes (P_1 and P_2) becomes harder and output errors appear.

Figure 18 plots the measured power consumption of the CWM demodulator at different carrier frequencies and data rates. For a specific carrier frequency, the power consumption increases with data rates due to the increase of the energy dissipation in comparators since the mean energy of their non-inverting inputs signals (V_{sp}) increases with data

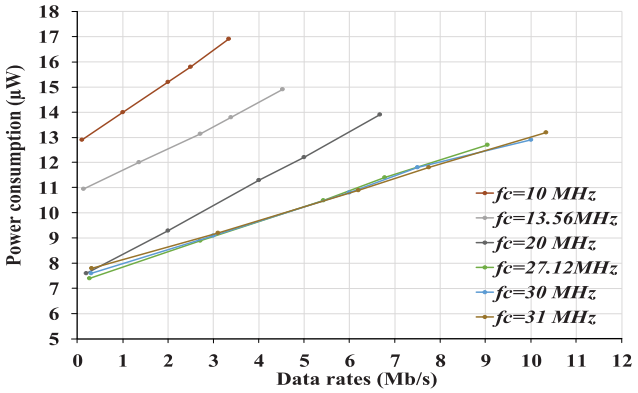

FIGURE 18. Measured power consumption versus data rates for different carrier frequencies.

rates. For the same reason, the power consumption increases when decreasing the carrier frequency. At lower frequencies, the sawtooth peaks P_1 and P_2 are high, which also requires higher voltage reference levels to be introduced on inverting inputs of the comparators. However, switching losses in PW-to-SP converter are increasingly significant at higher frequencies. This explains for example why the power consumption at 27.12 MHz, 30 MHz and 31 MHz, are close to each other.

The functionality of our proposed QCWM demodulator is also confirmed by experimental measurements using the same setup. In this test-bench, voltage references are applied from outside the chip, generated using resistive voltage dividers and a 1.2 V supply. Figure 19 shows the measurement results of the QCWM demodulator for repeated '11'-'10'-'01'-'00' pattern sequence of QCWM modulated signal. This demodulator achieves an ultra-low power of 35.5 μW at a data rate of 10.848 Mb/s corresponding to 3.27 pJ/bit.

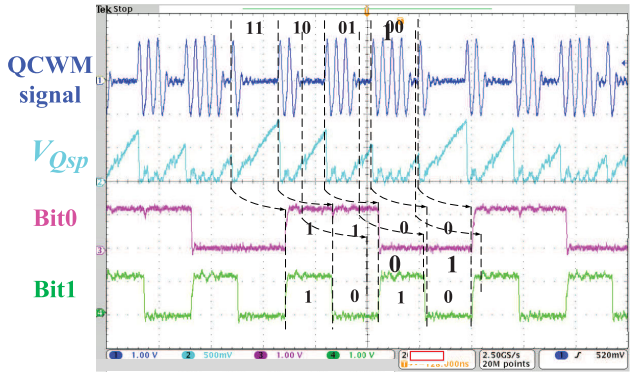

FIGURE 19. Measured waveforms of the proposed QCWM demodulator. The output digital bit-streams are delayed by $\Delta t + T_d$, as is the case for the CWM modulation.

Table 3 summarizes the measured performances of the QCWM demodulator and of the generic-CWM demodulator operating within the lower and upper f_c limits for $n = 3$. The table presents also competitive state-of-the-art demodulators

TABLE 3. Measured performance of the proposed demodulators and comparison with previous works.

Simultaneous powering	No			Yes					
Reference	[28][a]	[29][b]	[30][b]	[11][b]	[12][a]	[31][a]	[32][a]	This work[a]	
Modulation scheme	ASK	ASK	PHM	DFSK	QCPSK	ASK	ASK	QCWM	CWM
Technology (μm)	0.18	0.18	0.35	1.5	0.18	0.18	0.35	**0.13**	
f_c (MHz)	13.56	5	66.6	5-10	4	13.56	6	**27.12**	**31**
Data rate (Mbit/s)	6.78	0.5	20	2.5	0.8	2	1	**10.85**	**10.3**
Power consumption (μW)	348.7	17	250	380	59	35	200	**35.5**	**13.2**
Silicon area ($10^3 \mu m^2$)	80	0.92	60	4840	5	3	2.05	**3.25**	**2.137**
E/b (pJ/bit)	51.44	34	12.5	152	73.75	17.5	200	**3.27**	**1.28**
$FOM^1 \times 10^{-2}$	0.02	3.2	0.13	0.13×10^{-3}	0.27	1.9	0.24	**9.39**	**37.3**
$FOM^2 \times 10^{-2}$	0.06	20.7	0.25	–	2.2	4.55	$\cong 0$	**5.8**	**20.3**

[a] A signal generator is adopted to produce the modulated signal.
[b] A transmitter is used to produce the modulated signal.

used in inductive forward data transmission. Modulation methods reported in this table are divided into two groups. The first group includes methods intended for simultaneous power transfer over the same inductive link (indicated with 'Yes') and the second group includes methods optimized only for data transmission ('No').

For accurate comparison, we used figures of merit defined in [28] (FOM^1), and [29] (FOM^2).

$$FOM^1 = \frac{Data\ rate\ (Mb/s)}{Power(\mu W) \times area\ (\mu m^2)} \tag{5}$$

$$FOM^2 = \frac{Data\ rate(Mb/s) \times (Process)^2\ (\mu m^2)}{f_c(MHz) \times Power(\mu W) \times area(\mu m^2)} \tag{6}$$

Table 3 shows the superior performance of the proposed data demodulation techniques which achieve the lowest energy efficiency (E/b) and highest $FOMs^1$. Also, our demodulators have high $FOMs^2$. In addition, compared to the best published demodulators, the proposed CWM circuit operates at a wide range of carrier frequency, and data rates. Even at a carrier frequency as low as 10 MHz, the proposed system provides a very good energy efficiency of 5 pj/bit. The ultra-low power consumption of the reported circuit confirms that the CWM and QCWM techniques are applicable for low power battery-fed IMDs. Moreover, due to its genericity, the proposed CWM demodulator is convenient for a wide range of applications.

V. CONCLUSION

CWM and QCWM schemes allowing high data rates to carrier frequency ratio over a single inductive link for both power and data transfer were reported in this paper. These proposed modulation techniques maintain the advantages of ASK/FSK/PSK modulations. They allow low power consumption and simple implementation of the ASK modulation, while allowing high data rates and high immunity against amplitude disturbances ensured by PSK and FSK modulations. In addition, the genericity of the CWM demodulator was confirmed by operating under a wide range of data rates. Generic-CWM and QCWM demodulators fabricated in a 0.13-μm CMOS were implemented and tested. Measurements confirmed that the generic-CWM demodulator can operate at frequencies ranging from 10 MHz to 31 MHz, while offering an ultra-low power consumption. Moreover, comparisons with related works shows that our demodulators have the best energy efficiency for downlink data transfer over an inductive link supporting both power and data transfer.

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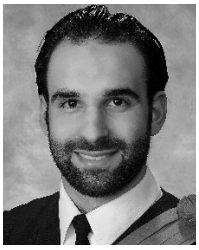

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