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Low Input Ripple High Step-Up Extendable Hybrid DC-DC Converter

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ABSTRACT The widely utilization of renewable energy with low output voltage makes the high voltage ratio boosting converter more popular. This article introduces a non-isolated low input ripple high step-up extendable hybrid DC-DC converter. The proposed converter is based on a two-phase interleaved BOOST converter and switch-capacitor (SC) boost circuit. One of the BOOST channels charges the capacitors in the SC circuit, and the other BOOST channel is connected in series with the capacitors to supply power to the load. Benefiting from this structure, the converter achieves high voltage gain, reduced semiconductor voltage stress, and low input current ripple. Moreover, the converter can be extended by increasing the number of switch-capacitor boost units or the parallel BOOST channels to perform better in voltage gain, input current ripple, and power density. The principle of operation, theoretical analysis, expansion scheme, and comparison with similar topologies are introduced in detail. Finally, a 100W prototype is implemented to verify the validity of the theoretical analysis.

INDEX TERMS High step-up, interleaved, low input ripple.

I. INTRODUCTION

The energy crisis and environmental pollution have become increasingly prominent. Renewable energy sources such as photovoltaic cells and fuel-cell stacks have begun to receive worldwide attention [1]–[6]. However, the output voltages of these energy sources are usually between 12V to 60V dc, so it is essential to use a high step-up DC-DC converter to boost these low voltage to standard dc bus voltage of 380-400V for grid-connected power generation [7]–[11].

The isolated high step-up DC-DC converters are widely used due to the simple structure and high reliability, furthermore, the voltage gain can be changed flexibly by adjusting the turns ratio of the transformer. However, the high turns ratio is ineluctable to bring about reduced efficiency and lower power density [12]–[14].

The conventional BOOST converter is popular in many step-up applications when isolation is not required. The converter has fewer components and is quite convenient in control. However, when the large boost ratio is realized, the switch duty cycle will reach a very high level, which will lead to serious reverse recovery current spike of the output diode. Furthermore, an extremely high switch duty cycle can also lead to lower efficiency and reduced reliability.

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Considering the above aspects, the coupled inductor is utilized to improve the transformation ratio. However, the leakage inductance introduced by the coupled inductor will cause large voltage spikes across the switching devices, which will lead to heavy press in the selection of components [15]. The clamp circuit is introduced to recover the leakage energy and suppress the voltage spikes, but the complexity in design, the size, and cost of the circuit increase [16], [17].

High step-up converters with SC circuits perform better in semiconductors voltage stress and power density. The capacitors in the unit are usually charged by the inductor or the input source in one stage and discharge at the output stage, therefore, the voltage conversion ratio can be improved markedly [18]. The opposite principle can be utilized in step-down applications, such as the BUCK converter with series capacitor can achieve ultrahigh step-down conversion ratio [19], [20]. In [21], an SC-based dual-switch converter with only one inductor is presented. High voltage gain is achieved but the voltage stress of the output diode is really high, and the input current ripple is quite large.

The interleaved structure is employed in [22]. The circuit is quite simple, but the voltage gain is not ample in some step-up applications and one of the diodes suffers from high voltage stress which is equal to the output voltage. In [23], a single-stage boost converter topology based on SC circuits is proposed. The converter operates on the basis of

parallel-charging-series-discharging principle which can be helpful in voltage boost. It inherits the merits of BOOST converter, and the voltage stress of the semiconductors and the input current ripple are decreased effectively. However, the voltage gain, which is only two times greater than that of conventional BOOST converter, is still not sufficient in some applications, which means extreme duty cycle may not be avoided when a relatively high voltage gain is required. In [24], a three-phase high step-up converter is proposed. The voltage gain of this converter is higher than that of [23], but the three inductors lead to a larger volume of converter and the three MOSFETs bring difficulties for design.

Circuit expansion scheme which can improve the boost ratio is proposed in [25]. Theoretically, the voltage gain of this converter can be improved boundlessly by increasing the number of SC circuits when the duty cycle is fixed. The expansion scheme will make the converter suitable for more applications. However, the input current ripple of the converter is quite large, which may pose a threat to the life of new energy sources such as solar cells and fuel cells.

In this paper, an interleaved switch-capacitor-based high step-up extendable hybrid DC-DC converter is presented. The proposed converter inherits the advantages of high voltage gain, low switches voltage stress and reduced input current ripple. Meanwhile, the converter can be extended by increasing the number of parallel channels or the SC units to further reduce input current ripple, increase voltage gain and power density.

II. WORKING PRINCIPLE

The proposed topology is shown in Fig. 1. The inductor L_1, the switch S_1, the diodes D_1, D_2 and the capacitors C_1, C_2 constitute a single-input-double-output BOOST converter. The inductor L_2, the switch S_2, the diode D_3, and the capacitor C_o constitute another BOOST converter. The two BOOST converters form a modified interleaved parallel BOOST converter with quite high voltage gain and low input current ripple.

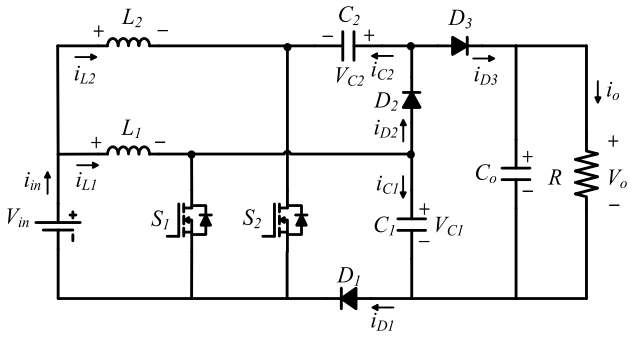

FIGURE 1. The proposed topology.

To simplify the analysis, the following assumptions are made.

1) The proposed circuit works under continuous conduction mode (CCM), and $L_1 = L_2 = L$.

2) Capacitors C_1, C_2 and C_o are large enough to keep the capacitors voltage constant.

3) All components are ideal. It means that there is no turn-ON resistance, stray capacitance, and threshold voltage.

The main working waveforms of the converter are shown in Fig. 2. The duty cycles of the switches S_1, S_2 are D_{s1}, D_{s2}, which are greater than 0.5 and interleaved with a 180° phase shift. The converter has four operating modes, as shown in Fig. 3.

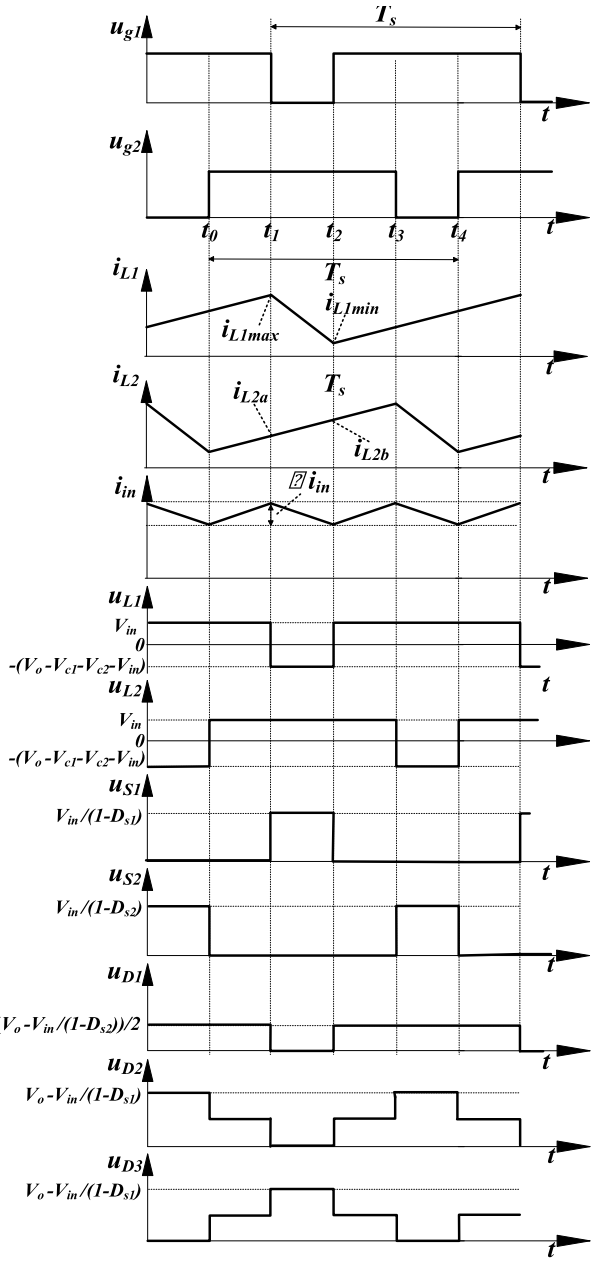

FIGURE 2. Main waveforms of the proposed converter.

1) Mode 1[t_0-t_1] : As shown in Fig. 3(a), at $t = t_0$, the switches S_1 and S_2 are both turned on. The inductors L_1 and L_2 are linearly charged by the input source V_{in}. Capacitor C_o supplies power to the load.

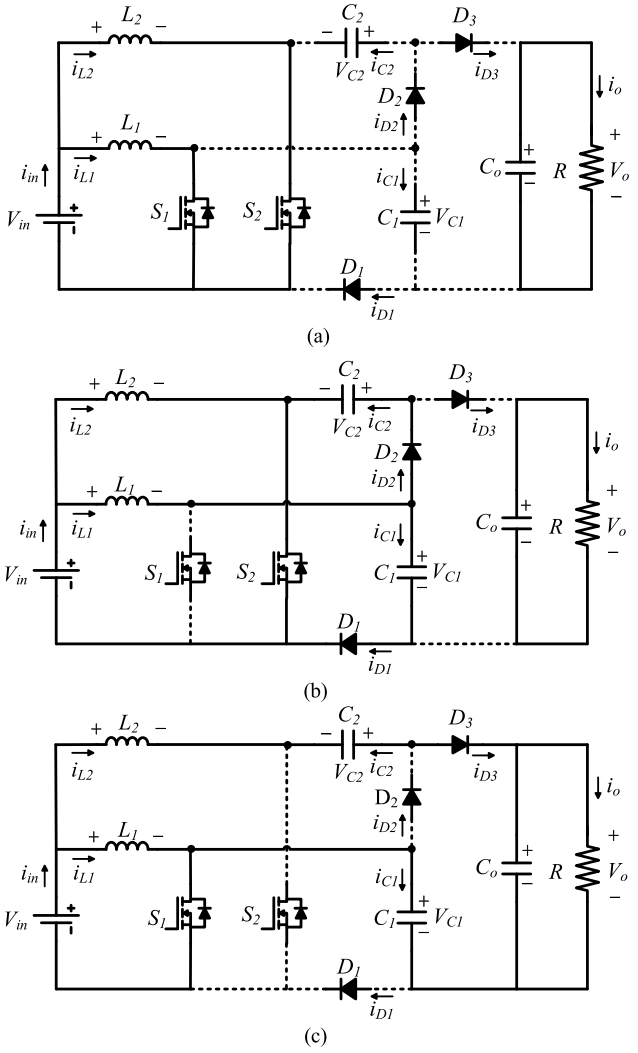

FIGURE 3. The equivalent circuits of different working modes.

2) Mode 2 $[t_1 - t_2]$: As shown in Fig. 3(b), at $t = t_1$, switch S_1 is turned off and S_2 is turned on. The inductor L_1 releases energy to C_1, C_2, and the current of L_1 decreases linearly. At this time, there are two current paths: 1) inductor current through the D_2, S_2 to charge capacitor C_2. 2) inductor current charges capacitor C_1 via D_1. Inductor L_2 is charged by the input source V_{in}, and the inductor current continues to rise linearly. Capacitor C_{o} supplies power to the load.

3) Mode 3 $[t_2 - t_3]$: As shown in Fig. 3(a), this mode is the same as mode 1.

4) Mode 4 $[t_3 - t_4]$: As shown in Fig. 3(c), at $t = t_3$, switch S_2 is turned off and S_1 continues to conduct. At the same time, L_2 is connected in series with V_{in}, C_1, C_2 to supply power to the load vias S_1 and D_3. The voltage across L_1 is V_{in}, and the current of inductor L_1 continues to rise linearly.

III. PERFORMANCE ANALYSIS

A. VOLTAGE GAIN

The voltage gain of the topology can be obtained based on the analysis of the above working modes.

The voltage across capacitors C_1, C_2 can be obtained as

$$V_{c1} = V_{c2} = \frac{1}{1 - D_{s1}} V_{in} \tag{1}$$

The following equation can be written from the volt-second balance principle on inductor L_2

$$\int_0^{D_{s2}T_s} V_{in} dt = \int_{D_{s2}T_s}^{T_s} (V_o - V_{c1} - V_{c2} - V_{in})\, dt \tag{2}$$

From (1) and (2), the output voltage can be obtained as

$$V_o = \frac{2V_{in}}{1 - D_{s1}} + \frac{V_{in}}{1 - D_{s2}} \tag{3}$$

When the duty ratio $D_{\text{s1}} = D_{\text{s2}} = D$, the voltage gain can be expressed as

$$M_v = \frac{3}{1 - D} \tag{4}$$

B. SWITCHING DEVICES VOLTAGE STRESS

According to the aforementioned analysis, the voltage stress across the semiconductors can be figured out. The voltage stress of the two switches can be calculated by

$$\begin{aligned} V_{s1\_\max} &= \frac{1}{1 - D_{s1}} V_{in} = \frac{V_o - \frac{1}{1 - D_{s2}} V_{in}}{2} \\ V_{s2\_\max} &= \frac{1}{1 - D_{s2}} V_{in} = V_o - \frac{2}{1 - D_{s1}} V_{in} \end{aligned} \tag{5}$$

The voltage stress of the three diodes can be calculated by

$$\begin{aligned} V_{D1\_\max} &= \frac{V_o - \frac{1}{1 - D_{s2}} V_{in}}{2} \\ V_{D2\_\max} &= V_{D3\_\max} = V_o - \frac{1}{1 - D_{s1}} V_{in} \end{aligned} \tag{6}$$

We can see from (5) that the voltage stress of the two switches reaches the minimum level when $D_{\text{s1}} = D_{\text{s2}}$. Therefore, $D_{\text{s1}} = D_{\text{s2}}$ is selected for analysis. The voltage stress of all the semiconductors can be calculated by

$$\begin{aligned} V_{s1\_\max} &= V_{s2\_\max} = \frac{V_o}{3} \\ V_{D1\_\max} &= \frac{V_o}{3} \\ V_{D2\_\max} &= V_{D3\_\max} = \frac{2V_o}{3} \end{aligned} \tag{7}$$

C. INPUT CURRENT RIPPLE

From Fig. 2, i_{L1max} and i_{L1min} are the maximum and minimum values of the inductor L_1 current, and i_{L2a} and i_{L2b} are the current of L_2 when the current of L_1 reaches the maximum and minimum values, respectively. Δi_{in} is the input current ripple. The following equations can be obtained

$$\begin{cases} i_{L1\,\max} - i_{L1\,\min} = \dfrac{U_{in}}{L} D T_S \\ i_{L2b} - i_{L2a} = \dfrac{U_{in}}{L} (1 - D) T_S \end{cases} \tag{8}$$

The input current ripple can be expressed as

$$\begin{aligned}\Delta i_{\text{in}} &= (i_{L1\max} + i_{L2a}) - (i_{L1\min} + i_{L2b}) \\ &= \frac{V_{in}T_S}{L}(2D-1) \\ &= \frac{V_oT_S}{L}\frac{(2D-1)(1-D)}{3}\end{aligned} \tag{9}$$

The curve of the input current ripple is shown in Fig. 4, where $L_1 = L_2 = 600$ uH, $V_{\text{o}} = 380$ V and $f_{\text{s}} = 100$ kHz. Within a given input voltage range, the input current ripple increases first and then decreases as the input voltage increases, and it reaches the maximum value when $V_{\text{in}} = 31.67$ V which can be calculated according to (9).

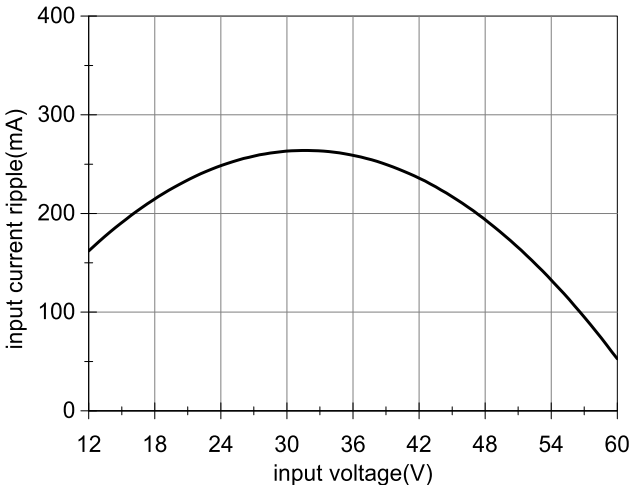

FIGURE 4. The input current ripple.

The relationship between the duty cycle of the two converters can be expressed as (10) when the input voltage and output voltage are in the same condition and the inductor current is continuous.

$$D = 3D_{\text{B}} - 2 \tag{10}$$

where D_{B} is the duty cycle of the conventional BOOST converter.

The reduction of the input current ripple of the proposed converter can be calculated as (11) when compared to the conventional BOOST converter.

$$\begin{aligned}\Delta i_{\text{B}} - \Delta i_{\text{in}} &= \frac{V_{in}T_S}{L}D_{\text{B}} - \frac{V_{in}T_S}{L}(2D-1) \\ &= \frac{V_{in}T_S}{L}D_{\text{B}} - \frac{V_{in}T_S}{L}(6D_{\text{B}}-5) \\ &= \frac{V_{in}T_S}{L}(5-5D_{\text{B}})\end{aligned} \tag{11}$$

where Δi_{B} is the input current ripple of the conventional BOOST converter

D. DESIGN CONSIDERATION OF MAIN COMPONENTS

The design example is given with the following specifications.

1) input voltage $V_{\text{in}} = 48$ V;
2) output voltage $V_{\text{o}} = 380$ V;
3) maximum output power $P_{\text{o}} = 100$ W;
4) switching frequency $f_{\text{S}} = 100$ kHz.

From the aforementioned analysis and the power balance principle, I_{in}, I_{L1}, and I_{L2} can be easily derived as

$$\begin{cases} I_{in} = \dfrac{3}{1-D}I_o \\ I_{L1} = 2I_{L2} = \dfrac{2}{1-D}I_o \end{cases} \tag{12}$$

where I_{in} is the average input current, I_{o} is the average output current, and I_{L1} and I_{L2} are the average currents of the two inductors, respectively.

We can see from (12) that I_{L1} is two times higher than I_{L2}, so the converter operates under CCM when the current of L_2 is continuous. The following equation can be obtained

$$L_2 = L_1 = \frac{DV_{in}T_s}{\Delta i_{L2}} \tag{13}$$

The capacitors C_1, C_2, and C_{o} can be calculated by

$$\begin{cases} C_1 = \dfrac{(1-D)I_{L1}}{2f_s\Delta V_{C1}} \\ C_2 = \dfrac{(1-D)I_{L2}}{f_s\Delta V_{C2}} \\ C_o = \dfrac{(1-D)I_o}{f_s\Delta V_o} \end{cases} \tag{14}$$

where ΔV_{C1}, ΔV_{C2}, and ΔV_{CO} are the maximum tolerant voltage ripple on the capacitors C_1, C_2, and C_{o}, respectively.

In order to design for operation in CCM and the input current ripple is assumed as 10% of I_{in}, the inductor L_1 and L_2 are equal to 558 uH. When ΔV_{C1}, ΔV_{C2}, and ΔV_{CO} are assumed as 1% of V_{C1}, V_{C2} and V_{o}, the capacitors C_1 and C_2 are equal to 2.08 uF and the capacitor C_{o} is equal to 0.26 uF. In the practical circuit, the inductor L_1 and L_2 are designed as 600 uH, and the capacitors C_1 and C_2 are designed as 2.2 uF. Actually, the capacitance of C_{o} should be much larger than the calculated value to reduce power loss, and C_{o} is designed as 47 uF in this paper.

The voltage rating of the semiconductors has been derived from (5)-(7). In practice, voltage spike may be caused by the parasitic capacitor and inductance, so enough safety margin should be considered.

IV. TOPOLOGY EXTENSION

The proposed converter can be extended on the output side and the input side, which can further improve the voltage gain and reduce the input current ripple.

A. OUTPUT SIDE EXPANSION

The expansion scheme on the output side is shown in Fig. 5, where N is the number of the expansion units.

The voltages of the two capacitors in the Nth expansion unit can be derived as

$$V_{c(2N+1)} = V_{c(2N+2)} = \frac{2V_{in}}{1-D} \tag{15}$$

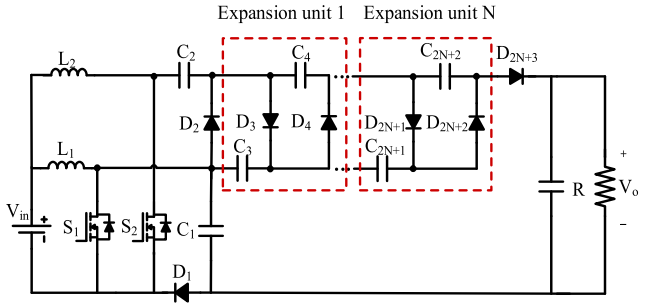

FIGURE 5. The circuit with output side expansion.

The following equation can be deduced according to the volt-second balance principle on inductor L_2

$$\int_0^{DT_s} V_{in}dt = \int_{DT_s}^{T_s} (V_o - V_{c1} - V_{c2} - V_{in} - \sum_{i=1}^{N} V_{c(2i+2)})dt \quad (i = 1, 2 \ldots n, n \geq 1) \tag{16}$$

The voltage gain can be derived as

$$M_v = \frac{(2N+3)}{1-D} = \frac{3}{1-D} + \frac{2N}{1-D} \tag{17}$$

The duty cycle of each switch can be expressed as

$$D_N = 1 - \frac{(2N+3)V_{in}}{V_o} \tag{18}$$

Under the same input voltage and output voltage, the input current ripple variation for each additional expansion unit is

$$\Delta i_{\text{in\_}N+1} - \Delta i_{\text{in\_}N} = \frac{V_{in}T_S}{L}(2D_{N+1} - 1) - \frac{V_{in}T_S}{L}(2D_N - 1) = -\frac{4V_{in}^2 T_S}{LV_o} \tag{19}$$

where $\Delta i_{\text{in\_N}}$ is the input current ripple of the circuit with N expansion units.

We can see that the input current ripple decreases as the number of expansion units increases.

B. INPUT SIDE EXPANSION

The expansion scheme on the input side is shown in Fig. 6, where M is the number of parallel channels. The input current ripple can be further reduced and the voltage gain can be improved simultaneously when M is increasing. Also, it is required that the driving signals of all the switches are interleaved with $(360 / M)°$ phase shift.

The voltage of the capacitor in the Mth parallel channel can be derived as

$$V_{c(M+2)} = \frac{(M+1)V_{in}}{1-D} \tag{20}$$

The following equation can be deduced according to the volt-second balance principle on inductor L_{M+2}

$$\int_0^{DT_s} V_{in}dt = \int_{DT_s}^{T_s} (V_o - V_{in} - V_{c1} - V_{c(M+2)})dt \tag{21}$$

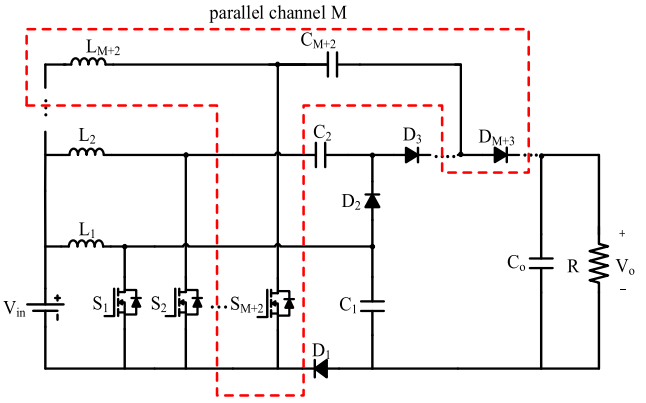

FIGURE 6. The circuit with input side expansion.

The voltage gain can be expressed as

$$M_v = \frac{(M+3)}{1-D} \tag{22}$$

Fig. 7 shows the comparison of the voltage gain between the proposed topologies and some similar converters. We can see that the voltage gain of the proposed converter is higher than that of similar converters. The voltage gain of the circuit with input-side-extension or output-side-extension is higher than that of the pre-extended circuit. And the circuit with output-side-extension has the highest voltage gain among all the compared circuits.

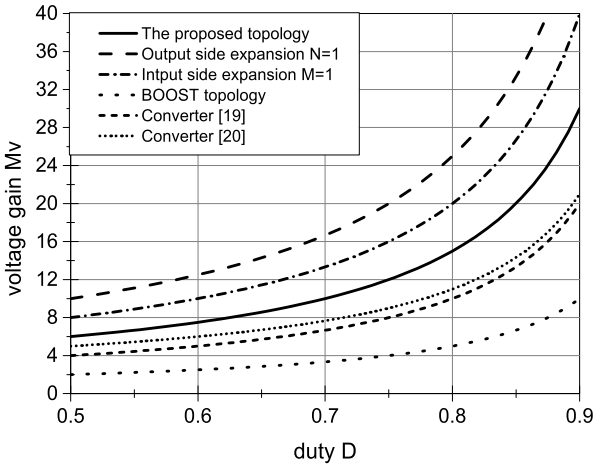

FIGURE 7. Voltage gains of proposed topology and BOOST topology.

The current waveforms of each inductor are shown in Fig. 8, where $i_{\text{L(M+2)a}}$ and $i_{\text{L(M+2)b}}$ are the current of the inductor $L_{(\text{M+2})}$ when the inductor L_1 reaches the maximum and minimum values respectively.

The following equations can be obtained

$$\begin{cases} i_{L1\,\max} - i_{L1\,\min} = \dfrac{V_{in}}{L}DT_S \\ i_{L2b} - i_{L2a} = \dfrac{V_{in}}{L}(1-D)T_S \\ \ldots \\ i_{L(M+2)b} - i_{L(M+2)a} = \dfrac{V_{in}}{L}(1-D)T_S \end{cases} \tag{23}$$

TABLE 1. Characteristics of similar converters.

Converters	Conventer[7] (n=1)	Converter[23]	Converter[25]	Proposed converter	Proposed converter with input expansion(M=1)	Proposed converter with output expansion(N=1)
Voltage gain	$\frac{1}{D(1-D)}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$	$\frac{3}{1-D}$	$\frac{4}{1-D}$	$\frac{5}{1-D}$
Max voltage stress on swithes	V_o	$V_o/2$	$\frac{V_o}{3-D}$	$V_o/3$	$V_o/4$	$V_o/5$
Max voltage stress on diodes	V_o	$V_o/2$	$\frac{V_o}{3-D}$	$2V_o/3$	$V_o/2$	$2V_o/5$
Input current ripple	$\frac{D^2(1-D)T_sU_o}{L}$	$\frac{(2D-1)(1-D)T_sU_o}{2L}$	$> \frac{D(1-D)T_sU_o}{(3-D)L}$	$\frac{(2D-1)(1-D)T_sU_o}{3L}$	$\frac{(3D-2)(1-D)T_sU_o}{4L}$	$\frac{(2D-1)(1-D)T_sU_o}{5L}$
Quantities of capacitors	2	3	4	3	4	5
Quantities of swithes	2	2	1	2	3	2
Quantities of diodes	2	3	4	3	4	5

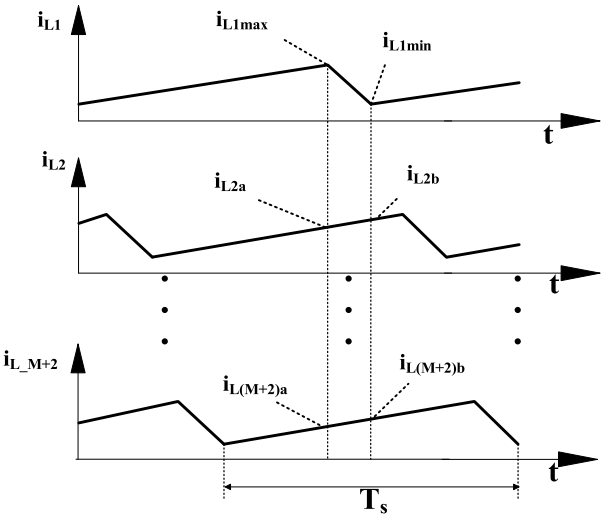

FIGURE 8. The inductors current waveforms.

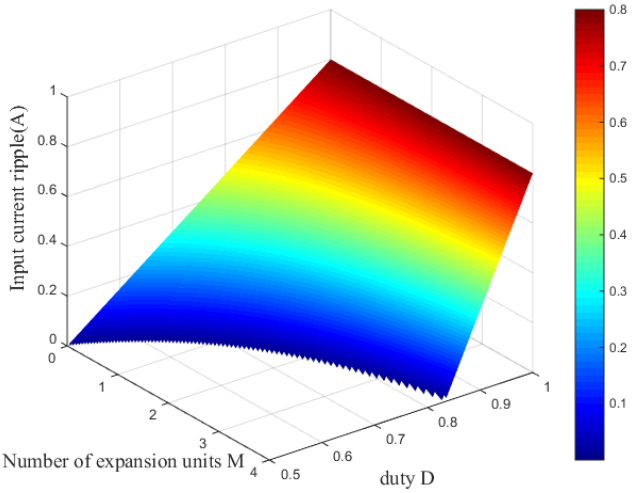

FIGURE 9. The current ripple of the circuit with input side expansion.

The input current ripple can be expressed as

$$\begin{aligned}\Delta i_{\text{in}} &= (i_{L1\max} + i_{L2a} + \cdots + i_{L(M+2)a}) \\ &\quad -(i_{L1\min} + i_{L2b} + \cdots + i_{L(M+2)b}) \\ &= \frac{V_{in}T_S}{L}[D-(M+1)(1-D)] \end{aligned} \tag{24}$$

The relationship between Δi_{in}, D and M is shown in Fig. 9, where $L_1 = L_2 = 600$ uH, $f_s = 100$ kHz and $V_{\text{in}} = 48$ V. From (24) and Fig. 9 we can see that the input current ripple decreases when the duty cycle decreases. The more parallel channels can also help to reduce the input current ripple, and the input current ripple decreases to zero when $D = (M+1)/(M+2)$.

The duty cycle of each switch can be deduced as

$$D_M = 1 - \frac{(M+3)V_{in}}{V_o} \tag{25}$$

Under the same input voltage and output voltage, the input current ripple variation for each additional parallel channel is

$$\begin{aligned}\Delta i_{\text{in\_}M+1} - \Delta i_{\text{in\_}M} &= \frac{V_{in}T_S}{L}[D_{M+1} - (M+2)(1-D_{M+1})] \\ &\quad -\frac{V_{in}T_S}{L}[D_M - (M+1)(1-D_M)] \\ &= -\frac{V_{in}^2T_S}{LV_o}(2M+6) \end{aligned} \tag{26}$$

where $\Delta i_{\text{in\_M}}$ is the input current ripple of the circuit with M parallel channels.

We can see that the input current ripple of the converter is further reduced as the number of parallel channels increases.

From the ampere-second balance on capacitors, the following equation can be obtained

$$\frac{1}{2}(1-D)I_{L1}T_s = (1-D)I_{L2}T_s = \ldots = (1-D)I_{LM}T_s \tag{27}$$

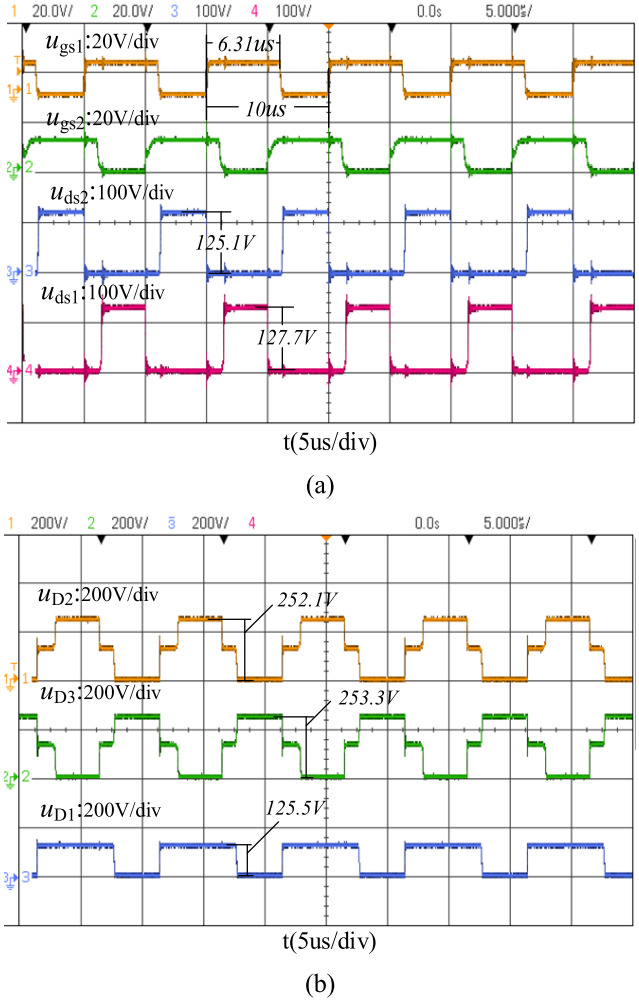

FIGURE 10. Experimental waveforms of switching devices.

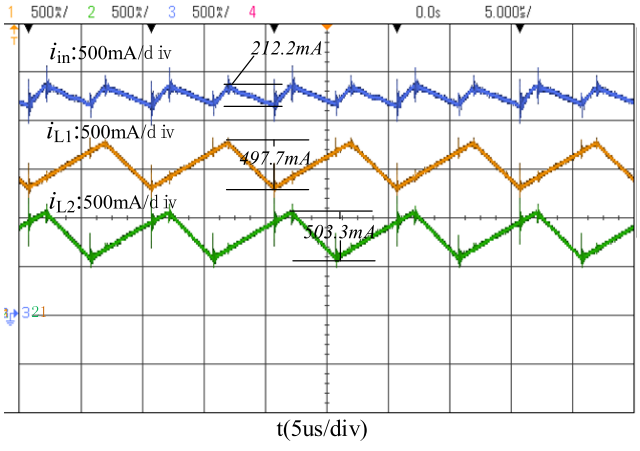

FIGURE 11. Waveforms of currents.

The relationship between different inductors currents can be expressed as

$$I_{L1} = 2I_{L2} = 2I_{L3} = \ldots = 2I_{LM} \tag{28}$$

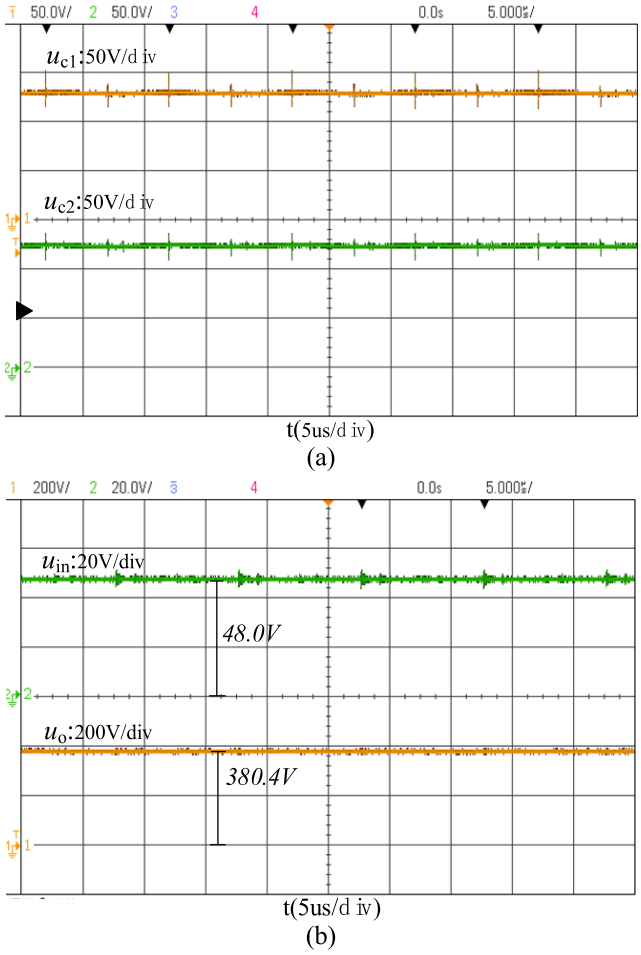

FIGURE 12. Waveforms of capacitors and input-output.

C. KEY CHARACTERISTICS COMPARISION

In order to demonstrate the proposed converter better, TABLE 1 shows some key characteristics of the converter and some similar converters.

We can observe from Table 1 that the proposed converter has a higher boost ratio in comparison to [23] and [25], and the input current ripple is lower than that of [23], and the voltage stress on diodes is lower than that in [7]. Likewise, the proposed converter shows a great superiority in the voltage stress across the switches which can be helpful to improve the efficiency. The input source of the converter in [25] has to charge a capacitor directly at every switching cycle, so the input current will have a large current spike. In addition, the proposed converter can perform better in the aforementioned characteristics when increasing the number of expansion units.

V. EXPERIMENT RESULTS AND ANALYSIS

In order to verify the correctness of the theoretical analysis, a 100W prototype was built with the specifications defined in Table 2.

TABLE 2. Parameter and components of prototype.

Symbol	Parameter	Value
P	Rated output power	100 W
V_{in}	Input voltage	48 V
V_o	Output voltage	380 V
f_s	Switching frequency	100 kHZ
L_1, L_2	Inductors	600 uH
S_1,S_2	Power MOSFETs	IRFP250MPBF
D_1,D_2,D_3	DIODEs	MUR840
C_1,C_2	Capacitors	2.2 uF
C_o	Capacitor	47 uF

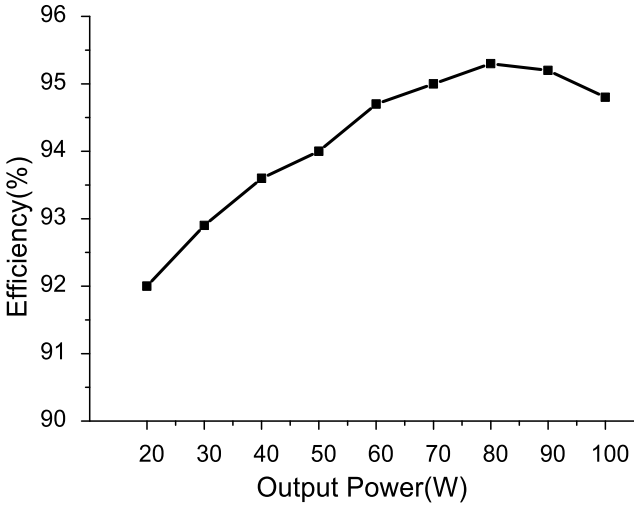

FIGURE 13. Efficiency curve.

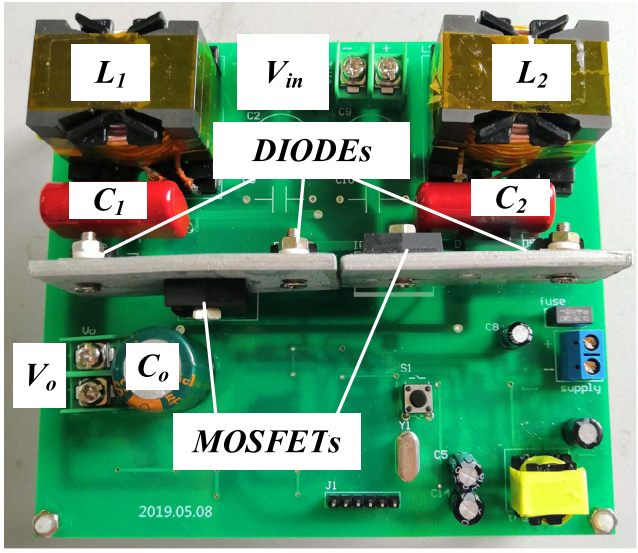

FIGURE 14. The experimental prototype.

The voltage waveforms of the switching devices are shown in Fig. 10. We can see that the duty cycle of the switch is only 0.631, the drain-source voltages of the two switches are 127.7 V and 125.1 V respectively, only one-third of the output voltage, and the voltage stresses across the three diodes are 125.5 V, 252.1 V and 253.3 V respectively. Therefore, small-on-resistance switches and low-voltage-rated diodes can be selected to improve the efficiency and lower the cost.

The waveforms of input current and inductor current are shown in Fig. 11. We can see that the input current ripple is only 212.2 mA which is much less than that of the conventional BOOST converter.

Fig. 12 shows the voltage waveforms. We can see that the voltages across the capacitors C_1, C_2 are basically constant and the output voltage is about 380.4 V.

Fig. 13 shows the efficiency curve of the experimental prototype. The efficiency increases first, and then it decreases after reaching the maximum value. The maximum efficiency of the prototype is around 95.3%, and the full-load efficiency is about 94.8%. The experimental prototype is shown in Fig. 14.

VI. CONCLUSION

For a better conversion of renewable energy, an interleaved high step-up DC/DC converter based on the switch-capacitor unit is proposed. The feasibility and theoretical analysis of the topology are verified by the experiment. The proposed topology has the following advantages:

1) The circuit can achieve higher voltage gain and prevent the switches from operating at the extreme duty cycle state.

2) The interleaved structure contributes to a lower input current ripple which is beneficial to the life of renewable energy modules.

3) The voltage stresses of the switching devices are greatly reduced and lower voltage switching devices can be selected to improve efficiency.

4) The circuit has good expandability. By increasing the number of parallel BOOST channels or switch-capacitor boost units, the input current ripple can be decreased observably, and the voltage gain, the efficiency and power density can be further improved.

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