Gd-Doped HfO2 Memristor Device, Evaluation Robustness by Image Noise Cancellation and Edge Detection Filter for Neuromorphic Computing

SHUBHRO CHAKRABARTTY[1], SUVOJIT ACHARJEE[2], ALAADDIN AL-SHIDAIFAT[1], MAINAK BISWAS[3], AND HANJUNG SONG[1]

[1]Department of Nanoscience and Engineering, Centre for Nano Manufacturing, Inje University, Gimhae 50834, South Korea
[2]Department of E & C Engineering, National Institute of Technology Agartala, Jirania 799046, India
[3]Department of CS & Engineering, JIS University, Agarpara 700109, India

Corresponding author: Hanjung Song (hjsong@inje.ac.kr)

ABSTRACT This paper estimates the robustness of non-volatile device (NVM) Gadolinium (Gd) doped Hafnium oxide (HfO2) nanoparticles (NPs) based memristor which was constructed using as-formed and annealed nanoparticles in 600 °C and 800 °C temperature, based on their performance in various basic image processing applications (i.e. edge detection filter and noise-canceling filter). A catalytic free glancing angle deposition technique (GLAD) is employed to grow Gd doped HfO2 nanoparticles (NPs) of 8 nm range on the thin film of Silicon oxide SiOx in 30 nm dimension. Annealing process is performed on Gd-doped HfO2 NPs and and the changes were demonstrated in its surface morphology. The elemental composition of the device was analyzed by Energy Dispersive X-ray (EDX). Photoluminescence (PL) analysis revealed that the topography and electrical characteristics of Gd-doped HfO2 alter swiftly after annealing process. A leakage current, interface state density (Dit) factor emphasizes that the device annealed at 600 °C portrayed significant improvement in the non-volatile characteristics in comparison with other devices. Additionally, the endurance of the device annealed at 600 °C was seen to possess more than decades of memory potential. The C-V and hysteresis curve measurement demonstrated maximal charge accumulation relative to other devices. Crossbar array is designed from both as-formed and annealed memristor devices.

INDEX TERMS Non-volatile memory, gadolinium (Gd), EDX, nanodots, interface state density.

I. INTRODUCTION

Recently, Memory Processing System (MPU) and Graphics Processing Technology (GPU) have being receiving substantial consideration for human retina diagnosis, some of the edge detection techniques followed include Laplace, Canny, Sobel and so on [1]. An MPU involves non-volatile devices (NVM) which plays a significant role in the artificial retina and brain computing applications [1]–[3]. Attractive charecterstics such as high density, better flexibility, low power consumption, and huge stability makes non-volatile memory (NVM) prolific and prominent for resistive random-access memory (RRAM) devices [3]–[6] and memristor devices [7], [1]. The RRAM and memristor devices have inherent memory so that they can easily retain information and make prolific for parallel computing paradigms [8]. In 1962, Hickmott [9] reported the resistive switching phenomena in materials such as SiOx, Al2O3, Ta2O5, ZrO2 and TiO2 materials. Various transition metal oxides were also explored for better resistive switching performance [10]. Hafnia is recently reported high performance non-volatile device and complementary metal-oxide-semiconductor (CMOS) devices which displayed characteristics such as high stability, wide band gap, excellent electrical properties, high dielectric permittivity (vary from $\varepsilon = 15$ to 27) [11], prolific endurance and good performance [12]. Various other

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researchers have reported such development of similar devices, for instance Rodriguez-Fernandez *et al.* [13], investigated TiN/Ti/HfO$_2$/TiN devices, Cabout *et al.* [14] have shown performance of HfO$_2$ with Pt, Ti and TiN electrode for resistive switching and Jiang *et al.* [15], have shown memristor performance in Ta/HfO$_2$/Pt combination. However, unacceptable leakage current, viability and scalability issues are bottlenecks in this area of research but few groups have worked efficiently to reduce the memory leakage issues by Gaussian filter [16]. In this draft, we have proposed an alternate system to counter this challenge. Moreover, various efforts are presented with metal nanocrystals such as Ni [17], Ir [18], Pt [19] and Au [20] with HfO2 films which improved the retention characteristics. Currently, Lu [21], Al [22], Zr [23] etc., dopants have been incorporated with HfO$_2$ but the formation of oxygen-related defect states, better switching and controlling dopant concentration for better NVM devices are still challenging. Therefore, Gadolinium (Gd) doped HfO$_2$ nanoparticles are fabricated by using a physical vapour deposition process to mitigate this issue and increase oxygen defect-related traps and provide better endurance in the device [24]. Apart from the above said investigations, crossbar memory has noteworthy advantages in parallel computing i.e., better storage, fast processing, etc., and those advantages could be useful for image processing applications [1]. Various types of fabrication processes are incorporated to grow HfO$_2$ films such as atomic layer deposition process [25], Sol-gel process [26] and RF magnetron sputtering [27]. Herein, Sobel filter is designed using 3×3 non-volatile memory-based crossbar, which is applied on images to find out the effectiveness and robustness for solving the complexity of neuro-artificial computing [1], [28]. The optimal charge storage in Gd based HfO$_2$ nanoparticles NVM devices is also presented. The catalytic free, controlled porosity and stable glancing angle deposition technique to make Gd doped HfO$_2$ nanoparticles on SiOx insulating layer. The prepared samples are annealed in different temperature and characterized by using field emission gun-scanning electron microscopes (FEG-SEM, JEOL, JSM-7600F) and element mapping by using EDX analysis. The paper is organized as follows: section 2 describes development methods of Gadolinium (Gd) doped Hafnium oxide (HfO2) nanoparticles on SiOx thin film with Copper bottom contact on Si substrate, while section 3 discussed different analytical procedures based on which the performance of NVM devices are evaluated. This section also investigates the robustness of NVM devices under different image processing applications. The section 4 concludes the overall outcome. The Figure 1 presents the schematic, of endurance of Ag/Gadolinium (Gd) doped Hafnium oxide (HfO$_2$) nanoparticles/SiOx Thin film/ Cu/ Si substrate.

II. DEVELOPMENT AND METHOD

In this section, the development of the Gd-HfO$_2$ NVM device layer and horizontal Sobel Filter using proposed 3×3 crossbar array would be discussed. The experimental procedure of
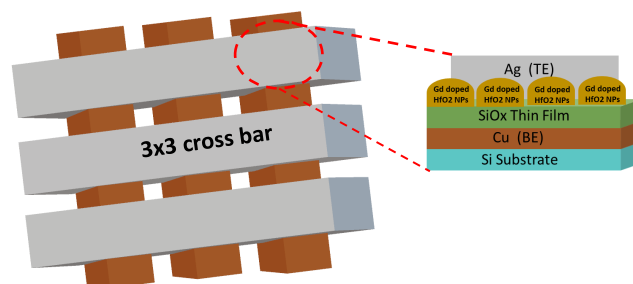

FIGURE 1. Device Schematic and 3 × 3 crossbar array.

Gd-HfO$_2$ will be explained in detail in the following subsection. The Analog image processing using NVM device, image noise cancellation and edge detection filter will be described in the process.

A. EXPERIMENTAL PROCEDURE

The experimental process includes a glancing angle deposition technique which is a combination of oblique angle deposition (OAD) and azimuthal rotation. In this procedure, vapour flux is deposited over a substrate which is fixed in an incident angle while Silicon (Si) substrate is properly cleaned by the RCA method during inception. At the inception copper (Cu, 99.995% pure) electrode at bottom was deposited through aluminum mask on the substrate. Furthermore, a 30 nm film of Silicon oxide (SiOx) is grown over it by using perpendicular deposition method. A Gadolinium (Gd) doped-Hafnium dioxide (HfO$_2$) nanoparticles in 8 nm range is also grown over SiOx film. The Gd-HfO$_2$ pellets are prepared by mixing third Gd$_2$O$_3$ (99.995% purity, MTI USA) and two-third of HfO$_2$ (99.995% purity, MTI USA) with polyvinyl alcohol and held in hydraulic pressed for 20 minutes. The rate of evaporation is almost ~ 0.14 nm s^{-1} and the vacuum pressure is maintained at 5.2×10^{-6} mbar. The thickness of the deposited film is monitored by using a digital thickness monitor. Subsequently, two samples (Gd-HfO$_2$/SiOx/Cu) are separately treated by annealing process at different temperatures i.e., 600 °C and 800 °C for one hour by using tube furnace mistreatment even heating and cooling ramp of 4°C/min. Finally, a top electrode of silver (Ag, 99.995% pure) is grown by using an aluminum mask through perpendicular deposition. The Figure 1 shows a typical schematic representation of Transmission Electron Microscopy (TEM) image of grown nanoparticles, endurance and image of Gadolinium (Gd) doped Hafnium oxide (HfO$_2$) nanoparticles/SiOx Thin film/ Cu/ Si substrate and the effect after annealing at 600 °C and 800 °C. The samples are characterized by using scanning electron microscopy (SEM) where the gun vacuum is kept on 2.17e-009 mbar and analysis of Photoluminescence (PL) is examined. The electrical measurements are also performed by using Semiconductor parameter analyzer. The edge detecting Sobel filter using a crossbar pattern is implemented to check the robustness of the grown non-volatile devices. In the process we have clearly explained the experimental results
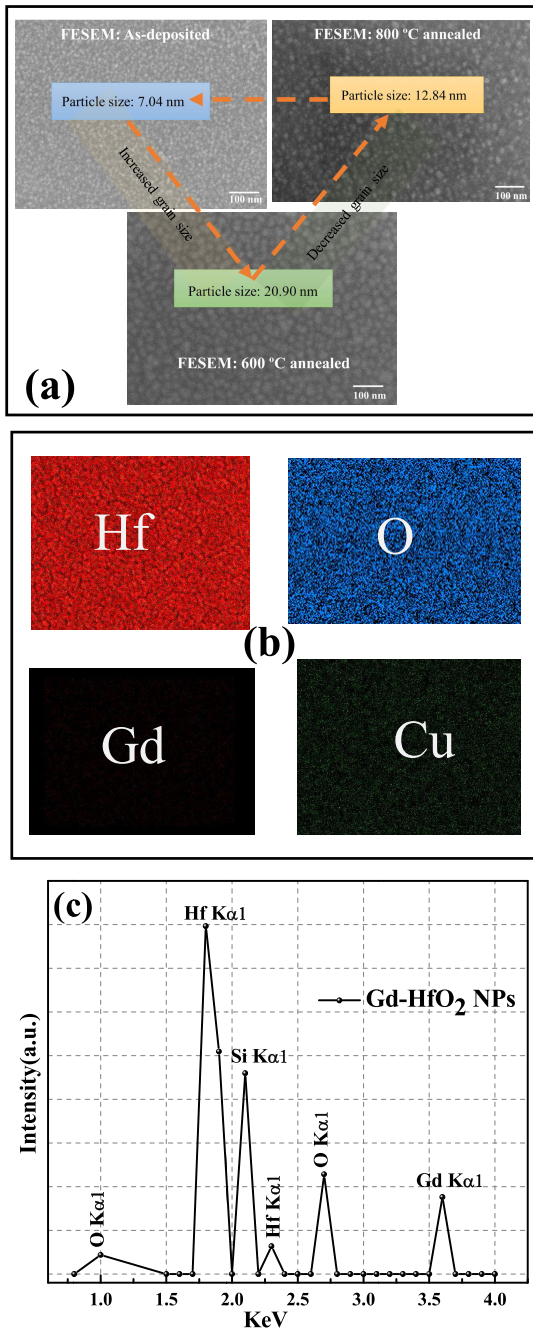
FIGURE 2. FEG-SEM images of HfO2 NPs/SiOx TF/Cu/Si (as-fabricated and 600°C and 800°C annealed samples) with its (a) Top view (b) Chemical mapping (c) EDX analysis.

one after the other. Additionally we have explained the application part supporting the established result from the analysis part.

III. RESULT AND DISCUSSION

A. ANALYSIS BASED ON EXPERIMENTAL PROCEDURES

1) ANALYSIS BASED ON STRUCTURE

A FEG-SEM image of respective (as-deposited, 600 °C and 800 °C) devces are illustrated in Figure 2(a). It can be observed that the particles size is seen to have increased
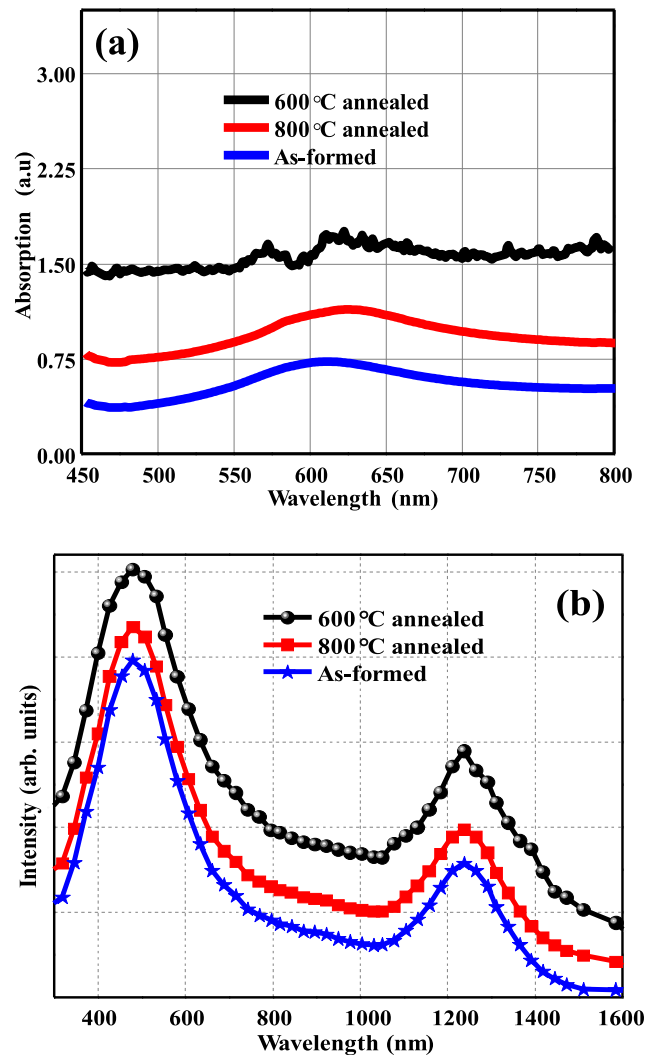

FIGURE 3. (a) Absorption (b) Photoluminescence (PL) analysis.

from 7.04 nm (Gd-HfO₂ as-deposited) to 20.90 (annealed at 600 °C) and furthermore annealing at 800 °C reduced the particle size of nano grains to 12.84 nm. Previous reports have reported the effect of increasing grain size by executing the thermal annealing process [29] but in this case grain size gets reduced at 800 °C, this mainly occurs due to mismatch in the coordination number of Hf and Si, and that actually produce larger number of dangling bonds in the interdiffusion region of Gd doped HfO₂ and SiOx. Therefore, trap sites are created by using dangling bonds to trap the more charges [30]. At higher annealing, the dangling bonds gets broken resulting in decrease of size of the particles Figure 2 (b) projects element mappings of presence of Hafnium (Hf), Silicon (Si), Gadolinium (Gd) and oxygen (O₂), in the samples. The spectrum projects the emission from Hf Kα1, O₂ K α1, Gd K α1, and Si K α1 shells are shown in Figure 2 (c).
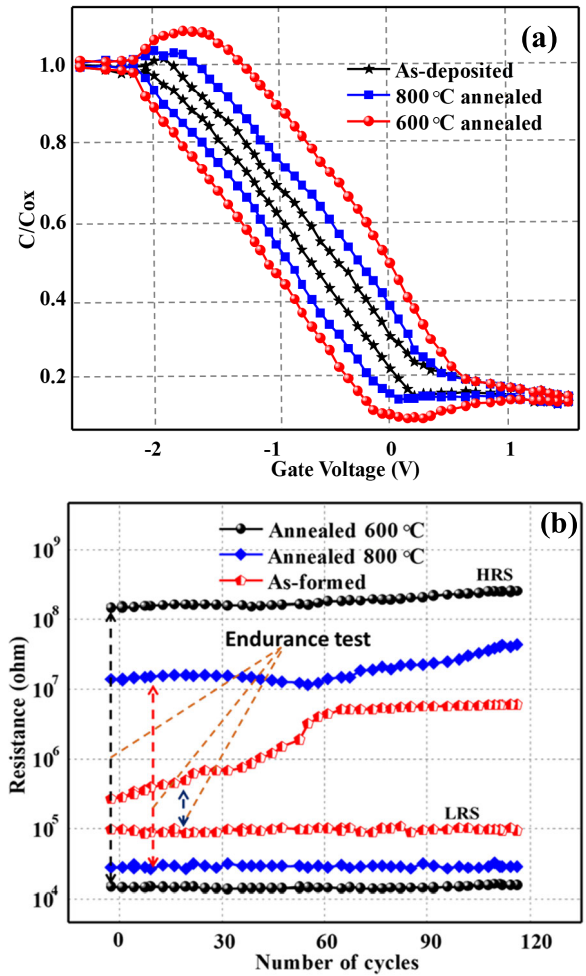
2) ANALYSIS BASED ON OPTICAL ABSORPTION

The absorption of as-formed and annealed samples was recorded by spectrophotometer (Figure 3 (a)). It is depicted
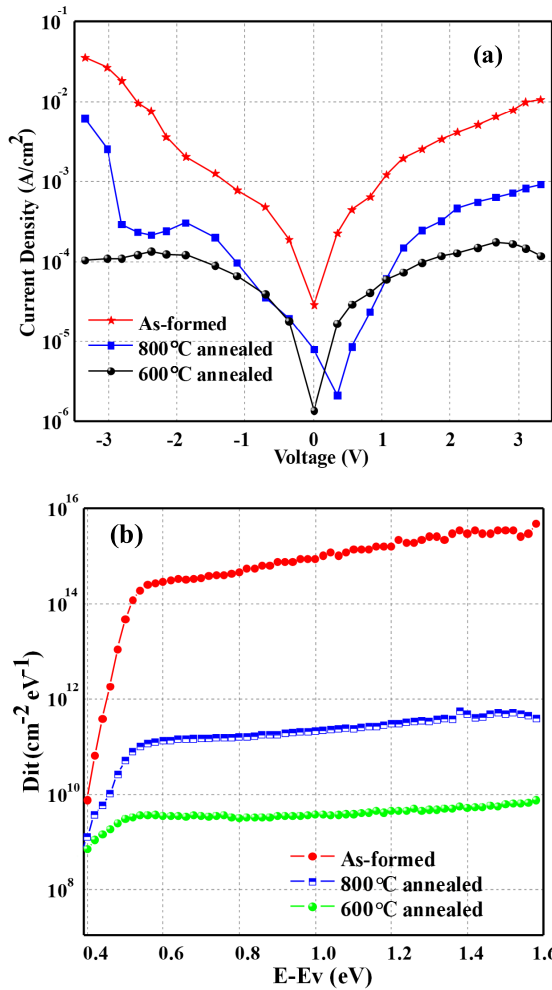
FIGURE 4. As-formed and annealed device at 600°C and 800°C with (a) J-V characteristics and (b) Effective interfacial traps.

FIGURE 5. (a) C-V measurement of as-formed and 600 °C and 800°C annealed device at 1MHz and (b) Endurance cycle of devices.

that enhanced absorption of ∼1.2 times is received for 600 °C Gd-HfO$_2$ NPs/SiOx TF annealed sample as compared to its as-formed. Furthermore, an increment in annealing temperature (800 °C), contributes decrement in absorption by almost one-fold. At higher temperature i.e. 800 °C, the blocking layer is formed i.e. Gadolinium silicate, which actually reduces the generation of electron-hole pair in the system [31]. The FESEM result (Figure 3 (a)) also verifies the morphology of particle size of Gd-HfO$_2$ NPs/SiOx TF, it can be seen that at 800 °C particle size was reduced as compare to sample annealed at 600 °C temperature. In Figure 3 (b), Photoluminescence (PL) intensity peak is observed at 543 and 1282 nm (Spectro-fluorophotometer (RF-540) by using 325 nm line of He-Cd laser as excitation source) and 600 °C annealed sample demonstrates pronounced intensity among other devices, which also supports the FESEM results (Figure.3 (a)). In-fact, oxygen defect increases with rising temperature due to pulling of oxygen from HfO$_2$, bringing less stress and creating sub-band gap transition which results in increase in intensity (in [32]) authors reported similar phenomenon where increment in

PL intensity of NPs layer is achieved as compared to thin film layer), but when the sample is annealed to 800 °C, the intensity decreases by some folds and it may be due to higher temperature (<600 °C) and development of dangling bonds (at 600 °C annealed) gets broken up. Therefore, it was observed that the intensity reduced in other case. Hence, Gd-HfO$_2$ 600 °C annealed sample is prominent for making memory device.

3) ANALYSIS BASED ON NON-VOLATILE CHARACTERISTICS OF DEVICES

A variation of current density for Gd doped HfO$_2$ NPs/SiOx TF/Cu/Si at 600 °C and 800 °C is shown in Figure 4 (a). It is very clear at the observation point that annealing process increases the grain size and the surface roughness through SEM analysis at 600 °C annealing process, but clear decrement is observed at 800 °C, it is found to clearly decrease due to lower decay process, which suppresses the excess carriers generated in 600 °C. A low leakage current of the order of almost ∼10^{-4} A/cm^2 is obtained at 600 °C annealed device. Actually, reduced leakage current is obtained because of low
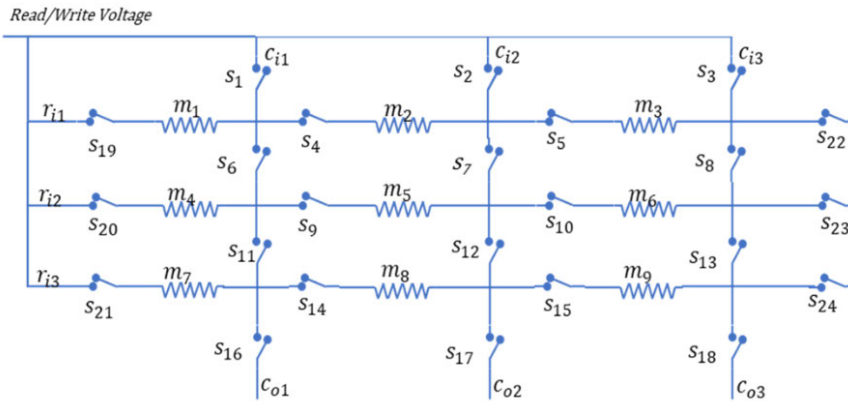
FIGURE 6. Arrangement of NVM devices and switches across 3 × 3 crossbar.
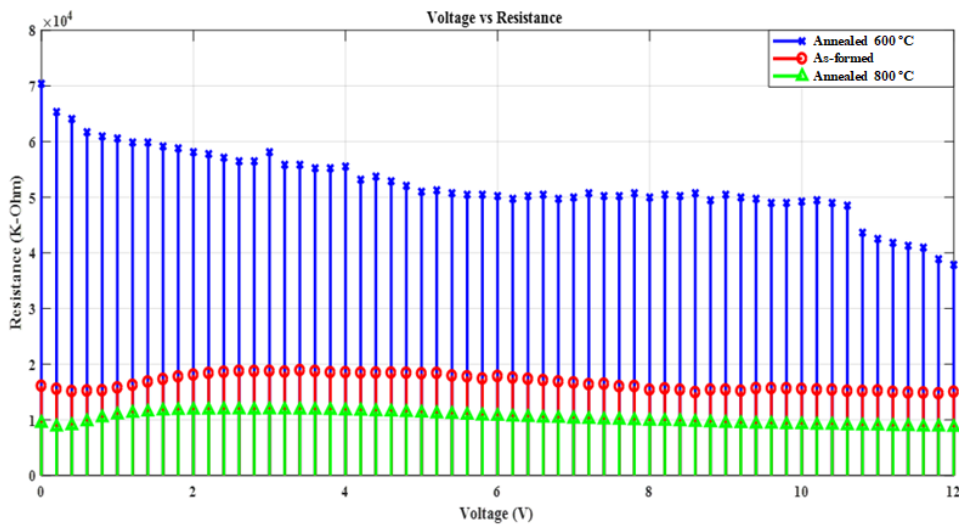

FIGURE 7. Variation of Voltage Vs Resistance in NVM devices.

trap density and better electron mobility for 600 °C device compared to 800°C annealed device. As-formed device found increment in the trap density which results in trap assisted tunneling that increases the leakage current and decreases the non-volatile performance of the device [33]. Figure 4 (b) shows the interface level traps (Dit) with respect to E-Ev curvature of as-formed and annealed devices. The extracted interface level traps density of as-formed at 600 °C and 800 °C annealed device is in the order of $\sim 10^{14}$ cm^{-2} eV^{-1}, 10^{09} cm^{-2} eV^{-1} and 10^{11} cm^{-2} eV^{-1} respectively. So, as-formed device has higher Dit factor among all annealed devices. This may be possibly occur because the as-formed device shows large leakage current (in Figure 4 (a)). Hence, the results suggested that lower trap density allows electrons to move fast and improves the charge storage capability at 600 °C annealed device.

4) ANALYSIS BASED ON CAPACITIVE PERFORMANCE AND ENDURANCE

Figure 5 illustrates C-V curve of the as-formed and annealed devices at 1MHz. The hysteresis curvature is achieved when
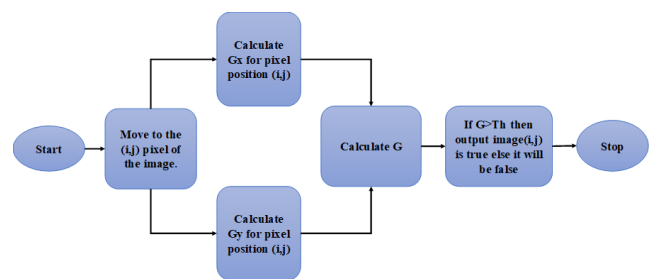
FIGURE 8. Sobel Filtering process.

gate voltage swept back and forth. It is justified from the output that electrons and holes are trapped significantly through the tunneling process which shows important characteristics to make non-volatile device. The clockwise and anti-clockwise sweep gives a larger memory window in the case of 600 °C annealed device, because of the larger electron trapped by annealing process. Furthermore, the endurance is measured for memory performance of as-formed and annealed devices with considering 0.5V of read voltage for resistance (Figure 5 (b)). NVM device presents repeated
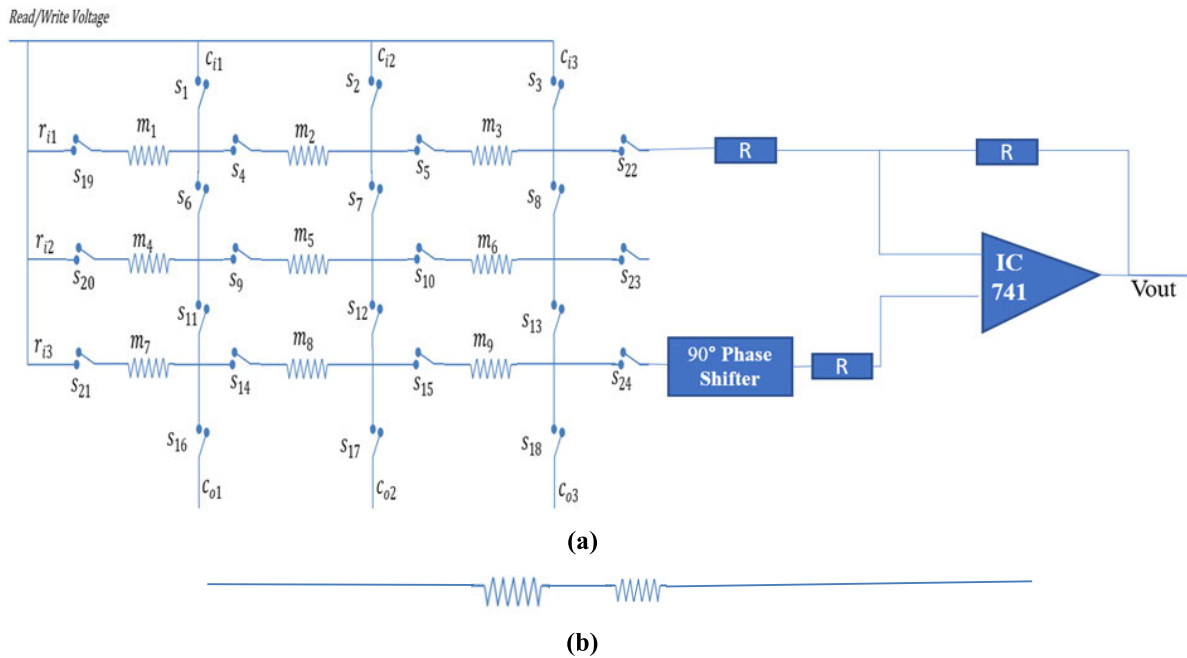
FIGURE 9. (a) Proposed cross-bar array to implement Sobel filter with the read circuit. (b) arrangement of NVM device for m$_2$ and m$_8$.

switching between low resistance state (LRS) and high resistance state (HRS). Here Gd-HfO$_2$ 600 °C annealed devices have maintained decades of stable endurance in 120 cycles because of larger oxygen vacancies, which created strong conductive path within the device.

This shows 600 °C annealed devices have promising retention and reproducible resistive switching property for NVM device.

B. ANALYSIS BASED ON PERFORMANCE IN APPLICATION
1) ANALOG IMAGE PROCESSING USING NVM DEVICE

Analog image processing through the NVM device is gaining interest in recent days [34]–[36]. As NVM devices are in continuous output states, each NVM has numerous resistive levels. Therefore, 8-bit pixel values of a Grayscale image can be stored by mapping the various resistive states with the equivalent Grayscale value. An N × N crossbar which consist of non-volatile memory device sandwiched between two metal electrodes, vertically and horizontally, [28], [37] was used to store the image of size N × N. Each pixel value at (x, y) [x, y <= N] will be represented by the NVM device at junction (x, y) in crossbar. The high resistive state (HRS) and the low resistive state (LRS) of the NVM device represent Grayscale pixel value 0 (dark intensity) and 255 (light intensity), respectively. All other pixel values are mapped to other resistive states between HRS and LRS. The resistive states can be achieved by applying various write voltage across the NVM devices. Arrangement of the NVM device in a 3 × 3 crossbar is shown in Figure 6. Here m$_n$ represents the n-th NVM device, s$_n$ represents switches essential to control the flow of signal through NVM devices, r$_{in}$ and c$_{in}$ represents

TABLE 1. Performance of HRS and LRS for as-formed and annealed devices.

Device	HRS with respective voltage	LRS with respective voltage	Variation in resistance	Decision Boundary of resistance level of two pixel
As-formed	18kΩ at 4V	15kΩ at 10 V	3 KΩ	0.011kΩ
600°C	70kΩ at 0V	15KΩ at 10 V	55 KΩ	0.214kΩ
800°C	11.8kΩ at 4V	8.7kΩ at 10 V	3.1 KΩ	0.012kΩ

the input row and column, r$_{on}$ and represents the output row and column.

The comparison of voltage versus resistance relation for fixed time duration signal of 0.02s (as shown in Figure 6) for NVM as-formed and annealed devices at different temperatures, was carried out and it concludes that the resistance changed linearly from 70 KΩ at 0V to 15 KΩ at 10V for NVM device annealed at 600 °C (Table 1). While change in resistance with applied voltage for as formed NVM device and NVM device annealed at 800 °C did not follow a linear relation (Figure 7). The difference between LRS and HRS is also higher for the NVM device annealed at 600 °C compared to as formed NVM and NVM annealed at 800 °C. From this comparison, NVM annealed at 600 °C is the most robust for different application. In this paper, kernel-based edge detection filter (i.e. Sobel filter) and noise-canceling filter (i.e. Mean filter) were designed using a crossbar of NVM to evaluate and compare the performance of as-formed as well
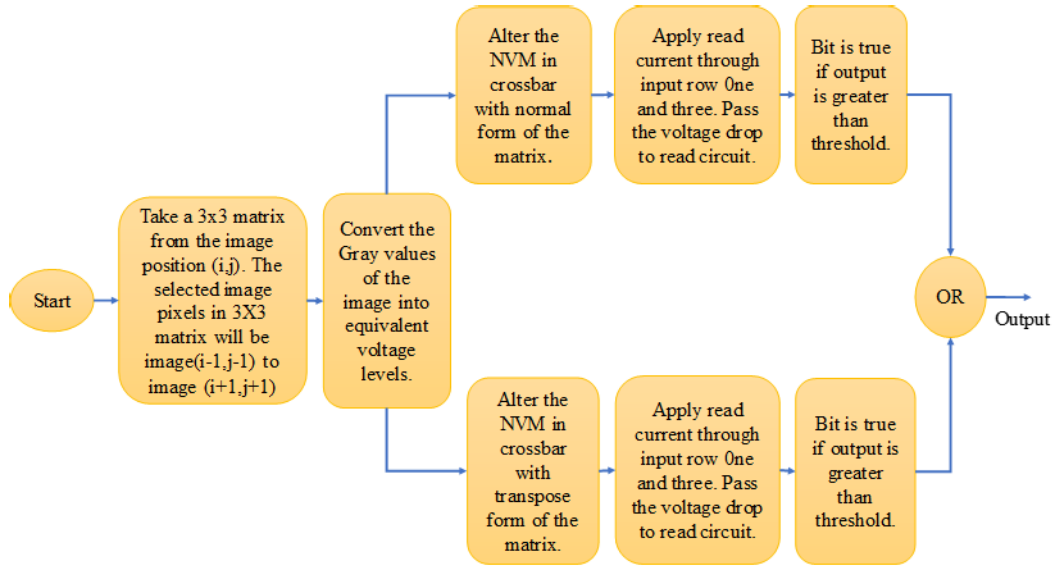
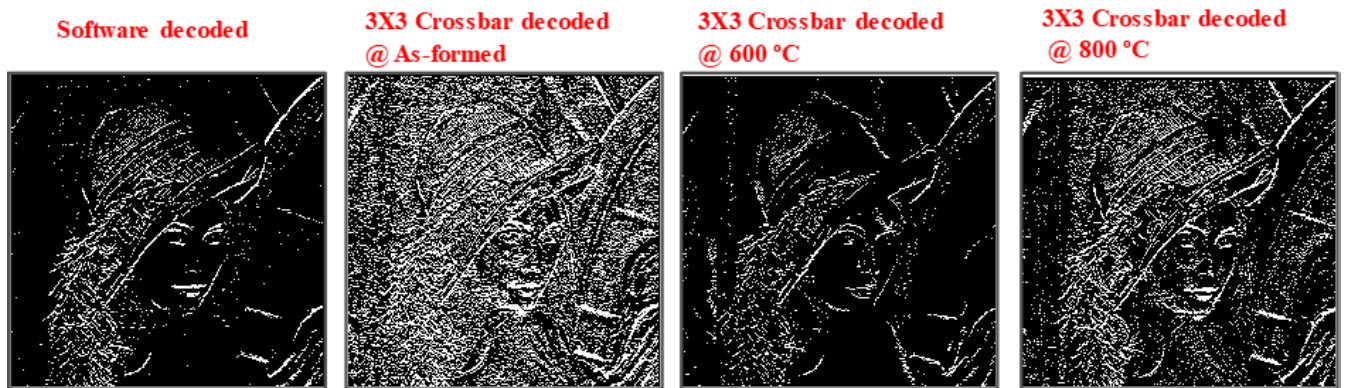**FIGURE 10.** Proposed flow charts for Sobel filtering using 3 × 3 crossbar.

FIGURE 11. Simulated demonstration of original image and output image by crossbar of NVM device.
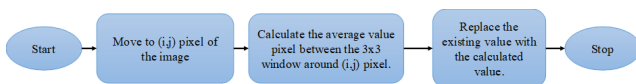

FIGURE 12. Flow chart to calculate mean filter.

as annealed NVM in different temperature. Simple convolution filters were implemented to compare the robustness in performance of various NVM devices as robust NVM device can be used for further complex filter structure.

## 2) KERNEL BASED EDGE DETECTING FILTER (SOBEL FILTER)

Sobel operator calculates the first order derivative of the function. The function is based on two independent variables. The first order derivative of the function can be calculated as a combination of partial differentiation of the function with respect to two independent variables.

$$\frac{\partial f}{\partial x \partial y} = \frac{\partial f}{\partial x} + \frac{\partial f}{\partial y}$$

An image can be described as a 2-dimensional function which describes the variation in light intensity in vertical and horizontal direction. To calculate the first order differentiation of an image, Sobel operator need to be applied in horizontal and vertical direction. First order differentiation increases the magnitude of the pixels which observes a sudden change in intensity i.e. transition pixels from background to foreground. The first order differentiation result was compared with a predefined threshold to decide whether the pixel belongs to the transition or not. Sobel filter kernel is represented by two matrices

$$Gx = \begin{bmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} \quad and \quad Gy = \begin{bmatrix} 1 & 0 & -1 \\ 2 & 0 & -2 \\ 1 & 0 & -1 \end{bmatrix}.$$

As Sobel filter is a sliding-window spatial convolution filter, both kernels moved all over the image to detect the pixels with sudden change in intensity. First kernel (Gx) detects the changes in horizontal direction and second kernel (Gy)
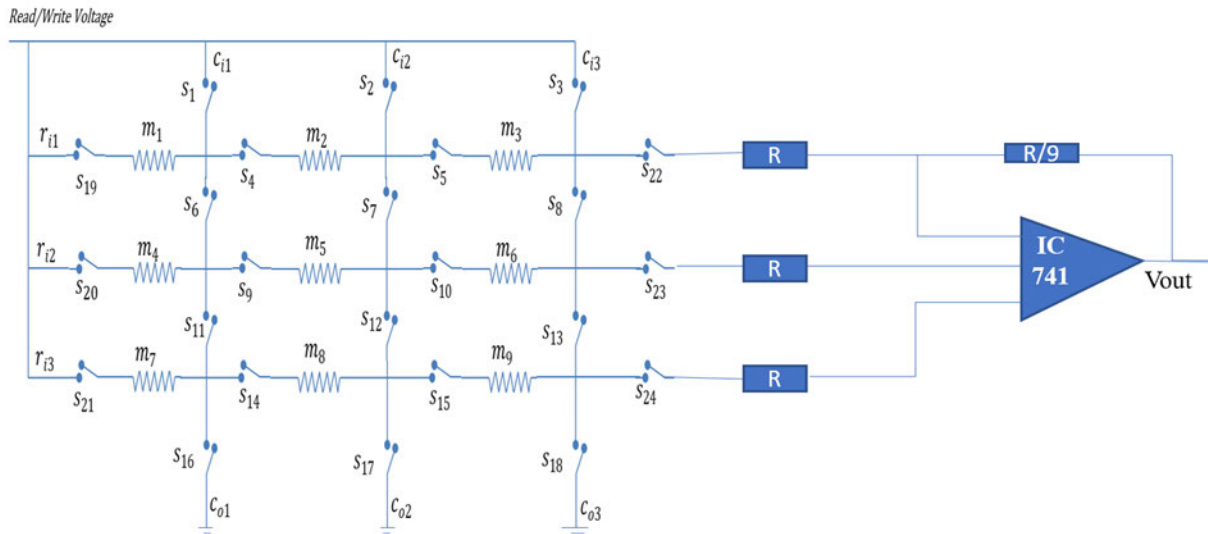
FIGURE 13. Proposed crossbar arrays to implement mean filter with the read circuit.
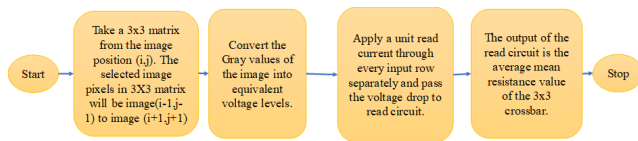
FIGURE 14. Proposed flow chart for Mean filter implemented using 3 × 3 Crossbar.

detects the changes in vertical direction. By combining both the result using (1) the overall Sobel filter output was calculated. Flow chart (Figure 8) to calculate the Sobel filter output is shown in the below flowchart.

$$G = \sqrt{Gx^2 + Gy^2} \tag{1}$$

a: IMPLEMENTATION OF SOBEL FILTER USING CROSSBAR
A crossbar of 3 × 3 size made up of NVM device (as shown in Figure 9a), is used to represent the Sobel filter kernel. This crossbar is a little different than our previous crossbar structure shown in Figure 6. In the crossbar structure presented in Figure 9a, m_2 and m_8 are representing two NVM devices connected in series (as shown in Figure 9b).

Two crossbars were used to detect the changes in horizontal and vertical direction. Initially, all the NVM device was placed at Roff value. The image pixel values were used to alter the resistive states of NVM devices at the junction of the crossbar. At the beginning of the calculation, the first 3 × 3 matrix from the image was passed in normal form and transpose from two crossbars. Crossbar which was written with normal form of the matrix traced the change in horizontal direction and the other one detected the change in vertical direction. Figure 10 shows the flow chart representation that calculate the outcome of the horizontal and vertical kernel of Sobel filter using crossbar.

A read signal with a current I was applied through the first and third input row. Voltage drop at first output row is given by:

$$V1 = I(R(1, 1) + 2R(1, 2) + R(1, 3))$$

The voltage drop at the second row is 0 as no read signal was applied in this row. Voltage drop at third output row is given by:

$$V3 = I(R(3, 1) + 2R(3, 2) + R(3, 3))$$

Voltage drop V1, V2, V3 was passed to the read circuit. V3 was passed through a phase shifter before it was applied in the read circuit. The overall voltage output is given by:

$$\begin{aligned} Vout &= V1 + V2 - V3 \\ &= I((R(1, 1) + 2R(1, 2) + R(1, 3)) \\ &\quad - (R(3, 1) + 2R(3, 2) + R(3, 3)) \end{aligned}$$

Two separate outputs will be obtained for the vertical and horizontal kernel and both will be logical output after passing through the comparator. A logical OR operation between the output of horizontal and vertical kernel is the overall outcome of the Sobel filtering process.

b: RESULT
The design of Sobel Filter with 3 × 3 crossbar of non-volatile devices is explained well in the methodology section (Figure 9 (a)). To capture or process a Grayscale image, it needs 256 levels and this level can be achieved by altering the resistance values of the crossbars. So, the device with the maximum difference in their HRS and LRS is the most suitable candidate for image acquisition. A high difference increases the decision boundary and reduce the chance of

FIGURE 15. Output of decoded image through different crossbars.

false detection. From Table 1 and Figure 7, it can be concluded that the NVM device annealed at 600 °C will perform better than the other two options.

Figure 11 shows the comparison of the outputs of the Sobel filtering process performed through software, crossbar of as formed NVM devices and annealed NVM devices. Output from 600 °C annealed crossbar shows the best correlation (0.8) with software decoded image.

3) KERNEL BASED EDGE DETECTING FILTER (SOBEL FILTER)

Noise cancellation is one of the most important parts of image pre-processing to improve the result of later processing. Averaging filter or mean filter is one of the basic filters which can be applied to eliminate noise. Mean filter replaces the pixel value in an image with the mean value of its neighboring pixels. This will eliminate the sudden change in an image by changing the pixel value which is not in accordance with its surroundings. Like Sobel filter it is also kernel-based filter. The kernel represents the shape and size of the neighborhood which is going to be considered for calculating the mean. The 3×3 mean filter kernel can be represented by

$$Mx = \begin{bmatrix} \frac{1}{9} & \frac{1}{9} & \frac{1}{9} \\ \frac{1}{9} & \frac{1}{9} & \frac{1}{9} \\ \frac{1}{9} & \frac{1}{9} & \frac{1}{9} \end{bmatrix}.$$

This kernel moved all over the image to calculate mean pixel values. Flow chart to calculate the output is shown in the below flowchart 12.

a: IMPLEMENTATION OF MEAN FILTER USING CROSSBAR

A crossbar structure as shown in Figure 13 was used to represent the kernel of mean filter. This structure was similar to the crossbar structure in Figure 6. Unlike the Sobel structure, here all the junction carries a single NVM device. Initially all the NVM device are placed at R_{off} value. The write and read process on crossbar are similar like described in the Sobel filter process.

In the beginning, the kernel was placed at the first pixel of the image and the first pixel (row = 1, column = 1)

value of the image was converted to respective write voltage and applied on NVM positioned at first junction (row = 1, column = 1) of the crossbar. Similarly, second pixel (row = 1, column = 2) and third pixel (row = 1, column = 3) values was used to change the resistance of NVM positioned at second junction (row = 1, column = 2) and third junction (row = 1, column = 3) of the crossbar. A read signal with current I was applied through in each input row. Overall crossbar with the applied read circuit is shown in Figure 13. Figure 14 shows the flow chart representation to calculate the outcome of the mean filter process using a crossbar.

Voltage drop at row 1 (for horizontal kernel) or Column 1 (for vertical kernel) is given by:

$$V1 = I(R(1, 1) + R(1, 2) + R(1, 3))$$

Voltage drop at row 2 (for horizontal kernel) or Column 2 (for vertical kernel) is given by:

$$V2 = I(R(2, 1) + R(2, 2) + R(2, 3))$$

Voltage drop at row 3 (for horizontal kernel) or Column 3 (for vertical kernel) is given by:

$$V3 = I(R(3, 1) + R(3, 2) + R(3, 3))$$

Voltage drop V1, V2, V3 was then passed to the read circuit (shown in Figure 13). V3 was passed through a phase shifter before it was applied in read circuit.

The overall voltage output after read circuit is given by:

$$\begin{aligned} Vout &= V1 + V2 + V3 \\ &= \frac{I}{9}(R(1, 1) + R(1, 2) + R(1, 3) + R(2, 1) \\ &\quad + R(2, 2) + R(2, 3) + R(3, 1) + R(3, 2) + R(3, 3)) \end{aligned}$$

The output voltage was obtained at the end of read circuit used to write the changed value in pixel position.

b: RESULT

A test image infused with Gaussian noise was used as an input image to test the effectiveness of noise-canceling filter. Figure 15 compares the output of the mean filtering process performed through software, crossbar of as formed NVM devices and annealed NVM devices. A high correlation

(0.93) between software decoded output and the output of crossbar constructed from NVMs annealed at 600 °C represents the best efficiency than the performance of other NVM (as-formed and 800 °C).

IV. CONCLUSION

This work concludes Gadolinium (Gd)-doped-HfO2 nanoparticles in 8nm dimensions is prepared by low cost, efficient catalytic free GLAD technique. The effect of open-air thermal annealing is investigated among the devices. FESEM images depicted the growth of particles from the range of 7.04 nm to 20.90 nm. The grown nanoparticles over thin film with 600 °C as optimal annealing process could improve the surface roughness and charge accumulation cum retention characteristics ability of the device. C-V measurements elucidated the optimum charge trapping memory in 600 °C annealed devices. A low leakage current and low interface level traps (Dit) factor are extracted by 600 °C. The sobel filter is implemented using a 3×3 crossbar array of NVM devices. Hence, Gd/HfO₂ NPs annealed at 600 °C device with maximum variation in their resistance value having a correlation greater than 0.93 between software decoded image and crossbar image output. So, 600 °C annealed devices have great similarity between desired results and actual output. It maintains more than decades of memory window for more than 100 cycles. Hence, higher oxygen affinities, reduced power of 600 °C annealed Gd-doped HfO₂ NPs based device make it progressive for developing memristor devices.

REFERENCES

[1] A. Róka, Á. Csapó, B. Reskó, and P. Baranyi, "Edge detection model based on involuntary eye movements of the eye-retina system," *Acta Polytechnica Hungarica*, vol. 4, no. 1, pp. 31–46, 2007.

[2] A. Al-Shidaifat, S. Kumar, and H. Song, "Voltage regulation of retina neuron model with dynamic feedback for biological acquisition image," *BioChip J.*, vol. 11, no. 4, pp. 300–307, 2017.

[3] M. A. Zidan, J. P. Strachan, and W. D. Lu, "The future of electronics based on memristive systems," *Nature Electron.*, vol. 1, no. 1, p. 22, Jan. 2018.

[4] F. Zhou, Y.-F. Chang, B. Fowler, K. Byun, and J. C. Lee, "Stabilization of multiple resistance levels by current-sweep in SiO_x-based resistive switching memory," *Appl. Phys. Lett.*, vol. 106, no. 6, 2015, Art. no. 063508.

[5] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal-oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

[6] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, 2009.

[7] L. Chua, "Resistance switching memories are memristors," *Appl. Phys. A, Solids Surf.*, vol. 102, no. 4, pp. 765–783, 2011.

[8] T. D. Dongale, K. V. Khot, S. V. Mohite, N. D. Desai, S. S. Shinde, V. L. Patil, S. A. Vanalkar, A. V. Moholkar, K. Y. Rajpure, P. N. Bhosale, P. S. Patil, P. K. Gaikwad, and R. K. Kamat, "Effect of write voltage and frequency on the reliability aspects of memristor-based RRAM," *Int. Nano Lett.*, vol. 7, no. 3, pp. 209–216, 2017.

[9] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films," *J. Appl. Phys.*, vol. 33, no. 9, pp. 2669–2682, 1962.

[10] X. Hong, D. J. Loy, P. A. Dananjaya, F. Tan, C. Ng, and W. Lew, "Oxide-based RRAM materials for neuromorphic computing," *J. Mater. Sci.*, vol. 53, no. 12, pp. 8720–8746, 2018.

[11] N. Kumar, B. P. A. George, H. Abrahamse, V. Parashar, S. S. Ray, and J. C. Ngila, "A novel approach to low-temperature synthesis of cubic HfO₂ nanostructures and their cytotoxicity," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 9351.

[12] F.-Y. Yuan, N. Deng, C.-C. Shih, Y.-T. Tseng, T.-C. Chang, K.-C. Chang, M.-H. Wang, W.-C. Chen, H.-X. Zheng, H. Wu, H. Qian, and S. M. Sze, "Conduction mechanism and improved endurance in HfO₂-based RRAM with nitridation treatment," *Nanoscale Res. Lett.*, vol. 12, no. 1, 2017, Art. no. 574.

[13] A. Rodriguez-Fernandez, C. Cagli, L. Perniola, E. Miranda, and J. Suñé, "Characterization of HfO₂-based devices with indication of second order memristor effects," *Microelectronic Eng.*, vol. 195, pp. 101–106, Aug. 2018.

[14] T. Cabout, J. Buckley, C. Cagli, V. Jousseaume, J.-F. Nodin, B. de Salvo, M. Bocquet, and C. Müller, "Resistance switching variability in HfO₂-based memory structures with different electrodes," in *Proc. EMRS Spring Meeting*, 2012, pp. 1–27.

[15] H. Jiang, L. Han, P. Lin, Z. Wang, M. H. Jang, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin, and Q. Xia, "Sub-10 nm Ta channel responsible for superior performance of a HfO₂ memristor," *Sci. Rep.*, vol. 6, Jun. 2016, Art. no. 28525.

[16] J. K. Eshraghian, S.-M. Kang, S. Baek, G. Orchard, H. H.-C. Iu, and W. Lei, "Analog weights in ReRAM DNN accelerators," in *Proc. IEEE Int. Conf. Artif. Intell. Circuits Syst.*, Mar. 2019, pp. 267–271.

[17] Z. Tan, S. Samanta, W. J. Yoo, and S. Lee, "Self-assembly of Ni nanocrystals on HfO₂ and N-assisted Ni confinement for nonvolatile memory application," *Appl. Phys. Lett.*, vol. 86, no. 1, 2005, Art. no. 013107.

[18] T. T.-J. Wang, C.-L. Chu, I.-J. Hsieh, and W.-S. Tseng, "Formation of iridium nanocrystals with highly thermal stability for the applications of nonvolatile memory device with excellent trapping ability," *Appl. Phys. Lett.*, vol. 97, no. 14, 2010, Art. no. 143507.

[19] R. C. Jeff, Jr., M. Yun, B. Ramalingam, B. Lee, V. Misra, G. Triplett, and S. Gangopadhyay, "Charge storage characteristics of ultra-small Pt nanoparticle embedded GaAs based non-volatile memory," *Appl. Phys. Lett.*, vol. 99, no. 7, Aug. 2011, Art. no. 072104.

[20] V. Mikhelashvili, B. Meyler, S. Yoffis, J. Salzman, M. Garbrecht, T. Cohen-Hyams, W. D. Kaplan, and G. Eisenstein, "A nonvolatile memory capacitor based on Au nanocrystals with HfO₂ tunneling and blocking layers," *Appl. Phys. Lett.*, vol. 95, no. 2, 2009, Art. no. 023104.

[21] T. C. U. Tromm, J. Zhang, J. Schubert, M. Luysberg, W. Zander, Q. Han, P. Meuffels, D. Meertens, S. Glass, P. Bernardy, and S. Mantl, "Ferroelectricity in Lu doped HfO₂ layers," *Appl. Phys. Lett.*, vol. 111, no. 14, 2017, Art. no. 142904.

[22] S. Spiga, F. Driussi, G. Congedo, C. Wiemer, A. Lamperti, and E. Cianci, "Sub-1 nm equivalent oxide thickness Al-HfO₂ trapping layer with excellent thermal stability and retention for nonvolatile memory," *ACS Appl. Nano Mater.*, vol. 1, no. 9, pp. 4633–4641, 2018.

[23] C.-C. Lin, Y. Kuo, and S. Zhang, "Nonvolatile memory devices with AlO_x embedded Zr-doped HfO₂ high-*k* gate dielectric stack," *J. Vac. Sci. Technol. B, Microelectron.*, vol. 32, no. 3, 2014, Art. no. 03D116.

[24] R. Chattopadhyay, *Surface Wear: Analysis, Treatment, and Prevention*. Cleveland, OH, USA: ASM International, 2001.

[25] J. Gope, Vandana, N. Batra, J. Panigrahi, R. Singh, K. K. Maurya, R. Srivastava, and P. K. Singh, "Silicon surface passivation using thin HfO₂ films by atomic layer deposition," *Appl. Surf. Sci.*, vol. 357, pp. 635–642, Dec. 2015.

[26] Y. Aoki, T. Kunitake, and A. Nakao, "Sol-gel fabrication of dielectric HfO₂ nano-films; formation of uniform, void-free layers and their superior electrical properties," *Chem. Mater.*, vol. 17, no. 2, pp. 450–458, 2005.

[27] A. Vinod, M. S. Rathore, and N. S. Rao, "Effects of annealing on quality and stoichiometry of HfO₂ thin films grown by RF magnetron sputtering," *Vacuum*, vol. 155, pp. 339–344, Sep. 2018.

[28] X. Hu, S. Duan, L. Wang, and X. Liao, "Memristive crossbar array with applications in image processing," *Scientia Sinica Informationis*, vol. 41, no. 4, pp. 500–512, 2011.

[29] C. Yakopcic, R. Hasan, and T. M. Taha, "Flexible memristor based neuromorphic system for implementing multi-layer neural network algorithms," *Int. J. Parallel, Emergent Distrib. Syst.*, vol. 33, no. 4, pp. 408–429, 2018.

[30] S. Chakrabartty, A. Mondal, and A. K. Saha, "Effect of annealing on optical, electrical and charge trapping properties of TiO₂ NPs arrays," *J. Nanosci. Nanotechnol.*, vol. 17, no. 2, pp. 1300–1306, 2017.

[31] X. Yan, T. Yang, X. Jia, J. Zhao, and Z. Zhou, "Impacts of thermal annealing temperature on memory properties of charge trapping memory with NiO nano-pillars," *Phys. Lett. A*, vol. 381, no. 10, pp. 913–916, 2017.

[32] S. Chakrabartty, S. Kumar, H. Song, and M. Jeon, "Ag/TiO₂ NPs/TiO₂ TF/Si based non-volatile memristor device for neuromorphic computing applications," *J. Nanoscience Nanotechnol.*, vol. 18, no. 11, pp. 7912–7916, 2018.

[33] P. Singh, R. K. Jha, R. K. Singh, and B. R. Singh, "On the structural and electrical properties of metal–ferroelectric–high *k* dielectric–silicon structure for non-volatile memory applications," *Bull. Mater. Sci.*, vol. 41, no. 4, p. 101, 2018.

[34] L. Petropoulos and S. C. Wong, "Correction of corrupted elements in sensors using analog/multi-level non-volatile memory," U.S. Patent 6 760 068 B2, Jul. 6, 2004.

[35] J. Heller and J. Breisch, "CMOS imaging device with integrated defective pixel correction circuitry," U.S. Patent 6 396 539 B1, May 28, 2002.

[36] M. J. Marinella, R. B. Jacobs-Gedrim, C. Bennett, A. H. Hsia, D. R. Haghart, C. D. James, and A. A. Yalin, "Energy efficient neuromorphic algorithm training with analog memory arrays," Sandia Nat. Laboratories, Albuquerque, NM, USA, Tech. Rep., 2019.

[37] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves, Z. Li, J. P. Strachan, P. Lin, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, and Q. Xia, "Analogue signal and image processing with large memristor crossbars," *Nature Electron.*, vol. 1, no. 1, pp. 52–59, Jan. 2018.

SHUBHRO CHAKRABARTTY received the B.Tech. degree in electronics and communication engineering and the M.Tech. degree in electronics from Pondicherry Central University, and the Ph.D. degree from the National Institute of Technology Agartala. He has also done his postdoctoral studies in CSIR-funded project from the National Institute of Technology Durgapur. He has published his findings in 16 SCI journals of good repute. Recently, he has applied for a Korean patent. His research work comprises of nano fabrication and design, low power circuit design, and fabrications of memristors for neuromorphic applications.

SUVOJIT ACHARJEE received the M.Tech. degree from Jadavpur University, India, where he is currently pursuing the Ph.D. degree. He is currently with the National Institute of Technology Agaratala. His areas of interests include digital image processing, soft computing, and optimization. He has published his findings in five SCI journals.

ALAADDIN AL-SHIDAIFAT received the B.S. degree in software engineering from Al-Hussein Bin Talal University, Jordan, in 2011, and the M.Eng. degree in computer engineering from Inje University, South Korea, in 2015, where he is currently pursuing the Ph.D. degree with the Nanoscience and Engineering Department, joining Nano Circuit Design Laboratory (NCDL). His research interests include medical image processing, computer vision, integrated circuits, computational sensors, smart structures, and neuromorphic applications.

MAINAK BISWAS received the B.Tech. degree in information technology from the Government College of Engineering and Ceramic Technology, Kolkata, India, in 2007, the M.Tech. degree in distributed and mobile computing from Jadavpur University, Kolkata, India, in 2009, and the Ph.D. degree from the National Institute of Technology Goa, Farmagudi, India. He was an Assistant Professor with O.P. Jindal University, Raigarh, India, from 2009 to 2013, and the Madhav Institute of Technology and Science, Gwalior, India, from 2014 to 2015. He has authored or coauthored and has presented articles in various international journals and conferences.

HANJUNG SONG was born in South Korea. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Hanyang University, South Korea, in 1986, 1988, and 2000, respectively. He joined the Nano Design Circuit Laboratory, Inje University, South Korea, in 2004, where he is currently the Head and a Professor with the Department of Nanoscience Engineering. He has published several research articles in referred international journals. He is carrying out three sponsored research projects as a Principal Investigator. His research interests include power IC circuit design, analog VLSI design of silicon neuron system and chaotic circuit, and semiconductor device modeling and reliability.

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